



General Description

- Proprietary α MOS5™ technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

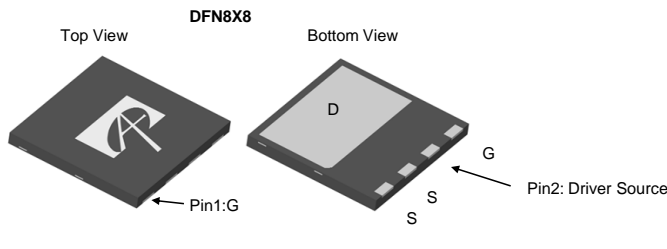
Applications

- SMPS with PFC, Flyback and LLC topologies
- Micro inverter with DC/AC inverter topology

Product Summary

$V_{DS} @ T_{j,max}$	700V
I_{DM}	96A
$R_{DS(ON),max}$	< 0.18 Ω
$Q_{g,typ}$	46nC
$E_{oss} @ 400V$	4.9 μ J

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONV180A60	DFN8x8_4L_EP1_S	Tape & Reel	3500

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	V
Gate-Source Voltage (dynamic) AC (f>1Hz)	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	24
		$T_C=100^\circ\text{C}$	15
Pulsed Drain Current ^C	I_{DM}	96	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	4.3
		$T_A=70^\circ\text{C}$	3.4
Avalanche Current ^C	I_{AR}	6	A
Repetitive avalanche energy ^C	E_{AR}	18	mJ
Single pulsed avalanche energy ^G	E_{AS}	172	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Diode reverse recovery	dv/dt		20
		di/dt	250
$V_{DS}=0$ to 400V, $I_F \leq 20A$, $T_j=25^\circ\text{C}$			A/us
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	250
		Derate above 25 $^\circ\text{C}$	2
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	8.3
		$T_A=70^\circ\text{C}$	5.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	12	15	$^\circ\text{C/W}$
$t \leq 10s$				
Maximum Junction-to-Ambient ^{A D}	$R_{\theta JC}$	0.31	0.50	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	Steady-State			

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600			V	
		I _D =250μA, V _{GS} =0V, T _J =150°C		700			
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.56		V/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V			1	μA	
		V _{DS} =480V, T _J =125°C			10		
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA		3		V	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A		0.16	0.18	Ω	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =12A		20		S	
V _{SD}	Diode Forward Voltage	I _S =12A, V _{GS} =0V		0.87	1.2	V	
I _S	Maximum Body-Diode Continuous Current				24	A	
I _{SM}	Maximum Body-Diode Pulsed Current ^C				96	A	
DYNAMIC PARAMETERS							
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		2340		pF	
C _{oss}	Output Capacitance				62		pF
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		56		pF	
C _{o(tr)}	Effective output capacitance, time related ^J				233		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1.3		pF	
R _g	Gate resistance	f=1MHz		5.4		Ω	
SWITCHING PARAMETERS							
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =12A		46		nC	
Q _{gs}	Gate Source Charge				17		nC
Q _{gd}	Gate Drain Charge				14		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =400V, I _D =12A, R _G =5Ω		34		ns	
t _r	Turn-On Rise Time				29		ns
t _{D(off)}	Turn-Off DelayTime				63		ns
t _f	Turn-Off Fall Time				19		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, dI/dt=100A/μs, V _{DS} =400V		387		ns	
I _{rrm}	Peak Reverse Recovery Current				30		A
Q _{rr}	Body Diode Reverse Recovery Charge				7.3		μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=2.4A, R_G=25Ω, Starting T_J=25° C.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

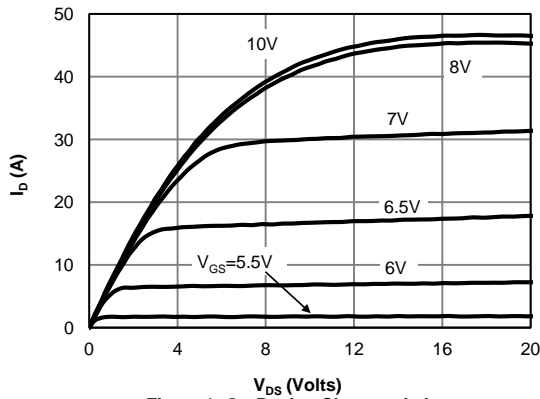


Figure 1: On-Region Characteristics

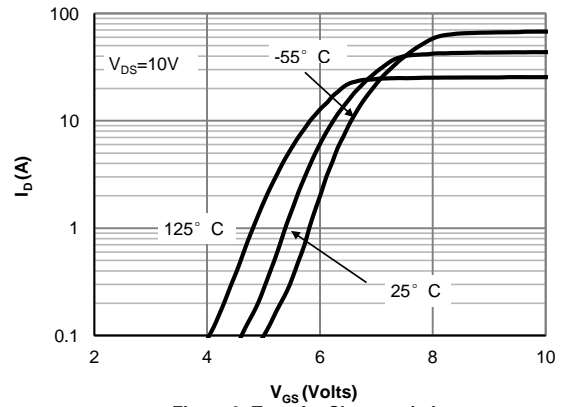


Figure 2: Transfer Characteristics

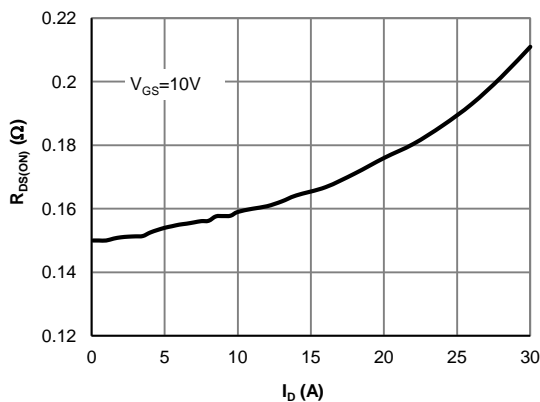


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

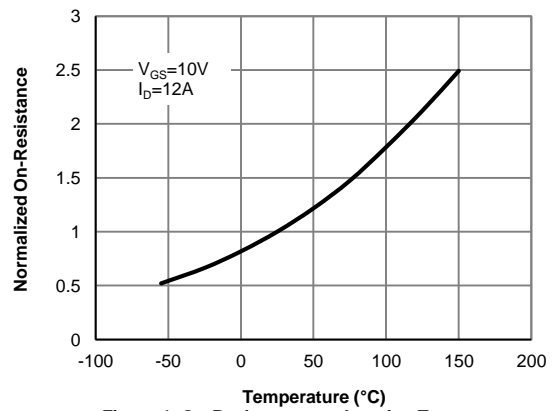


Figure 4: On-Resistance vs. Junction Temperature

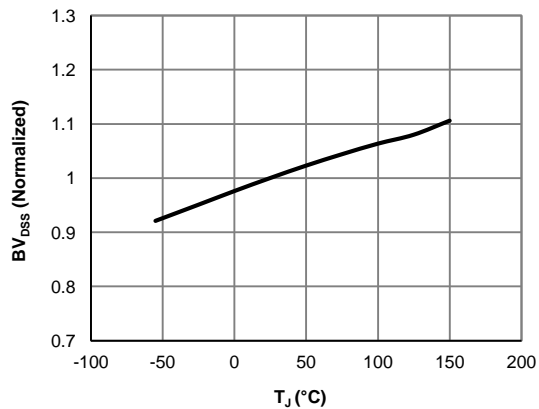


Figure 5: Break Down vs. Junction Temperature

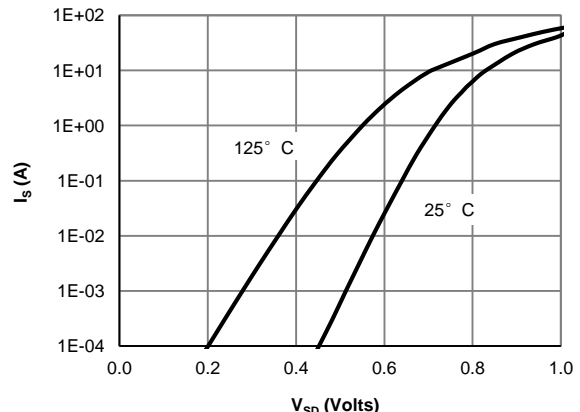


Figure 6: Body-Diode Characteristics

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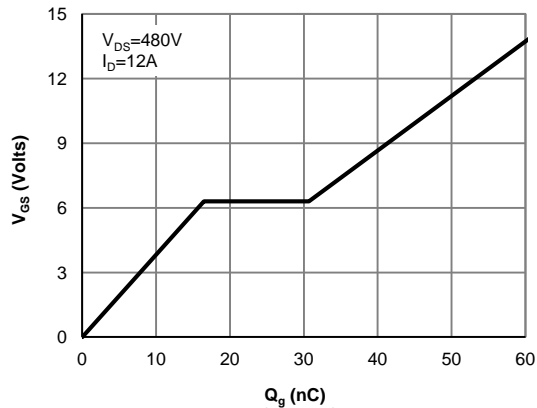


Figure 7: Gate-Charge Characteristics

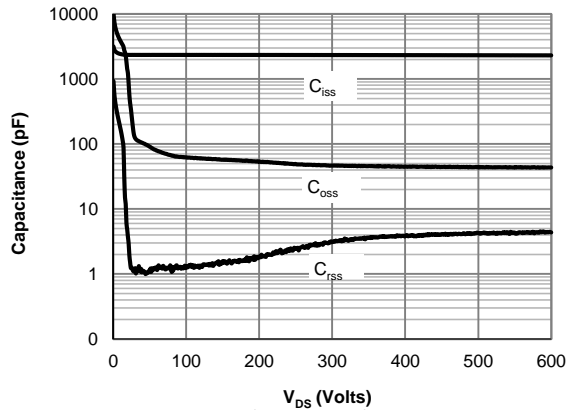


Figure 8: Capacitance Characteristics

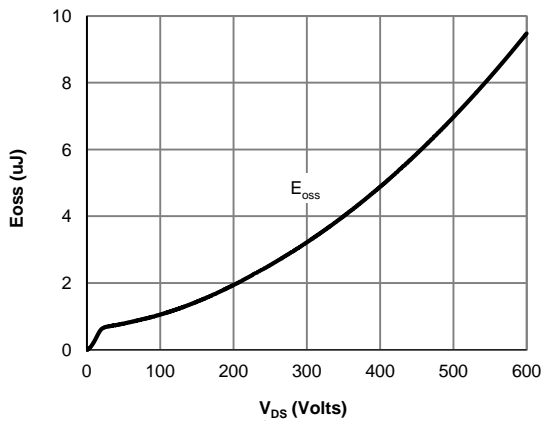


Figure 9: Coss stored Energy

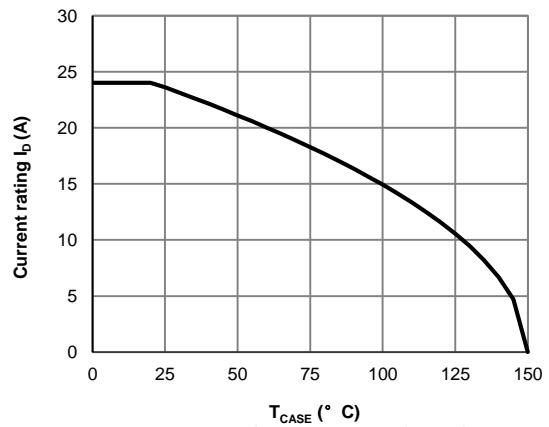


Figure 10: Current De-rating (Note F)

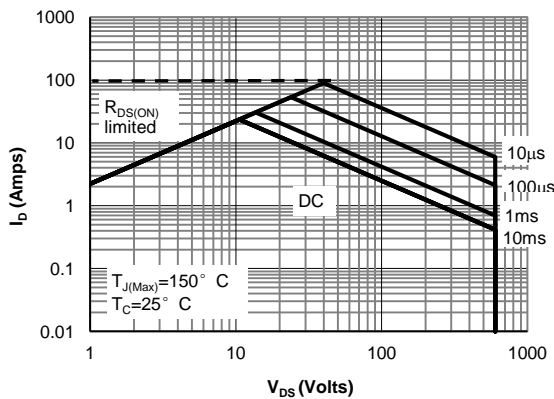


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

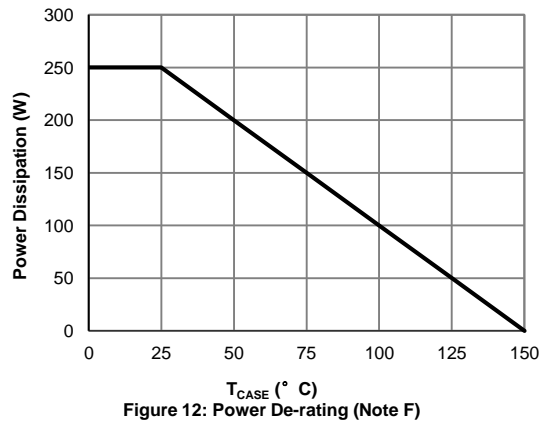


Figure 12: Power De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

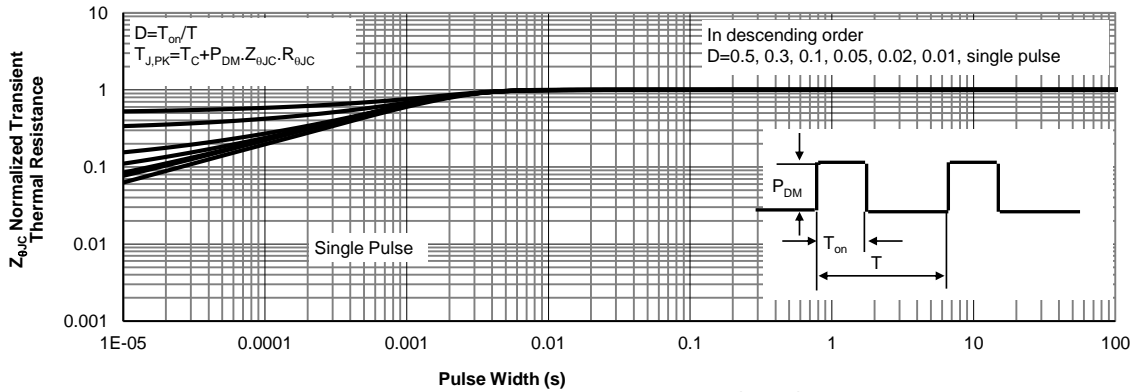


Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)

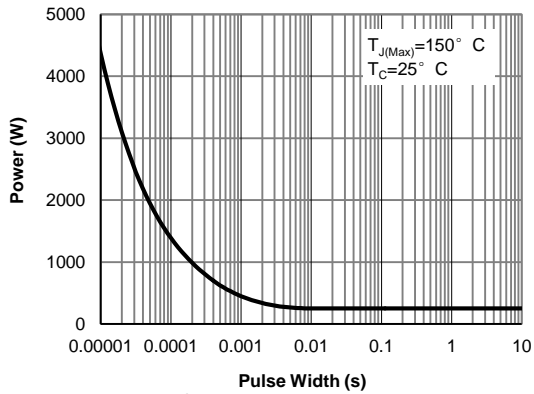


Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

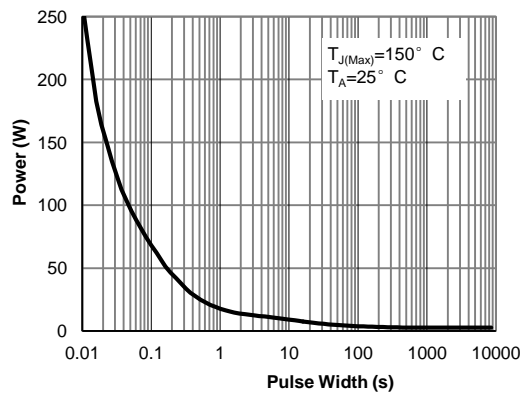


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

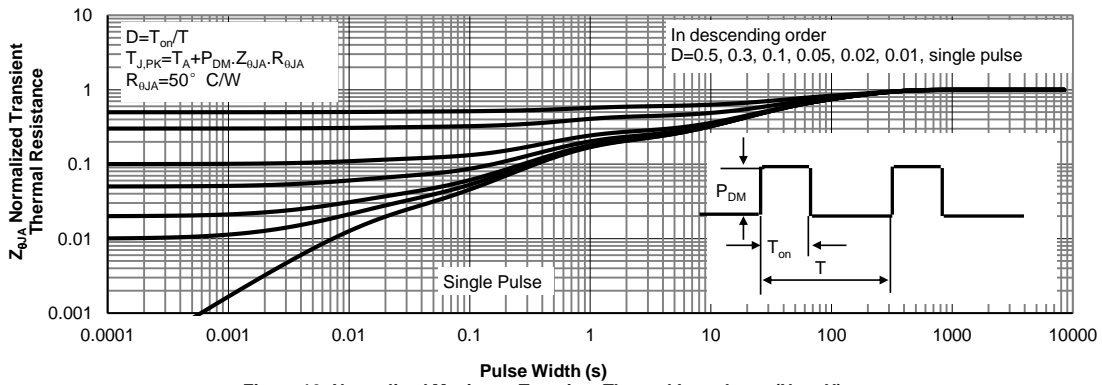
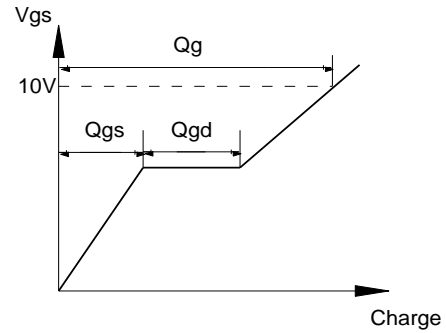
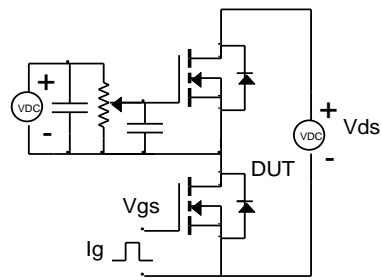
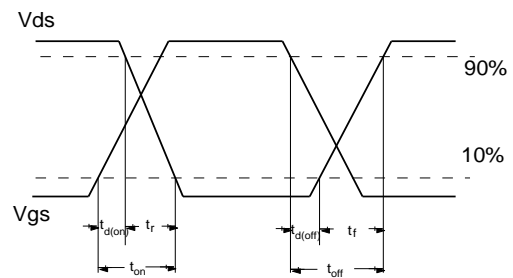
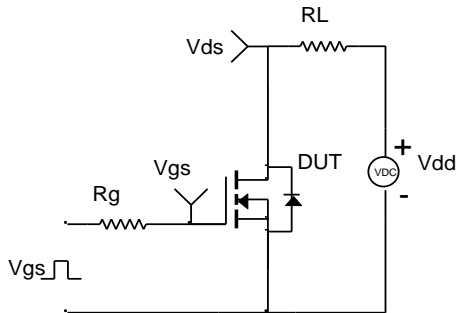


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

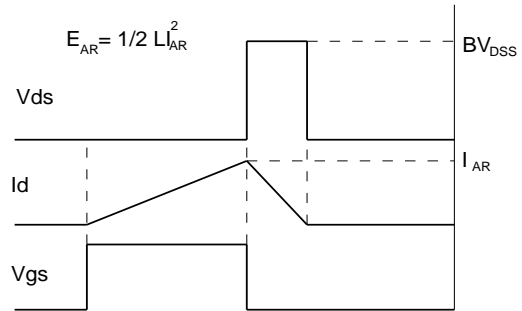
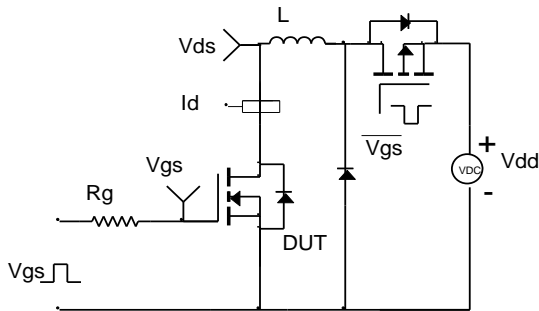
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

