

General Description

- Proprietary α MOS5™ technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

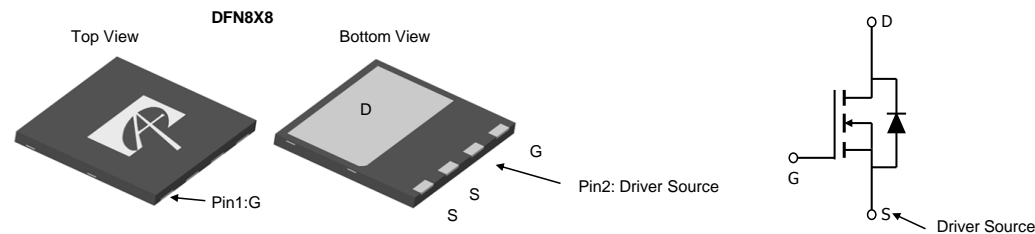
Applications

- SMPS with PFC, Flyback and LLC topologies
- Silver ATX, adapter, TV, lighting, Server power

Product Summary

V_{DS} @ $T_{j,max}$	700V
I_{DM}	44A
$R_{DS(ON),max}$	< 0.42 Ω
$Q_{g,typ}$	18nC
E_{oss} @ 400V	2.6 μ J

100% UIS Tested
 100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONV420A60	DFN8x8_4L_EP1_S	Tape & Reel	3500

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	V
Gate-Source Voltage (dynamic) AC($f > 1\text{Hz}$)	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	11
		$T_C=100^\circ\text{C}$	8
Pulsed Drain Current ^C	I_{DM}	44	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2.5
Avalanche Current ^C	I_{AR}	2.5	A
Repetitive avalanche energy ^C	E_{AR}	3.1	mJ
Single pulsed avalanche energy ^G ($T_J=25^\circ\text{C}$, $V_{GS}=10\text{V}$, $I_L=2\text{A}$, $L=105\text{mH}$, $R_{GS}=25\Omega$)	E_{AS}	210	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Diode reverse recovery	dv/dt	20	V/ns
$V_{DS}=0$ to 400V, $I_F \leq 10\text{A}$, $T_J=25^\circ\text{C}$	di/dt	100	A/us
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	139
		Derate above 25 $^\circ\text{C}$	1.1
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	8.3
		$T_A=70^\circ\text{C}$	5.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	12	15	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A,D}				
Maximum Junction-to-Case	$R_{\theta JC}$	0.62	0.9	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		700		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.52		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V			1	μA
		V _{DS} =480V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA		3.2		V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5.5A		0.38	0.42	Ω
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =5.5A		9.3		S
V _{SD}	Diode Forward Voltage	I _S =5.5A, V _{GS} =0V		0.85	1.2	V
I _S	Maximum Body-Diode Continuous Current				11	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C				44	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		955		pF
C _{oss}	Output Capacitance			29		pF
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		30		pF
C _{o(tr)}	Effective output capacitance, time related ^J			122		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		2.4		pF
R _g	Gate resistance	f=1MHz		4.8		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =5.5A		18		nC
Q _{gs}	Gate Source Charge			7		nC
Q _{gd}	Gate Drain Charge			4.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =400V, I _D =5.5A, R _G =5Ω		20		ns
t _r	Turn-On Rise Time			13		ns
t _{D(off)}	Turn-Off DelayTime			43		ns
t _f	Turn-Off Fall Time			16		ns
t _{rr}	Body Diode Reverse Recovery Time			251		ns
I _{rm}	Peak Reverse Recovery Current	I _F =5.5A, di/dt=100A/μs, V _{DS} =400V		19		A
Q _{rr}	Body Diode Reverse Recovery Charge			3.1		μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. This is the absolute maximum rating. Parts are 100% tested at T_J=25° C, L=60mH, I_{AS}=1A, V_{DD}=150V, R_G=25Ω.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

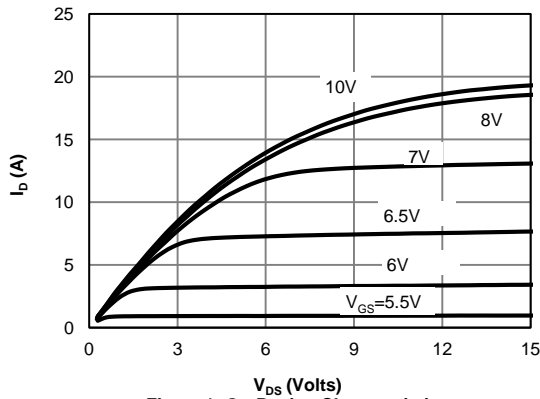


Figure 1: On-Region Characteristics

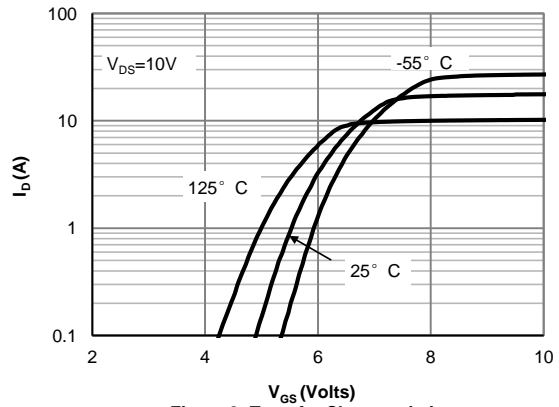


Figure 2: Transfer Characteristics

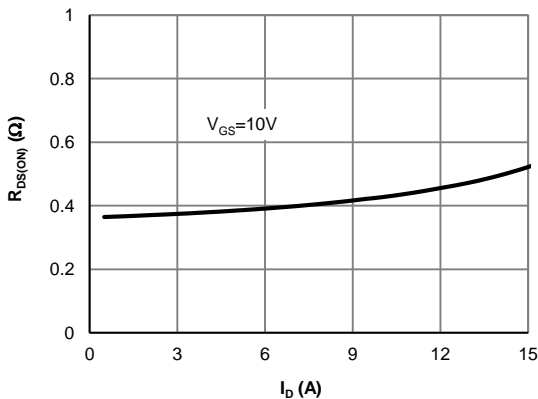


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

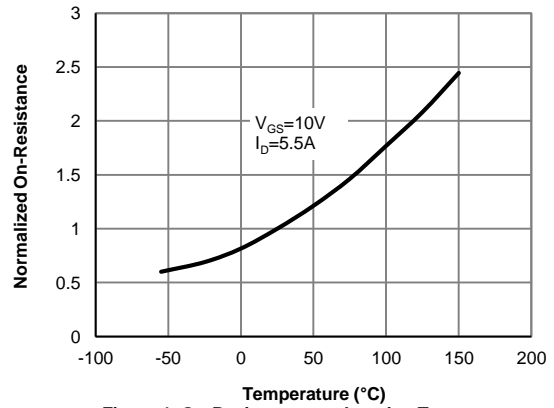


Figure 4: On-Resistance vs. Junction Temperature

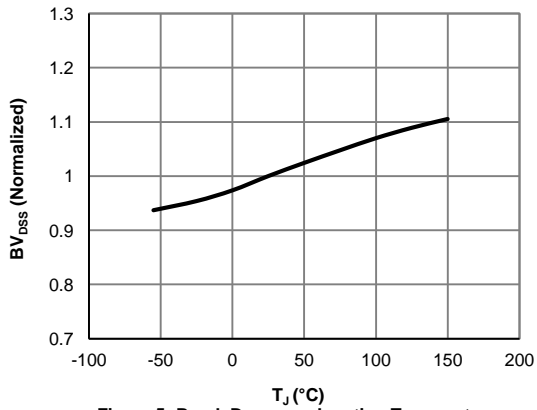


Figure 5: Break Down vs. Junction Temperature

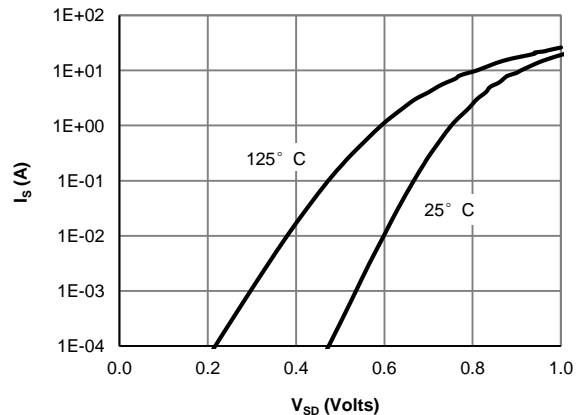


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

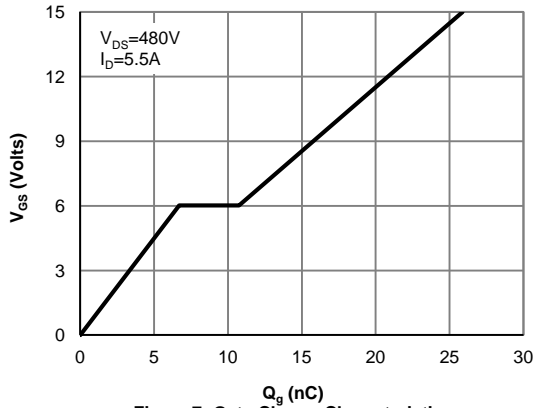


Figure 7: Gate-Charge Characteristics

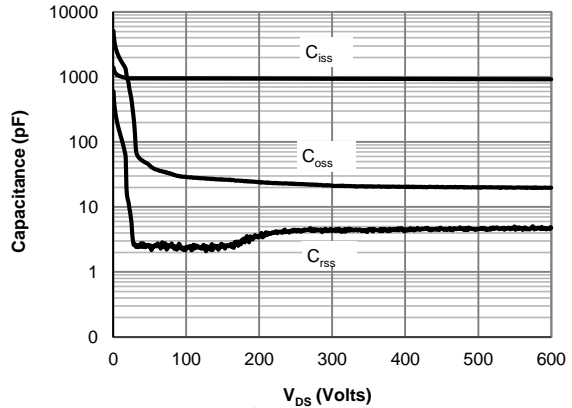


Figure 8: Capacitance Characteristics

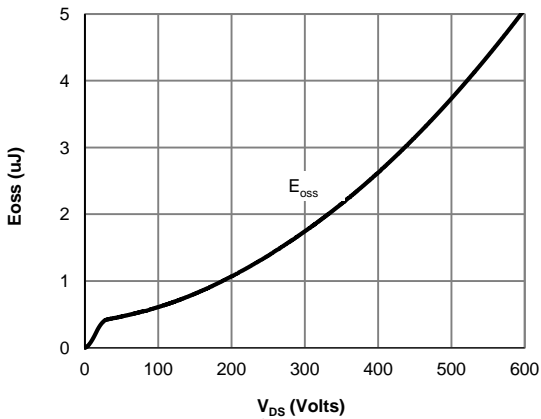


Figure 9: Coss stored Energy

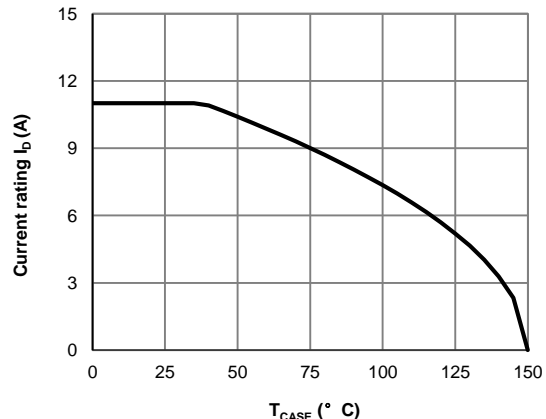


Figure 10: Current De-rating (Note F)

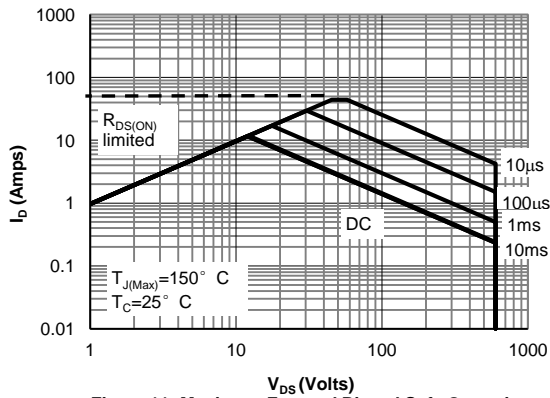


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

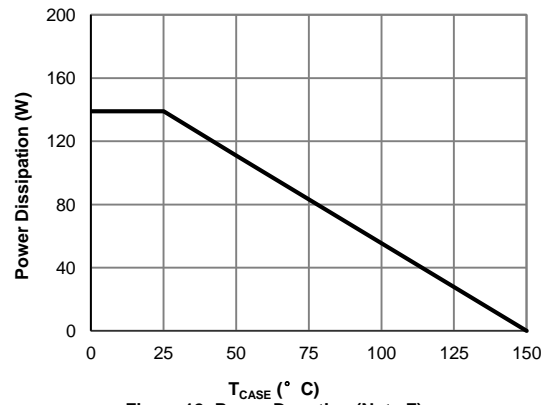


Figure 12: Power De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

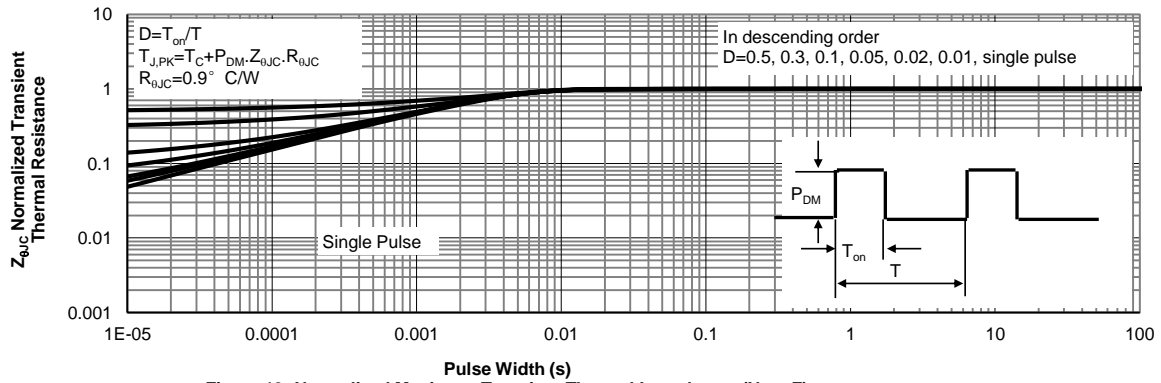


Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)

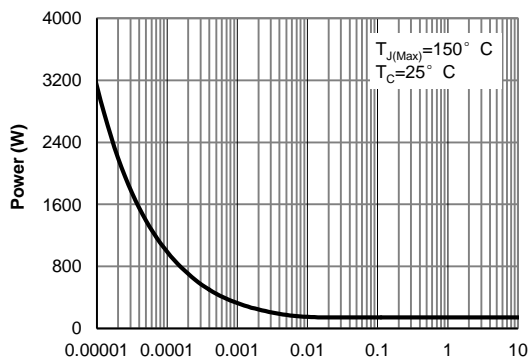


Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

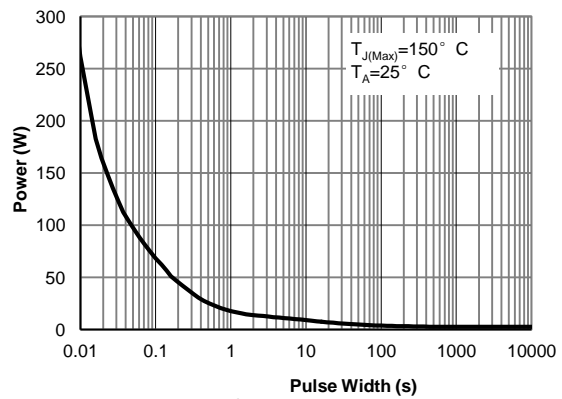


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

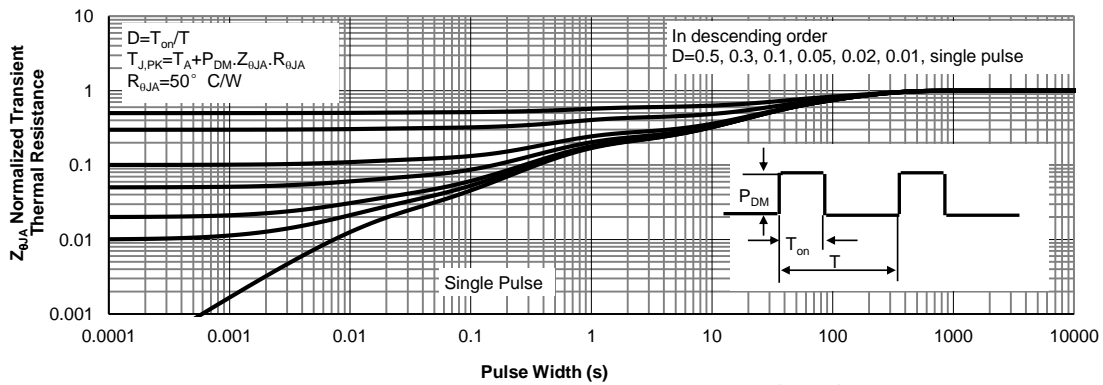
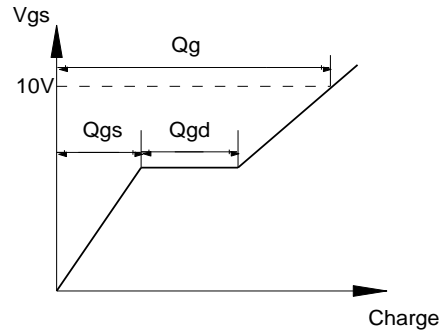
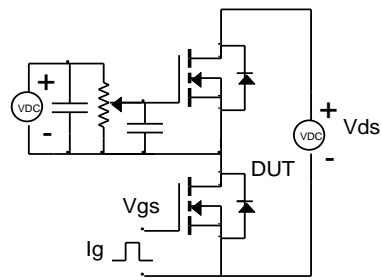
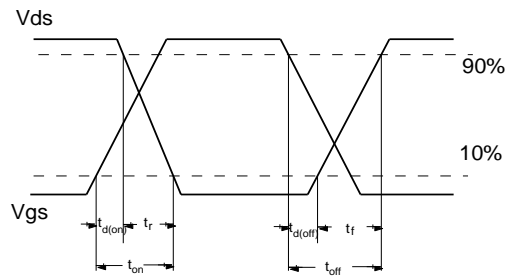
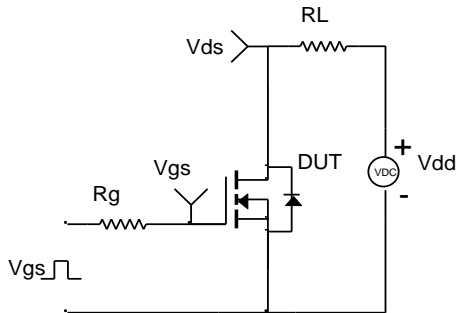


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

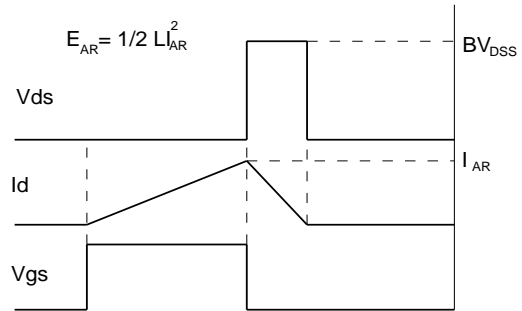
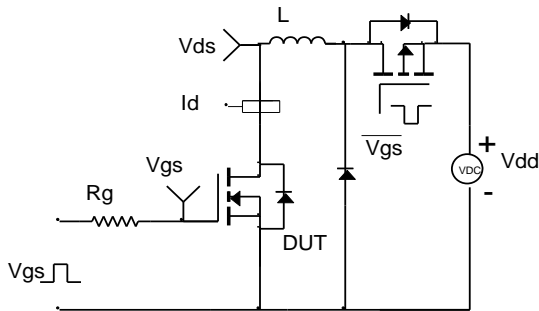
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

