

## DESCRIPTION

The SD6273 is a compact, high efficiency, fixed frequency pulse-width-modulation (PWM) controller. It provides an easy-to-use power supply solution for the application from one Li-ion battery to 5V output. All compensation and protection circuitry are integrated to minimize external components. The 1.2MHz high switching frequency allows smaller inductor and output capacitor, making the SD6273 ideally suited for small battery-powered applications and saves PCB space.

The SD6273 contains thermal shutdown function and output short protection circuit. Built-in soft-start circuitry prevents excessive inrush current during start-up.

The SD6273 is available in a Pb-free, thin-SOT23-5 and SOT23-6 packages.

## FEATURES

- $V_{DD}$  Range: 2.7V to 5.5V
- High Efficiency up to 90%
- 1.2MHz Fixed Switching Frequency
- Tiny External Components
- Output Short Protection
- $<1\mu\text{A}$  Shutdown Current
- 3.3V to +5.0V Distributed Power Supply
- Single Cell Li-ion Battery to 5V Converter
- Available in SOT23-5 and SOT23-6 Packages
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

## APPLICATIONS

- One Li-Ion Battery to 5V Output
- Handheld Devices

## Typical Application Circuit

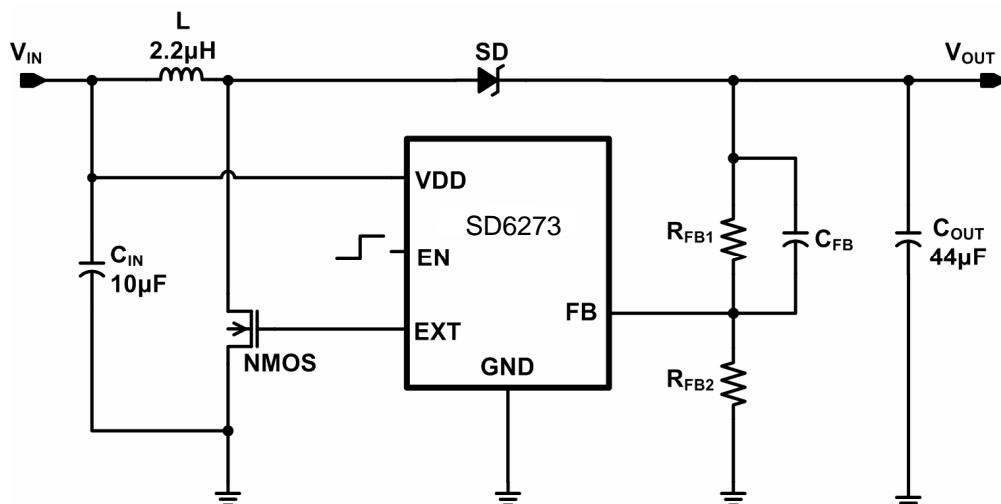


Figure 1. Connecting VDD to  $V_{IN}$

## Typical Application Circuit (Continued)

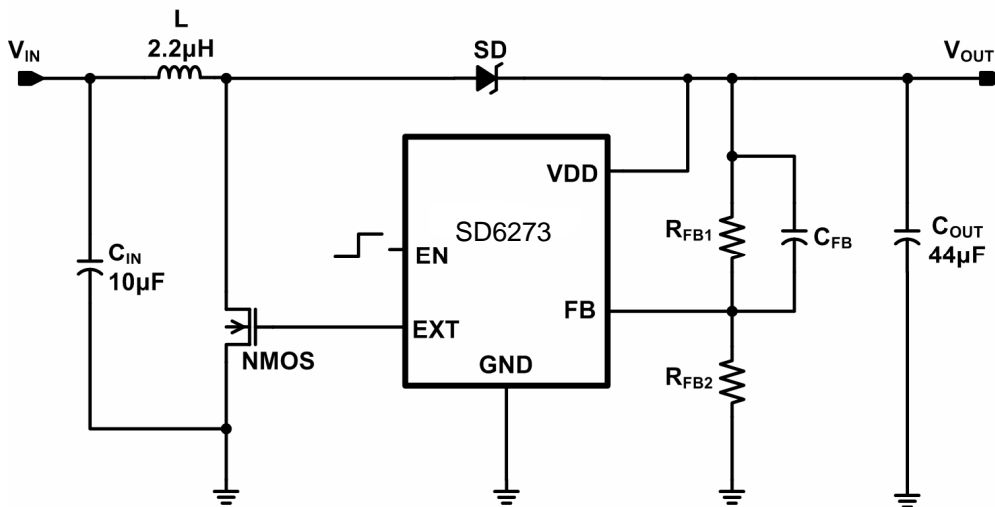


Figure 2. Connecting VDD to V<sub>OUT</sub>

## Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
SOT23-5	(TOP VIEW)	SOT23-6	(TOP VIEW)

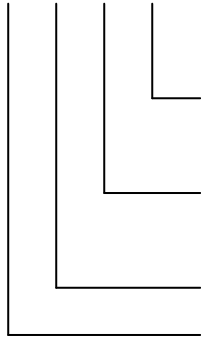
## Pin Description

PIN	SOT23-5	SOT23-6	DESCRIPTION
EN	1	4	Enable input. EN is an active high asserted input. Set EN lower than 0.4V will disable SD6273.
GND	2	5	Ground.
EXT	3	6	Output of MOSFET gate driver. Connect this pin to the gate of the external MOSFET.
VDD	4	1	Power input. Connect VDD to the input power supply or to the output of the regulator.
FB	5	3	Feedback pin.
NC	-	2	No connect.

## Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
SD6273VIR1	SOT23-5	xxxxx An00	-40 °C to 85°C
SD6273VAIR1	SOT23-6	xxxxx An00	-40 °C to 85°C

SD6273 □ □ □ □ □



Lead Free Code  
1: Lead Free, Halogen Free

Packing  
R: Tape & Reel

Operating temperature range  
I: Industry Standard

Package Type  
V : SOT23-5  
VA: SOT23-6

## Block Diagram

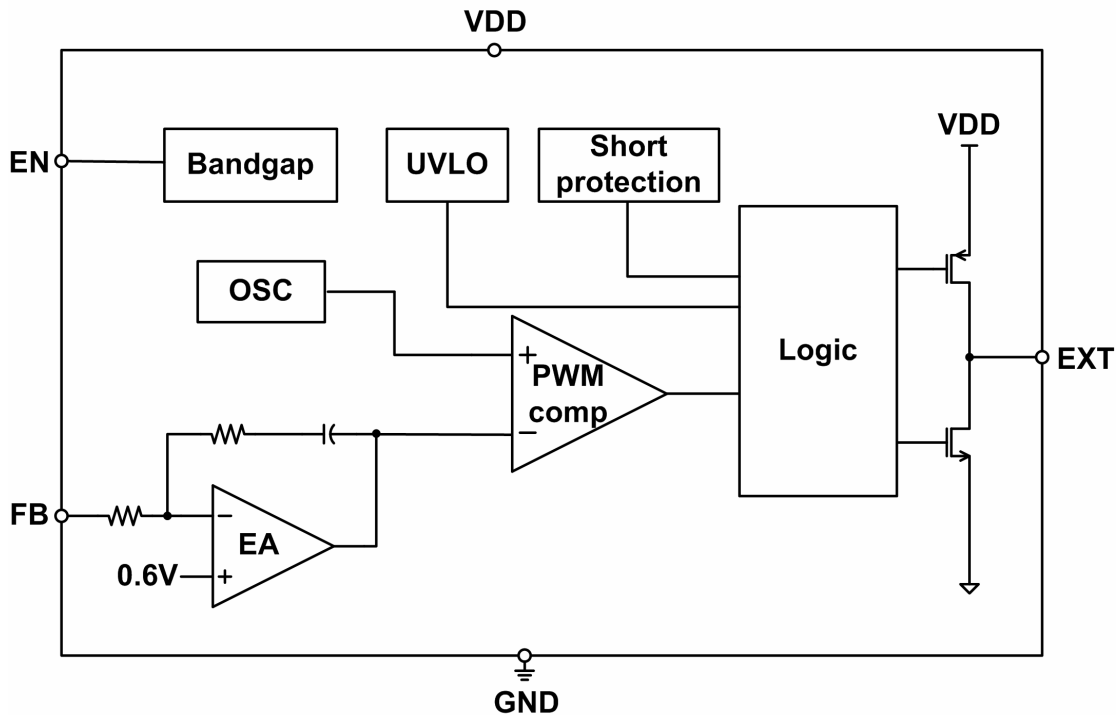


Figure 3.

## Absolute Maximum Ratings (1)

■	FB, EN to GND -----	-0.3V to 6V
■	Supply Voltage, $V_{DD}$ -----	-0.3V to 6V
■	Output of Gate Driver, $V_{EXT}$ -----	-0.3V to 6V
■	Power Dissipation, $P_D$ @ $T_A=25^\circ\text{C}$ SOT23-5, SOT23-6 -----	0.488W
■	Package Thermal Resistance SOT23-5, SOT23-6, $\theta_{JA}$ -----	205°C/W
■	Operating Temperature Range -----	-40°C to 85°C
■	Lead Temperature (Soldering, 10sec.) -----	260°C
■	Storage Temperature Range -----	-65°C to 150°C
■	ESD Susceptibility (HBM) -----	2kV

## Recommend Operating Conditions (2)

■	Junction Temperature Range -----	-40°C to 125°C
■	Supply Voltage, $V_{DD}$ -----	2.7V to 5.5V

Note (1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

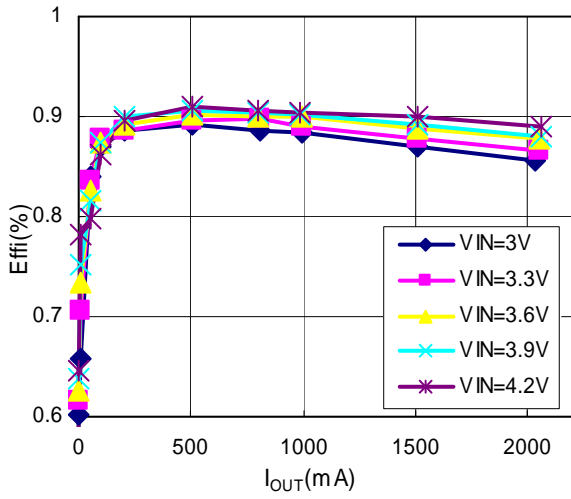
## Electrical Characteristics

$V_{DD}=3.6\text{V}$ ,  $T_A=25^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Conditions	SD6273			Unit
			Min.	Typ.	Max.	
<b>Power Supply</b>						
$V_{DD}$	Input Voltage Range		2.7		5.5	V
$I_Q$	Supply Current	$EN=V_{DD}=3.6\text{V}$		500	650	$\mu\text{A}$
$I_S$	$V_{DD}$ Shutdown Current	$V_{DD}=3.6\text{V}$ , $EN = \text{GND}$			1	$\mu\text{A}$
$V_{UVLO}$	Under-Voltage Lockout	Rising	2.2	2.35	2.5	V
$V_{UVLO\_HYS}$	Under-Voltage Lockout Hysteresis			80		mV
$F_{OSC}$	Switching Frequency	$T_A = 25^\circ\text{C}$	1.0	1.2	1.4	MHz
$V_{FB}$	Feedback Voltage		0.588	0.6	0.612	V
$I_{FB}$	FB Input/Output Current				0.2	$\mu\text{A}$
$D_{MAX}$	Maximum Duty Cycle		80	85	90	%
$I_{EXTH}$	High Side Output Current	$V_{EXT}=V_{DD}-0.4\text{V}$	150	200		mA
$I_{EXTL}$	Low Side Output Current	$V_{EXT}=0.4\text{V}$	200	300		mA
$T_{SD}$	Thermal Shutdown Threshold			150		$^\circ\text{C}$
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis			30		$^\circ\text{C}$
<b>EN Logic Control</b>						
$V_{EN(L)}$	EN, Input Low Threshold				0.4	V
$V_{EN(H)}$	EN, Input High Threshold		1.4			V
$I_{ENH}$	EN Input Current	$EN = 6\text{V}$		0.1		$\mu\text{A}$
$I_{ENL}$	EN Input Current	$EN = 0\text{V}$		0.1		$\mu\text{A}$

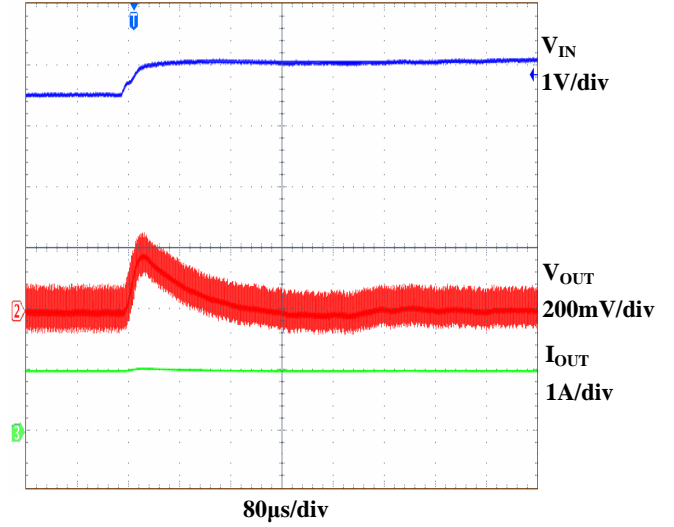
## Typical Operating Characteristics

### $I_{OUT}$ vs. Efficiency



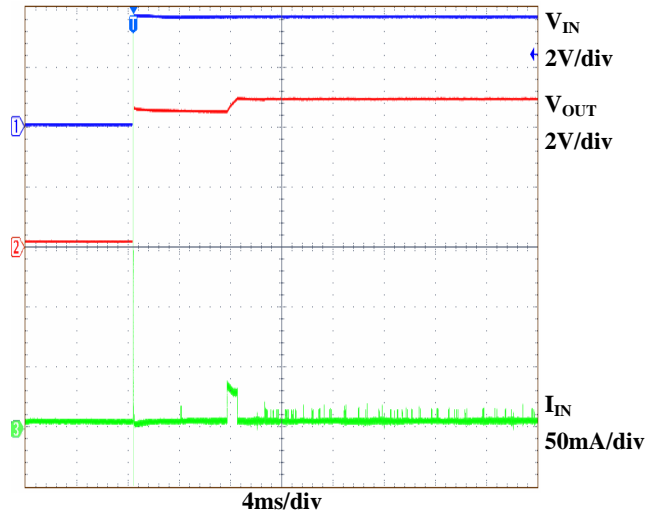
### Line Regulation

( $V_{IN}=3.6V \rightarrow 4.2V, V_{OUT}=5V, L=2.2\mu H, C_{OUT}=44\mu F, R_L=5\Omega$ )



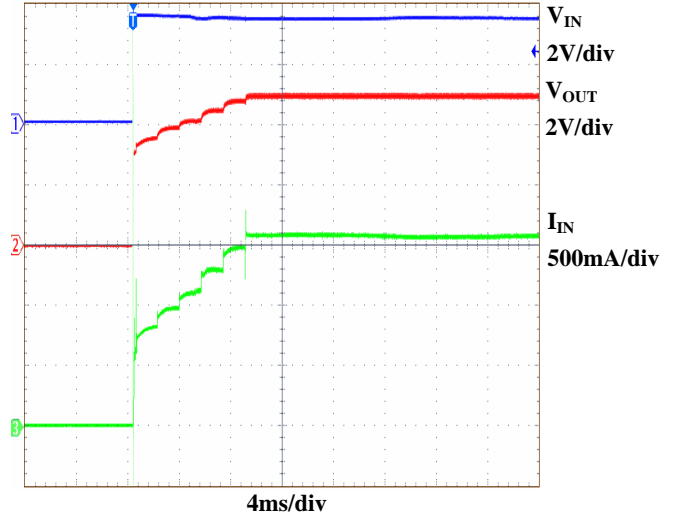
### Power On

( $V_{IN}=3.6V, V_{OUT}=5V, L=2.2\mu H, C_{OUT}=44\mu F, R_L=\infty$ )



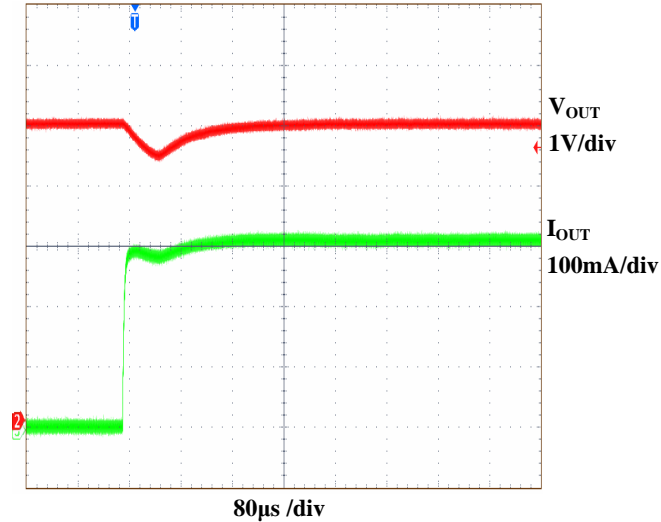
### Power On

( $V_{IN}=3.6V, V_{OUT}=5V, L=2.2\mu H, C_{OUT}=44\mu F, R_L=5\Omega$ )



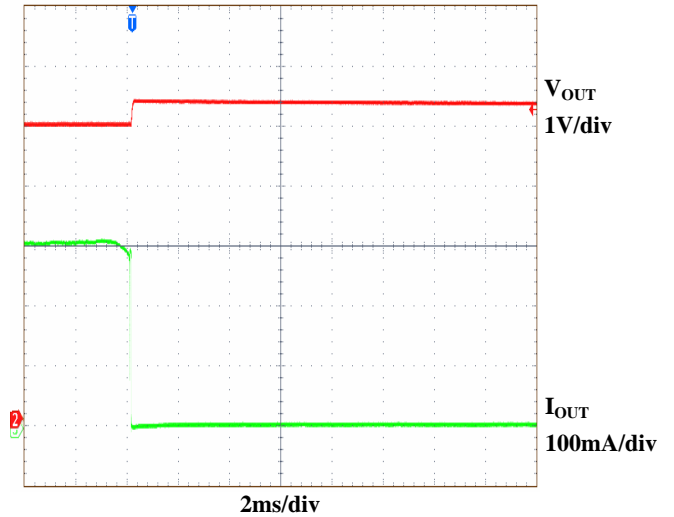
### Load Regulation 0 $\rightarrow$ 300mA

( $V_{IN}=3.6V, V_{OUT}=5V, L=2.2\mu H, C_{OUT}=44\mu F$ )



### Load Regulation 300 $\rightarrow$ 0mA

( $V_{IN}=3.6V, V_{OUT}=5V, L=2.2\mu H, C_{OUT}=44\mu F$ )



## Operation

The SD6273 is a switching regulator controller with pulse width modulation (PWM). In SD6273, pulses are skipped in light load to save energy.

The SD6273 uses a 1.2MHz fixed-frequency, voltage-mode regulation architecture to regulate the output voltage. It senses the output voltage through an external resistive voltage divider and compares that to the internal 0.6V reference to generate the error voltage, which is used to control the duty cycle and regulates the  $V_{OUT}$  to the set value.

When the SD6273 is disabled ( $EN = Low$ ), EXT will be pull down to turn off external NMOS. When enabled ( $EN = High$ ), SD6273 will operate in force PWM mode for regulating the output voltage to the target value.

The SD6273 is a step-up switching regulator controller. Figure 4. shows the basic circuit diagram. Step-up switching regulator starts the current supplied by the input voltage ( $V_{IN}$ ) when the NMOS is turned on and holds energy in the inductor at the same time. When the NMOS is turned off, the voltage of node SW is stepped up to discharge the energy held in the inductor and the current is discharged to  $V_{OUT}$  through the Shottky diode. Once the discharged current is stored in  $C_{OUT}$ , the potential of  $V_{OUT}$  increases until the voltage of the FB pin reaches the same potential as the internal reference voltage.

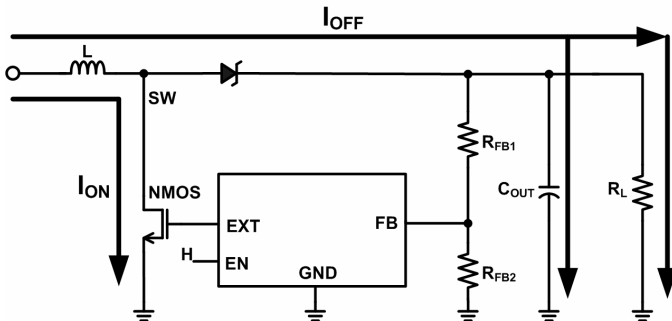


Figure 4.

For the PWM control method, the switching frequency ( $f_{sw}$ ) is fixed and the  $V_{OUT}$  voltage is held constant according to the ratio of the ON time and OFF time (ON duty) of NMOS in each period.

The ON duty in the current continuous mode can be calculated by using the equation below. Use the SD6273 in the range where the ON duty is less than the maximum duty. Note that the NMOS will be turned off when the voltage of FB pin is smaller than 0.2V.

## Soft-Start

The SD6273 includes a soft-start timer that steps up output voltage to prevent excessive current at the input. This will prevent premature termination of the source voltage at startup due to inrush current, and also force the input current to rise slowly to regulate the output voltage during soft-start.

## UVLO Function

The SD6273 has a UVLO (under voltage lock out) circuit for avoiding IC malfunctions due to power supply voltage drops. The SD6273 stops switching operation upon UVLO detection and retains the external transistor in the off state. Once entering the UVLO detection status, the soft-start function is reset.

## Application Information

### Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.6V feedback voltage. Use 110k $\Omega$  resistor for  $R_{FB1}$  of the voltage divider. Determine the low-side resistor  $R_{FB2}$  by the equation:

$$\frac{V_{OUT}}{V_{FB}} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

Where  $V_{OUT}$  is the output voltage; FB is the 0.6V feedback voltage. And when  $V_{OUT}$  is 5.0V,  $R_{FB2}$  is 15k $\Omega$ .

### Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. Multi-layer ceramic capacitors are the best choice as they have extremely low ESR and are available in small footprints. Use an input capacitor value of 10 $\mu$ F or greater. This capacitor must be placed physically close to the device.

### Selecting the Output Capacitor

A single 22 $\mu$ F ceramic capacitor usually provides sufficient output capacitance for most applications. Larger values up to 44 $\mu$ F may be used to obtain extremely low output voltage ripple and improve transient response. The impedance of the ceramic capacitor at the switching frequency is dominated by the capacitance, therefore the output voltage ripple is mostly independent of the ESR. The output voltage ripple  $V_{RIPPLE}$  is calculated as:

$$V_{RIPPLE} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{V_{OUT} \times C_{OUT} \times f_{SW}}$$

Where  $V_{IN}$  is the input voltage,  $I_{LOAD}$  is the load current,  $C_{OUT}$  is the output capacitor and  $f_{SW}$  is the 1.2MHz switching frequency.

### Selecting the Inductor

The inductor is required to force the output voltage higher while being driven by the lower input voltage. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30%-50% of the maximum input current. Calculate the required inductance value L using the equations:

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT} \times \Delta I \times f_{SW}}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

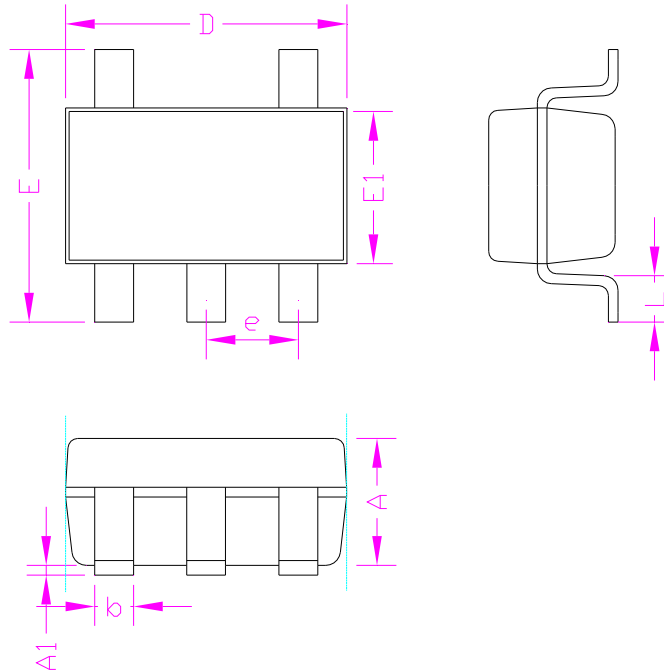
Where  $I_{LOAD(MAX)}$  is the maximum load current,  $\Delta I$  is the peak-to-peak inductor ripple current and  $\eta$  is efficiency. For the SD6273, typically  $2.2 \mu\text{H}$  is recommended for most applications. Choose an inductor that does not saturate at the peak switching current as calculated above with additional margin to cover heavy load transients and extreme startup conditions.

### Layout Considerations

High frequency switching regulators require very careful layout for stable operation and low noise. All components must be placed as close to the IC as possible. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace. The ground return of  $C_{IN}$  and  $C_{OUT}$  should be tied close to the GND pin. See the SD6273 demo board layout for reference.

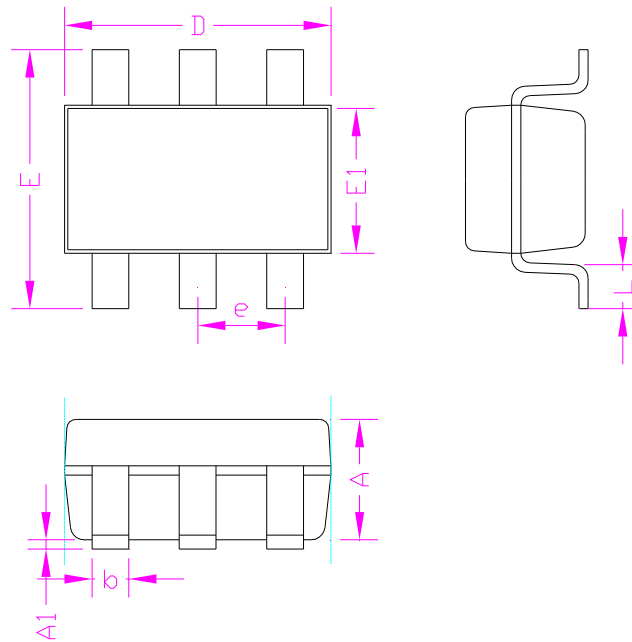
## Packaging Information

### SOT23-5



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	-	-	1.40	-	-	0.055
A1	0.00	-	0.15	0.000	-	0.006
D	2.65	2.90	3.15	0.104	0.114	0.124
E1	1.40	1.60	1.80	0.055	0.063	0.071
E	2.60	2.80	3.00	0.102	0.110	0.118
L	0.30	0.45	0.60	0.012	0.018	0.024
b	0.30	-	0.50	0.012	-	0.020
e	0.95 REF			0.037REF		

## SOT23-6



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	1.00	-	1.45	0.039	-	0.057
A1	0.00	-	0.15	0.000	-	0.006
b	0.30	-	0.50	0.012	-	0.020
D	2.70	2.90	3.10	0.106	0.114	0.122
E1	1.45	1.60	1.75	0.057	0.063	0.069
e	0.95 BSC			0.037 BSC		
E	2.60	2.80	3.00	0.102	0.110	0.118
L	0.30	-	0.60	0.012	-	0.024