Application Note: AN_SY6923D1

High Integrated 1-Cell Switching Charger With USB Compliance and USB-OTG Function

General Description

SY6923D1 is a high efficiency Buck mode switching charger for 1-cell Li-ion and Li-polymer battery. The SY6923D1 provides a high integrated solution for the portable device. It integrates the blocking FET, the power FETs, the input current sensing circuits and the charger controller. It is fully USB compliant to minimize the charging time when it is supplied from a USB port. SY6923D1 also support USB OTG with the integrated Boost regulator.

Three internal DACs are used as the reference of battery voltage and battery charge current and adapter input current limit, and programmed by host using I^2C. The adaptive input current limit allows the maximum charge current to minimize the charge time and keep the input supply from being overloaded.

The SY6923D1 is available in CSP1.93x2.05-20 package to allow small PCB footprint.

Ordering Information

SY6923 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6923D1PPC	CSP1.93x2.05-20	

Applications

- PADs
- Smart Phones
- Portable Equipment with Rechargeable Batteries
- Battery Back-up Systems

Features

- High Integrated and High Efficiency
- Up to 1.25A Charge Current (68mΩ R_{SENSE})
- Up to 1.55A Charge Current (55mΩ R_{SENSE})
- Up to 18V Absolute Maximum Input Voltage
- 6V Maximum Operating Input Voltage
- Adaptive Input Current Limit
- ±5% Input Current Limit Accuracy@500mA
- ±0.5% Charge Voltage Accuracy
- ±3.5% Charge Current Accuracy when I_{CHG} Higher than 550mA
- I^2C Controls(up to 3.4Mbps)
  - -- Battery Charge Voltage (3.5V – 4.44V)
  - -- Battery Charge Current (550mA – 1.25A)
  - -- Termination Current (50mA – 400mA)
  - -- Battery Weak Voltage (3.4V – 3.7V)
  - -- Input Current Limit
  - -- VBUS Threshold for Adaptive Input Current
  - -- Low Charge Current Mode Enable and Disable
  - -- Termination Enable and Disable
- Integrated Loop Compensation
- Internal Soft-start
- Bad adapter Detection and Rejection
- 3MHz Frequency PWM
- Automatic High Impedance Mode for Low Power Consumption
- 5V, Boost Mode for USB OTG
- CSP1.93x2.05-20 Package
- Spread Spectrum Frequency Control for Improved EMI Performance
- Factory Test-Mode for GSM Calibration Without a Battery

Typical Applications

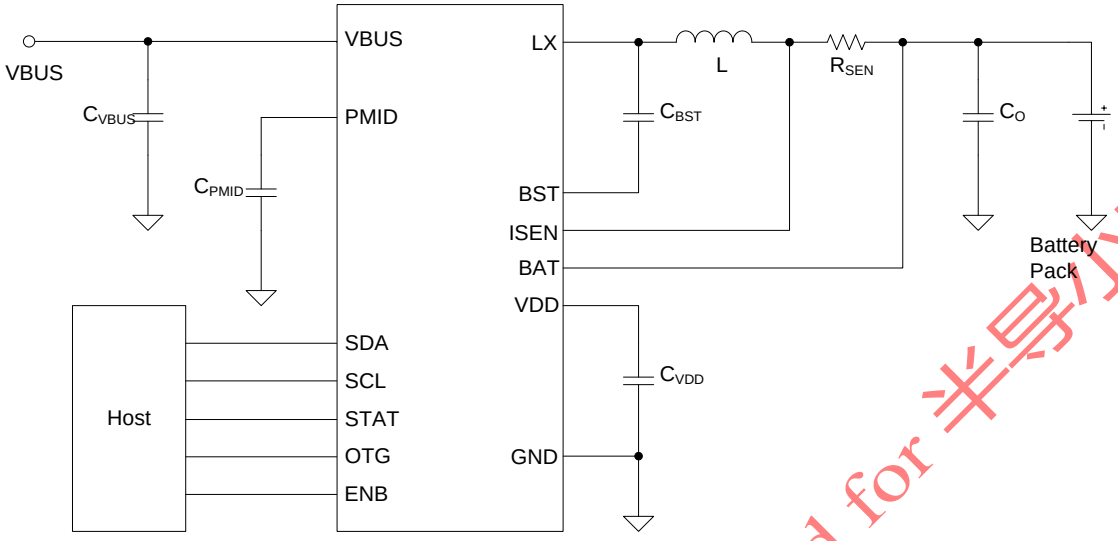
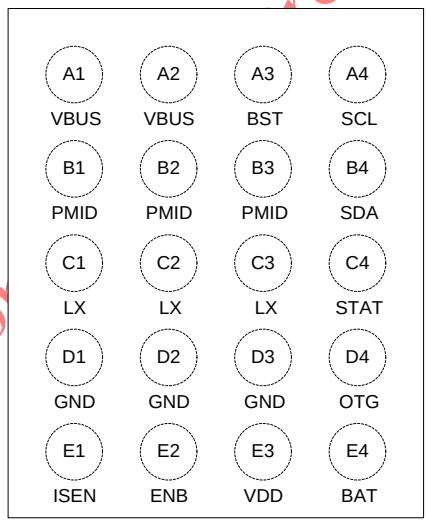


Figure1. SY6923D1 Schematic Diagram

Pinout (top view)



(CSP1.93x2.05-20)

Top Mark: BOT*xyz* (device code: **BOT**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin NO.	Pin Description
VBUS	A1,A2	Charger input voltage.
BST	A3	High side power MOSFET driver power supply.
SCL	A4	I^2C clock input. Connect an external pull-up resistor according to I^2C specification.
PMID	B1,B2,B3	Buck converter input point. Bypass it with a minimum of 4.7μF ceramic capacitor to GND.

SDA	B4	I^2C data I/O. Open-drain output. Connect an external pull-up resistor according to I^2C specification.
LX	C1,C2,C3	Switching node.
STAT	C4	Open drain output for charge status indicator. Pull low during charging.
GND	D1,D2,D3	Ground pins.
OTG	D4	Enable boost regulator with OTG_Enable and OTG_Level_Select bits. During faults, a 128μs pulse is sent out. On VBUS POR, this pin sets the input current limit in default mode.
ISEN	E1	Battery charging current sense positive input.
ENB	E2	Charge enable pin. Active low enables the charger.
VDD	E3	LDO output for converter power MOSFETs driver. Connect a 1μF ceramic capacitor at least to GND.
BAT	E4	Battery charging current sense negative input and battery voltage sense input.

Absolute Maximum Ratings (Note 1)

VBUS, PMID, STAT, SCL, SDA, OTG, ENB, ISEN, BAT ---------- -0.3V to 18V
LX ---------- -2V to 18V
VDD, BST-LX ---------- -0.3V to 3.6V
ISEN-BAT ---------- -0.5V to 0.5V
Package Thermal Resistance (Notes 2)
CSP1.93x2.05, θ_{JA} ---------- 85 ℃/W
Junction Temperature Range ---------- -40 ℃ to 150 ℃
Storage Temperature ---------- -65 ℃ to 150 ℃
Lead Temperature (Soldering, 10s) ---------- 260 ℃

Recommended Operating Conditions (Note 3)

VBUS, PMID, STAT, SCL, SDA, OTG, ENB, ISEN, BAT, LX ---------- -0.3V to 6V
VDD, BST-LX ---------- -0.3V to 3.3V
ISEN-BAT ---------- -0.5V to 0.5V
Junction Temperature Range ---------- -40 ℃ to 125 ℃
Ambient Temperature Range ---------- -40 ℃ to 85 ℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a low effective four layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{VBUS} = 5V, ENB=0, R_{SENSE}=68mΩ, T_J=25℃, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charge Operating Conditions						
VBUS Input Voltage Range	V_{VBUS}		4		6	V
VBUS Under Voltage Lockout	V_{VBUSUV}	VBUS rising edge	3.05	3.3	3.55	V
VBUS Under Voltage Lockout Hysteresis	V_{VBUSUV_HYS}	VBUS falling edge		150		mV
Input Over Voltage	V_{INOV}	VBUS rising edge		6.5		V
Input Over Voltage Hysteresis	V_{INOV_HYS}	VBUS falling edge		170		mV
VBUS Supply Current Control	I_{VBUS}	V_{VBUS} = 5V, PWM not switching			1.5	mA
Charge Regulation Range and Accuracy						
Charge Voltage Regulation Range	V_{BAT_REG}	BAT voltage	3.5		4.44	V
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	T_A=25℃	-0.5		0.5	%
Charge Current Regulation Range	I_{CHG_REG}	V_{ISEN} –V_{BAT}, 68mΩ sense resistor	550		1250	mA
		V_{ISEN} –V_{BAT},55mΩ sense resistor	608		1550	mA
Low Charge Current	I_{CC_LOW}	V_{SHORT}≤V_{BAT}≤V_{CV}, Low_Charge=1		325	350	mA
Charge Current Reference Voltage	V_{CHG}	Low_Charge=0, I_{CHG}_Reference=000	36.8		39.4	mV
		Low_Charge=0, I_{CHG}_Reference=011	57.2		60.5	mV
Battery Voltage Drop for Recharge Threshold	V_{RCH}	V_{RCH} =V_{CV_REG}-V_{BAT}	90	120	150	mV
Recharge Deglitch Time	t_{RCH}	V_{BAT} falls below threshold		130		ms
Input Current Limit Accuracy	I_{IN_LIM}	USB 100mA	83		97	mA
		USB 500mA	450	475	500	mA
VBUS Range for Adaptive Input Current Limit	V_{IIN_LIM}		4.2		4.76	V
VBUS Voltage Regulation Accuracy	$V_{IIN\_LIM\_ACC}$	Adaptive_IIN_Threshold=100	4.4		4.58	V
Charge Termination						
Termination Charge Current Range	I_{TERM}	V_{BAT}>V_{RCH}, V_{BUS}-V_{BAT}>V_{ASD}	50		400	mA
Deglitch Time for Charge Termination	t_{TERM}			30		ms
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM}=100mA	-15		15	%
		I_{TERM}=250mA	-10		10	%

Weak Battery Detection						
Weak Battery Voltage Threshold Range	V_{LOWV}		3.4		3.7	V
Weak Battery Voltage Accuracy	V_{LOWV_ACC}		-5		5	%
Weak Battery Voltage Hysteresis	V_{LOWV_HYS}	Battery voltage falling edge		100		mV
Input Source Qualification						
Poor Input Source Voltage	V_{INUV}	VBUS falling edge	3.6	3.8	4.0	V
Poor Input Source Voltage Hysteresis	V_{INUV_HYS}	VBUS rising edge		200		mV
Current Source to GND for Input Source Qualification	I_{IN_QUA}	During input source qualification		30		mA
Qualification Interval	t_{IN_QUA}	During input source qualification		2		s
Battery Detection						
Battery Detection Current Before Charge Done	I_{BAT_DET}	Begins after termination detected		-0.5		mA
Battery Detection Time	t_{BAT_DET}			260		ms
Auto Shutdown						
Auto Shutdown Threshold	V_{ASD}	V_{VBUS}-V_{BAT} falling edge	0	80	100	mV
Exit Auto Shutdown Threshold	V_{ASD_EXIT}	V_{VBUS}-V_{BAT} rising edge	120	200	280	mV
VDD						
Internal Bias LDO Output	V_{VDD}	I_{VREF}=1mA, C_{VREF}=1μF		3.3		V
VDD Short Circuit Current Limit	I_{VDD}			100		mA
PWM Converter						
Blocking FET $R_{DS(ON)}$	$R_{ON(BLKFET)}$			180	250	mΩ
High Side FET $R_{DS(ON)}$	$R_{ON(HSFET)}$			120	250	mΩ
Low Side FET $R_{DS(ON)}$	$R_{ON(LSFET)}$			110	210	mΩ
Swtching Frequency	f_{SW}			3.0		MHz
Charge Mode Protection						
Battery OVP	V_{BAT_OVP}	VBAT rising edge	110	117	121	%
Battery OVP Hysteresis	$V_{BAT\_OVP\_HYS}$	VBAT falling edge		11		%
Cycle-by-cycle Current Limit	I_{LIM}			2.7		A
Battery Short Threshold	V_{SHORT}	VBAT falling edge	1.85	1.95	2.05	V
Battery Short Hysteresis	V_{SHORT_HYS}	VBAT rising edge		100		mV
Short Mode Charge Current	I_{SHORT}	V_{BAT}<V_{SHORT}		30		mA
Boost Regulation and Accuracy						
OTG Output on VBUS	V_{VBUS_OTG}		4.90	5.05	5.20	V
Maximum OTG Output Current	I_{VBUS_OTG}	V_{VBUS_OTG}=5.05V	350			mA

Cycle-by-cycle Current Limit	I_{OTG_LIM}	V_{VBUS_OTG}=5.05V, 3V<V_{BAT}<4.5V		1		A
OTG Output OVP	V_{OTG_OVP}	VBUS rising edge	5.60	5.75	5.90	V
OTG Output OVP Hysteresis	$V_{OTG\_OVP\_HYS}$	VBUS falling edge		160		mV
Battery Voltage Input OVP	V_{BAT_OVP}	VBAT rising edge	4.75	4.9	5.05	V
Battery Voltage Input OVP Hysteresis	$V_{BAT\_OVP\_HYS}$	VBAT falling edge		200		mV
Battery Voltage Input UVP	V_{BAT_UVP}	VBAT rising edge		2.9	3.05	V
Battery Voltage Input UVP Hysteresis	V_{BAT_UVP}	VBAT falling edge		400		mV
Boost Output Resistance at HI-Z Mode		ENB=1 or HZ_Mode=1	300			kΩ
Thermal Regulation and Thermal Shutdown						
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising edge		155		℃
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}	Junction temperature falling edge		20		℃
Thermal Regulation Threshold	T_{REG}			120		℃
STAT Output						
Low Level Output Voltage		Sink 10mA current			0.55	V
Leakage Current		5V on STAT pin			1	μA
Logic Level and Timing						
ENB, OTG,SCL,SDA Low Level Threshold	V_{LOW}				0.4	V
ENB, OTG,SCL,SDA High Level Threshold	V_{HIGH}		1.2			V
I^2C Operating Frequency	f_{SCL}				3.4	MHz

Function Description

SY6923D1 includes multiple functions necessary to charge 1-cell Li-Ion and Li-polymer battery pack. A high efficiency 3MHz NMOS-NMOS synchronous Buck is integrated to control the charge voltage from 3.5V to 4.44V and charging current up to 1.55A. The SY6923D1 also has input current limit to avoid the USB crash. The input current limit, charge current limit, and charge voltage limit are set by internal registers written with I^2C. The SY6923D1 also support OTG function, which can support the power to USB port by internal Boost regulator.

SY6923D1 has three operation modes:

1. Charge mode.
2. Boost mode: Provide 5V power to USB by internal boost regulator with battery input.
3. High-impedance mode: Both the boost and charger are turned off in this mode. The charger enters a low quiescent current state to save power.

VBUS Detection

The adapter or USB can be connected as SY6923D1 input. VBUS is the source input pin and is used as the input voltage sensing.

When VBUS is higher than the UV threshold, the input source will be qualified by a 30mA current source.

SY6923D1 will start charging if the input is qualified ok.

If the VBUS drops below 3.8V, the IC disables the current source and set Bad source fault flag in 00H register.

Auto Shutdown

The IC will auto shutdown and enter low-power mode if the VBUS falls below the auto-shutdown threshold and above the UV threshold. During auto-shutdown, VDD, the blocking FET and PWM are turned off.

Input Current Limit

The input current limit can be programmed by 01H register, sensed by build-in current sensing circuits. When input current is higher than programmed value, IC will reduce the charge current automatically.

Battery Voltage, Battery Current, and Adapter Input Voltage Regulation

The battery voltage regulation is set by 02H register, programmed by the host microcontroller through the I^2C interface.

The battery current regulation is set by 04H register. It is sensed by a resistor connected between the ISEN and BAT pins. For a 68mΩ sense resistor, the maximum current is 1.25A. For a 55mΩ sense resistor, the maximum current is 1.55A.

The charge voltage and current can't be programmed higher than the safety limit values in 06H.

The input voltage regulation is set by 05H register, sensed by build-in voltage sensing circuits. When VBUS is lower than Adaptive_IIN_Threshold (default 4.52V), IC will reduce the charge current automatically.

Battery Detection

SY6923D1 can detect battery, once termination, the IC enables a discharge current, I_{BAT_DET}, for a period of t_{BAT_DET} (262ms), then checks the battery voltage. If the battery voltage is below the recharge threshold after t_{BAT_DET},the battery is absent, the IC will set no battery fault flag in 00H register and reset charge parameters registers.

The battery detection is used to ensure that some charge parameters are reset whenever the battery is replaced.

USB Friendly Power Up

If the battery voltage is above the BAT_Weak threshold while in default mode, the charger will be in the high impedance state. The default control bits set the charging current and regulation voltage low as a safety feature to avoid violating USB spec and over-charging any of the Li-Ion chemistries, while the host has lost communication. When operating in default mode, the OTG pin logic level sets the input current limit to 100mA for logic low and 500mA for logic high. In host mode, the input current limit is set by register 01H.

Charge Mode Operation

Once a good battery with voltage below the recharge threshold has been inserted and a good adapter is attached, the IC enters charge mode. In charge mode, the IC has five control loops to regulate input voltage, input current, charge current, charge voltage and device junction temperature. During the charging process, all five loops are enabled and the one that is dominant takes control. The IC supports a precision Li-ion or Li-polymer charging system for single-cell applications.

During the normal charging process with host control, once the voltage at the BAT pin is above the battery recharge threshold for the 30ms deglitch period, and the charge current is below the ITERM threshold, the

termination is detected, the IC turns off the PWM charge and enables battery detection.

The termination current level is programmable. To disable the charge current termination, the host can set the charge termination bit (Termination_Enable) of charge control register to 0.

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the recharge threshold.
- VBUS Power-on reset (POR), if battery voltage is below the weak battery threshold.
- ENB bit toggle or RESET bit is set (Host controlled).

Battery Protection in Charge mode

Battery over voltage protection protects the device, the battery and the system components from damage if the battery voltage goes too high, especially when the battery is removed suddenly. When OVP is detected, IC turns off the PWM and set flag fault bits. The charger recoveries when the fault condition is removed.

When the battery voltage is lower than V_{SHORT}, the IC turns off the PWM, VBAT is charged by a 30mA current.

Boost Mode Operation

In host mode, when OTG pin is high (and OTG_Enable bit is high thereby enabling OTG functionality) or the operation mode bit (OPA_MODE) is set to 1, IC operates in boost mode and delivers the power to VBUS from the battery. In normal boost mode, IC converts the battery voltage to V_{BUS_OTG} (about 5.05V) and delivers a current as much as I_{BUS_OTG} to support other USB OTG devices connected to the USB connector.

Different from charge mode operation, in boost mode, the IC provides an integrated, fixed 3 MHz frequency controller to regulate the output voltage at PMID pin (V_{PMID}). In boost mode, the blocking FET prevents battery discharge when VBUS pin is over loaded.

To prevent the inductor saturation and limit the inrush current, a soft-start control is applied during the boost start up.

Protection in Boost Mode

The IC provides a built-in over-voltage protection to protect the device and other components against damage if the VBUS voltage goes too high. When an over-voltage condition is detected, the IC turns off the PWM converter, resets OPA_MODE bit to 0, sets fault status bits, and sends out a fault pulse from the STAT pin. Once VBUS drops to the normal level, the boost starts after host sets OPA_MODE to "1" or OTG pin stays in active status.

The IC provides a built-in over-load protection to prevent the device and battery from damage when VBUS is over loaded. Once the over load condition is detected, Q1 operates in linear mode to limit the output current. If this condition lasts for more than 30ms, the over-load fault is detected. When an over-load fault is detected, the IC turns off the PWM converter, resets OPA_MODE bit to 0, sets fault status bits and sends out fault pulse in STAT pin.

In boost mode, when the battery voltage is above the battery over voltage threshold, V_{BATMAX}, or below the minimum battery voltage threshold, V_{BATMIN}, the IC turns off the PWM converter, resets OPA_MODE bit to 0, sets fault status bits and sends out fault pulse in STAT pin. Once the battery voltage goes above V_{BATMIN}, and below V_{BATMAX}, the boost will start after the host sets OPA_MODE to "1" or OTG pin stays in active status.

PFM

IC will automatic decreases the switching frequency at light load condition to achieve high efficiency.

Spread Spectrum

The spread spectrum mode can only be enabled in charge mode. The purpose of the spread spectrum clock modulation is to reduce EMI in charge mode. In charge mode, the switching frequency is not fixed to 3MHZ, but shifted by +/-10% in 1ms, the energy of the switching converter's EMI is distributed over a wider range of frequencies thereby lowering the magnitude of EMI at 3 MHZ +/-10% as well as harmonic frequencies.

Factory Test Mode

The factory mode can be enabled only in charge mode, whether the battery is present or not. This can be set through I^2C Reg05 bit6. Setting the factory mode bit enables the following changes:

- Output current limit is disabled, while Idpm still works unless disabled by host.
- Cycle-by-cycle peak current limit threshold in charge mode is doubled

HIGH IMPEDANCE (Hi-Z) MODE

Taking the ENB pin high causes the charger to enter Hi-Z mode.

When in default mode and the ENB pin is low, the charger automatically enters Hi-Z mode if

1. VBUS > UVLO and a battery with VBAT > V_{LOWV} is inserted
2. Or VBUS falls below UVLO.

When in host mode and the ENB is low, the charger can be placed into Hi-Z mode if the HZ-Mode control bit is set to “1” and OTG pin is not in active status.

In order to exit Hi-Z mode, the ENB pin must be low, VBUS must be higher than UVLO and the host must write a "0" to the HZ-Mode control bit.

Thermal Shutdown Protection (TSD)

When the junction temperature exceeds 155ºC,thermal shut down is detected, PWM is turned off. Charging recovers when Tj falls below 135 ˚C.

Status Output

The STAT pin is used to indicate operation status. STAT is pulled low during charging when STAT_Enable bit in control register (00H) is set to “1”. Under other conditions, STAT pin behaves as a high impedance (open-drain) output. Under fault conditions, a 128-µs pulse will be sent out to notify the host. The status of STAT pin at different operation conditions is summarized in below table. The STAT pin can be used to drive an LED or communicate to the host processor.

Charge Status	**STAT**
Charge in progress and STAT_Enable=1	Low
Other normal conditions	Open-drain
Charge mode faults: Auto shutdown, VBUS or battery overvoltage, poor input source, VBUS UVLO, no battery, thermal shutdown	128µs pulse, then open-drain
Boost mode faults: Over load, VBUS or battery overvoltage, low battery voltage, thermal shutdown	128µs pulse, then open-drain

I²C Interface

SY6923D1 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The SY6923D1 operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbits), fast mode (up to 400kbits),and high speed mode (up to 3.4Mbps in write mode).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

F/S Mode Protocol

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transfer.

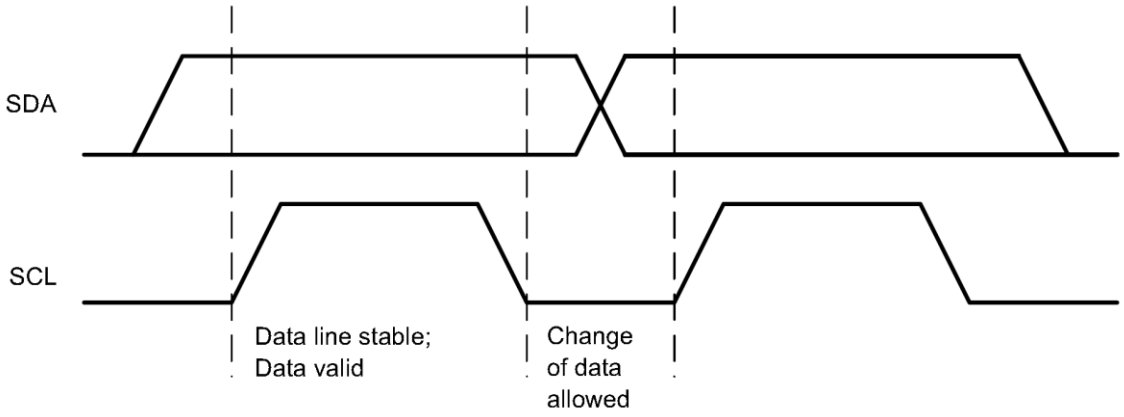


Figure 2. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

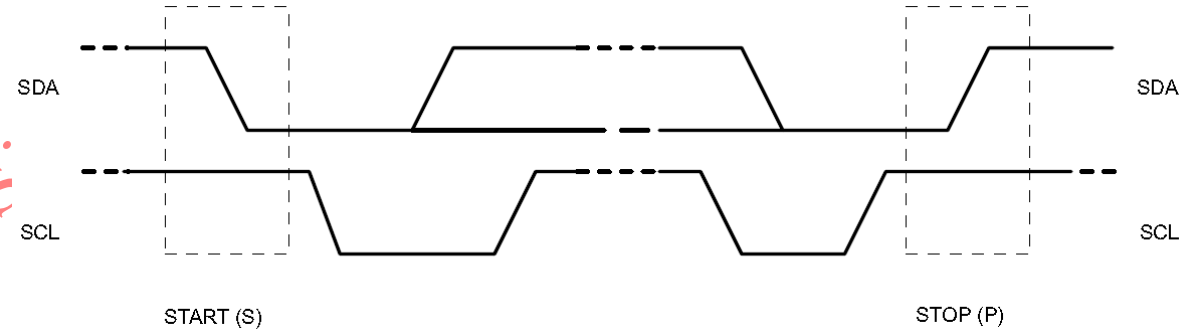


Figure 3. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first.

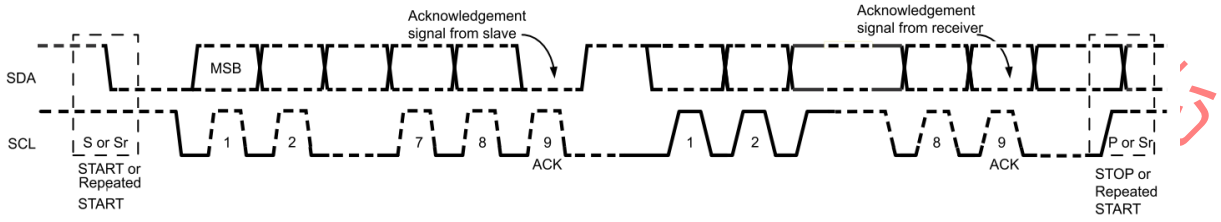


Figure 4. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

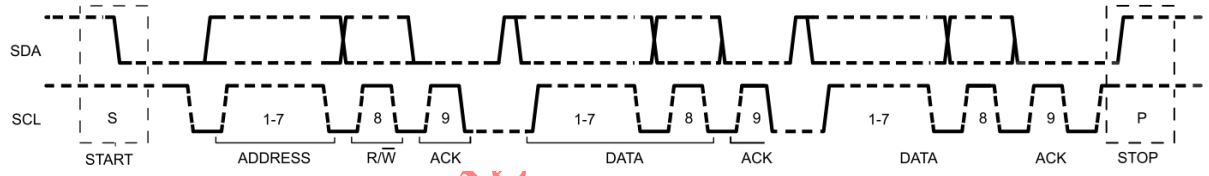


Figure 5. Complete Data Transfer

H/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition(a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I²C logic from getting stuck in a bad state.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

I²C Update Sequence

The IC requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the IC acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the IC. The IC performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

For the first update, the IC requires a start condition, a valid I²C address, a register address byte, and a data byte. For all consecutive updates, the IC needs a register address byte, and a data byte. Once a stop condition is received, the IC release the I²C bus, and awaits a new start conditions.

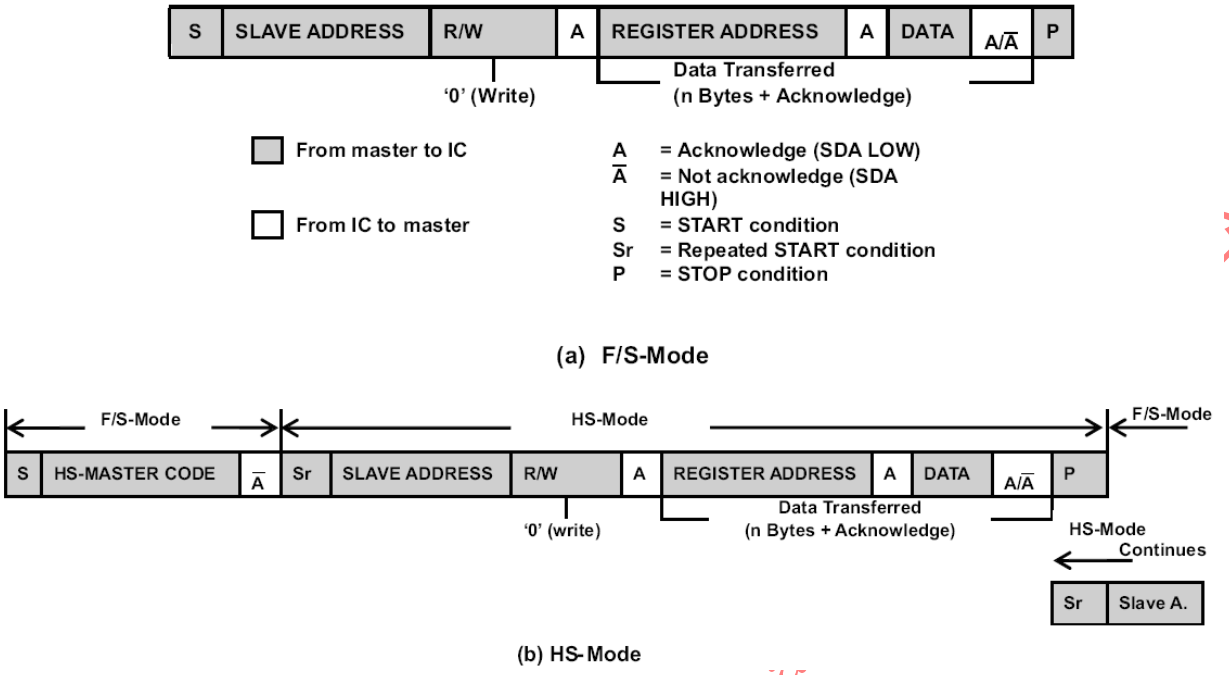


Figure 6. Bus Protocol

Register Description

Battery Charger Registers

The SY6923D1 supports seven battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. 03H are “read only” registers and can be used to identify the SY6923D1.

Table 1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	x1xx 0xxx
01H	Control Register	Read or Write	0011 0000
02H	Control/Battery Voltage Register	Read or Write	0000 1010
03H	Vendor/Part Number/Rev Register	Read only	0101 0xxx
04H	Constant/Termination Charge Current Register	Read or Write	0000 0001
05H	Adaptive IIN Threshold /ENB pin status Register	Read or Write	001x x100
06H	Safety Limit Register	Read or Write	0100 0000

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	OTG	R	OTG status, 0: OTG pin is low, 1: OTG pin is high
6	STAT_Enable	R/W	0: Disable STAT pin function 1: Enable STAT pin function (default)
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	Boost	R	1: In boost mode 0: Not in boost mode
2:0	Fault	R	Charge mode 000: Normal, 001: VBUS OVP, 010: Auto Shutdown, 011: Bad Input Source or VBUS<VUVLO, 100: Output OVP, 101: Thermal shutdown, 110: NA, 111: No battery Boost mode 000: Normal, 001: VBUS OVP, 010: Over load, 011: Battery voltage is too low, 100: Battery OVP, 101: Thermal shutdown, 110: NA, 111: NA

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7:6	IIN_Limit	R/W	00: USB input with 100mA current limit (default) 01: USB input with 500mA current limit 10: USB input or Adapter with 800mA current limit 11: No input current limit
5:4	BAT_Weak	R/W	00: 3.4V battery weak threshold 01: 3.5V battery weak threshold 10: 3.6V battery weak threshold 11: 3.7V battery weak threshold (default)
3	Termination_Enable	R/w	0: Disable charge current termination (default) 1: Enable charge current termination
2	Charge_Disable	R/W	0: Enable charger (default) 1: Disable charger
1	HZ_Mode	R/W	0: Not high impedance mode (default) 1: High impedance mode
0	OPA_Mode	R/W	0: Charger mode (default) 1: Boost mode

Table 4. Control/Battery Voltage Register (02H)

Bit	Bit Name	R/W	Description
7:2	Charge_Voltage	R/W	000000: 3.50V charge voltage (step is 20mV) 000001: 3.52V charge voltage 000010: 3.54V charge voltage (default) 000011: 3.56V charge voltage …… 101111: 4.44V charge voltage …… 111111: 4.44V charge voltage
1	OTG_Level_Select	R/W	0: OTG pin active low 1: OTG pin active high (default) Not applicable to OTG pin control of current limit at POR in host mode.
0	OTG_Enable	R/W	0: Disable OTG (default) 1: Enable OTG Not applicable to OTG pin control of current limit at POR in host mode.

Table 5. Vendor/PN/Rev Register (03H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	010: Identify Silergy as the supplied
4:3	PN	R	10: SY6923D1
2:0	Revision	R	001: Revision 0.0 010-111: Future Revisions……

Table 6. Constant/Termination Charge Current Register (04H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	W: write 1 to reset some charge parameters.
6:4	ICHG_Reference	R/W	000: 37.4mV for charge current regulation (default) (step is 6.8mV) 001: 44.2mV for charge current regulation 010: 51.0mV for charge current regulation …… 111: 85mV for charge current regulation
3	NA	R/W	Not used, 1 default
2:0	ITERM_Reference	R/W	000: 3.4mV for termination current (step is 3.4mV) 001: 6.8mV for termination current (default) 010: 10.2mV for termination current …… 111: 27.2mV for termination current

Table 7. Adaptive Iin Threshold/ENB pin status Register (05H)

Bit	Bit Name	R/W	Description
7	NA	R/W	Not used, 0 default
6	FAC_MODE	R/W	0:Disable factory test mode(default) 1:Enable factory test mode
5	Low_Charge	R/W	0: Normal charge current reference at 04H. 1: 22.1mV low charge current reference (default)
4	Adaptive_IIN_Limit	R	0: Adaptive current limit or input current limit is not active 1: Adaptive current limit or input current limit is active
3	ENB_Status	R	0: ENB Pin is low 1: ENB Pin is high
2:0	Adaptive_IIN_Threshold	R/W	000: 4.20V special charge voltage 001: 4.28V special charge voltage …… 100: 4.52V special charge voltage (default) …… 111: 4.76V special charge voltage

Table 8. Safety Limit Register (06H)

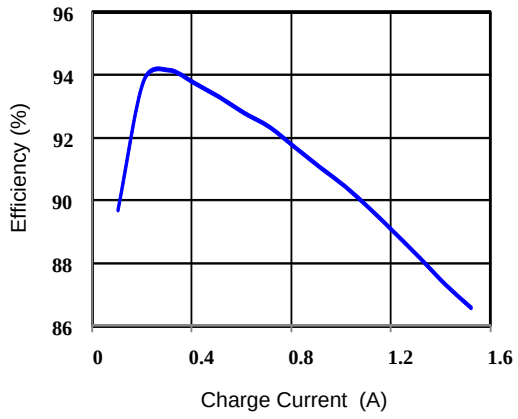
Bit	Bit Name	R/W	Description
7:4	MAX_Charge_Current	R/W	0000: 37.4mV for max charge current reference (step is 6.8mV) 0001: 44.2mV for max charge current reference …… 0100: 64.6mV for max charge current reference (default) …… 1010: 105.4mV for max charge current reference …… 1111: 105.4mV for max charge current reference
3:0	MAX_Charge_Voltage	R/W	0000: 4.20V maximum charge voltage (default) (step is 20mV) 0001: 4.22V maximum charge voltage …… 1100: 4.44V maximum charge voltage …… 1111: 4.44V maximum charge voltage

The Safety Limit Register is reset when V_{BAT} drops below V_{SHORT}. After reset, the limit values can be programmed, and any writing to other register locks the safety limits. The values in 02H (charge voltage) and in 04H (charge current) higher than the safety limit will be ignored.

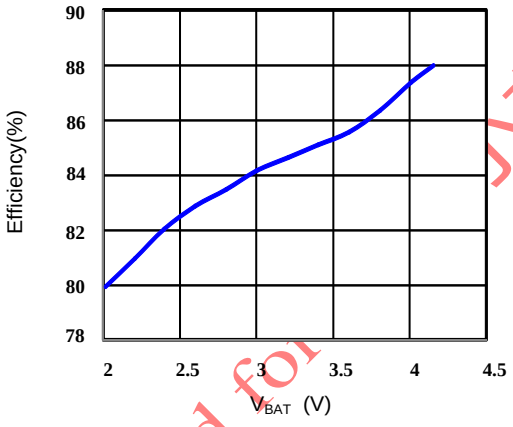
Typical Performance Characteristics

T_A=25℃, V_{IN}=5V, R_{SEN}=55mΩ, 1cell battery, unless otherwise specified.

Efficiency vs. Charge Current (CV mode)

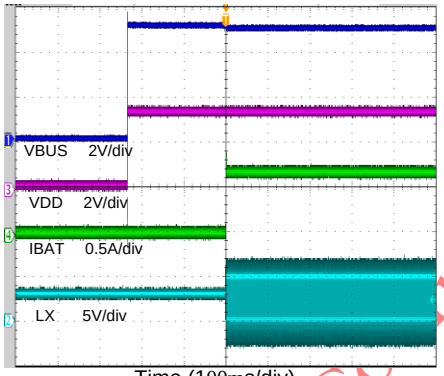


Efficiency vs. Charge Voltage (CC mode)



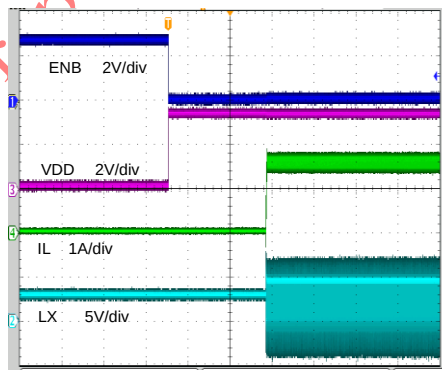
Power On

（VBUS=5V VBAT=3.4V host Mode）



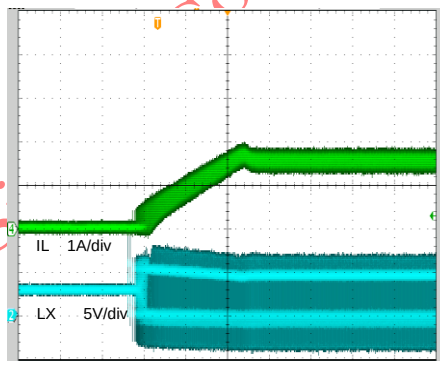
ENB On

（VBUS=5V VBAT=3.4V host Mode）



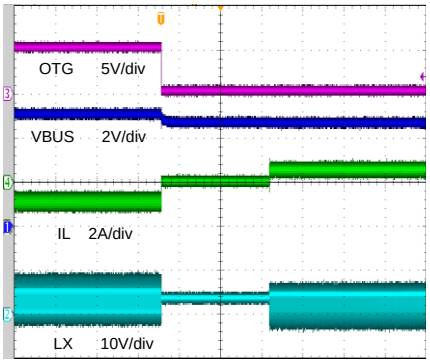
Charger Soft Start

（VBUS=5V VBAT=3.4V ICHG=1.55A host Mode）



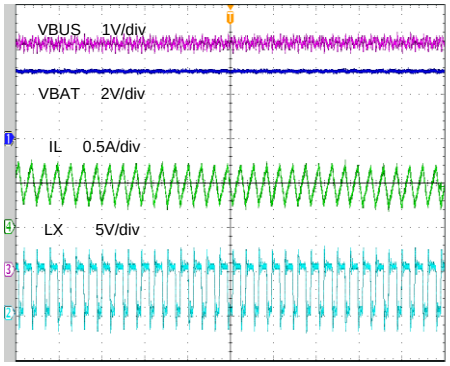
Boost To Charge Mode Transition

（VBUS connects 4.5V power supply, VBAT=3.6V OTG Control）



Constant Current Charge State

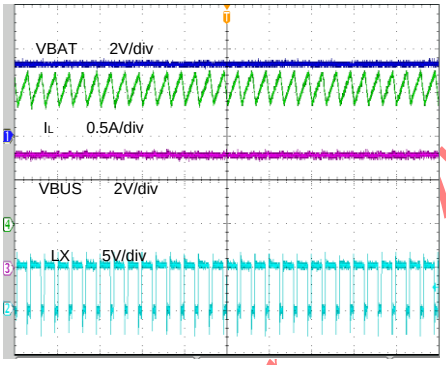
（VBUS=5V VBAT=3.2V Low charge 402mA）



Time (1μs/div)

Constant Current Charge State

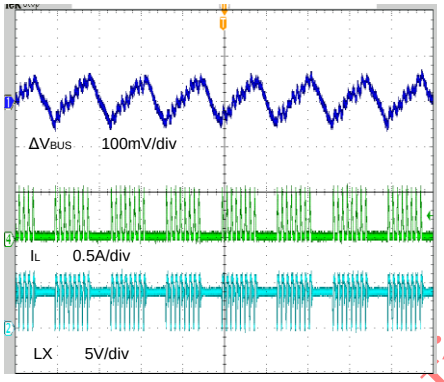
(VBUS=5V VBAT=3.2V ICHG=1.55A)



Time (1μs/div)

Boost Mode Light Load State

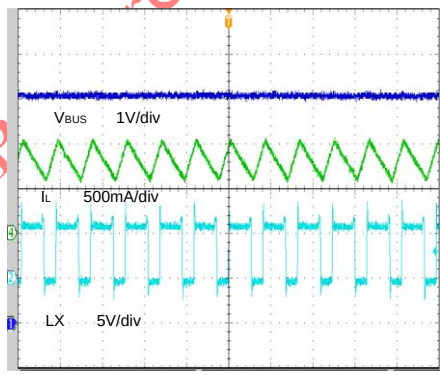
(VBAT=3.6V IBUS=0.05A)



Time (10μs/div)

Boost Mode Full Load State

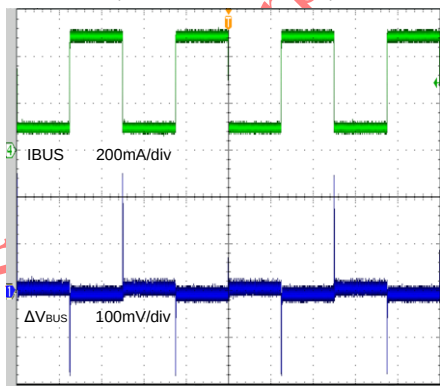
(VBAT=3.6V IBUS=0.5A)



Time (0.4μs/div)

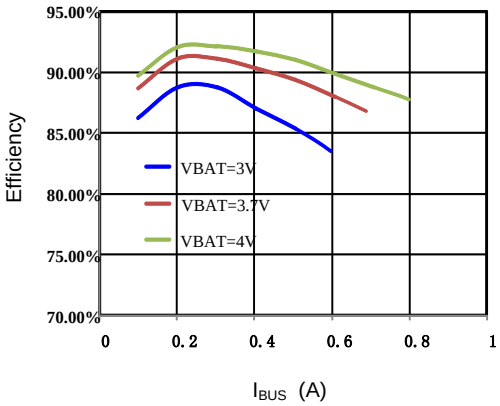
Boost Mode Load transient

(VBAT=3.6V IBUS=0.1A~0.5A)



Time (4ms/div)

Efficiency vs. Load current (Boost mode)



Applications Information

The following battery charger design refers to the "Schematic Diagram" (see Figure 1.). This section describes how to select the external components including the inductor, input and output capacitors, and sense resister.

Charging current sense resistor R_{SEN}

Both the termination current and the charge current depend on the sense resister R_{SEN}. The reference voltage range for termination current is 3.4mV to 27.2 mV, the reference voltage range for charge current is 37.4mV to 85mV.
The termination current is calculated as below:

$$I_{TERM} = \frac{V_{TERM}}{R_{SENSE}} \qquad \text{Unit: m}\Omega$$

While the V_{TERM} is set by register04, Bit [2:0].
The charge current is calculated as below:

$$I_{CHG} = \frac{V_{CHG}}{R_{SENSE}} \qquad \text{Unit: m}\Omega$$

While the V_{CHG} is set by register04, Bit [6:4] .
For example, RSEN=55mohm:

The constant current is

REG04[6:4]	V_{CHG}/mV	I_{CHG}/mA
000	37.4	680
001	44.2	804
010	51	927
011	57.8	1051
100	64.6	1175
101	71.4	1298
110	78.2	1422
111	85	1545

The termination current is

REG04[2:0]	V_{TERM}/mV	Iterm/mA
000	3.4	62
001	6.8	124
010	10.2	185
011	13.6	247
100	17	309
101	20.4	371
110	23.8	433
111	27.2	495

Inductor Selection

Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{CHG} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle ($D = V_{BAT}/V_{BUS}$), switching frequency (f_{SW}) and inductance (L):

$$I_{Ripple} = \frac{V_{VBUS} \times D \times (1-D)}{f_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used to absorb the high frequency switching ripple current and smooth the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow.

$$I_{RMS} = \frac{V_{VBUS}}{\sqrt{12} \times L \times f_{SW}} \times D \times (1-D)$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is typical operation for the battery charger.
A typical 20µF ceramic capacitor is a good choice to absorb this current and also has very small size.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the buck converter, which is given by below equation.

$$I_{RMS} = I_{CHG} \times \frac{\sqrt{V_{BAT} \times (V_{VBUS} - V_{BAT})}}{V_{VBUS}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC-adapter is plugged into the battery charger. For Notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors be used due to their small size and reasonable cost.

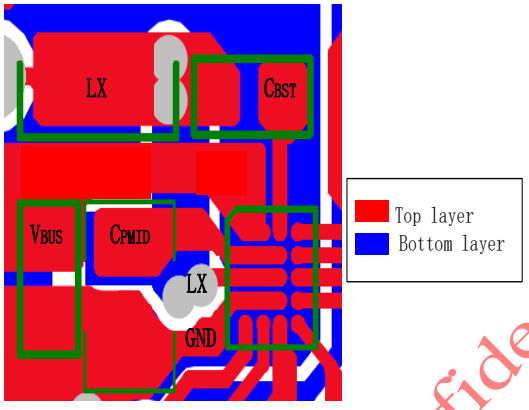
Layout Design:

The layout design of SY6923D1 is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{VBUS} C_{PMID} and C_{BST}.

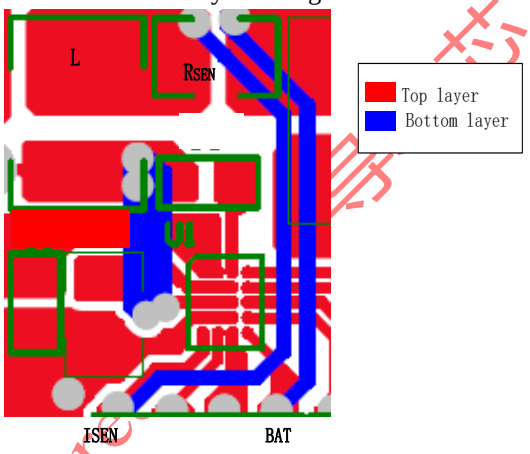
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{VBUS} C_{PMID} and C_{BST} must be close to IC.

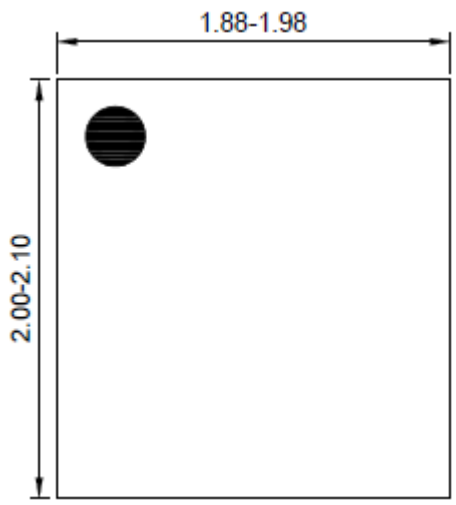
3) The loop area formed by C_{PMID} and GND must be minimized. The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem. The picture below is the recommended layout design of LX, C_{VBUS} ,C_{PMID} and C_{BST}.



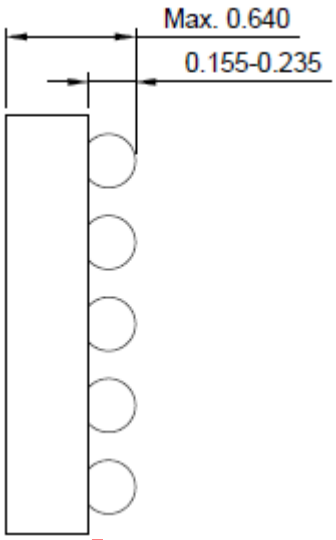
4) The sense resistor should be adjacent to the junction of the inductor and output capacitor, the routes from sense leads on the sense resistor back to the IC should be close to each other to minimize loop area, please don't route the sense leads through a high current path. The picture below is the recommended layout design .



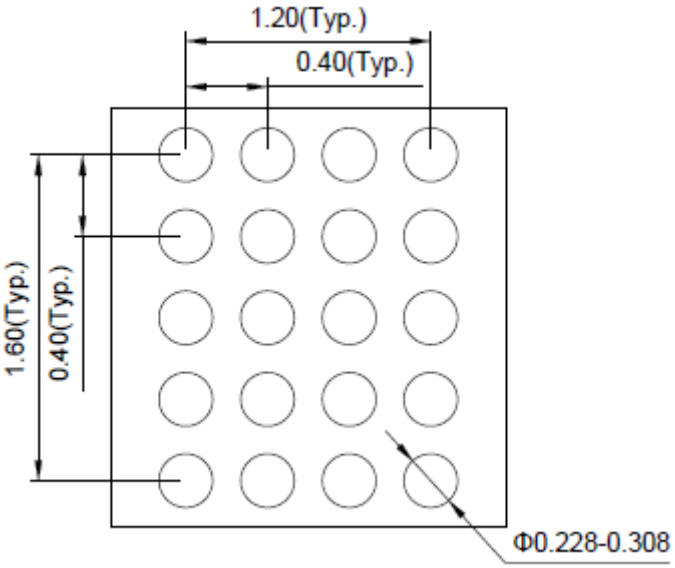
CSP1.93x2.05-20 Package Outline Drawing



Top view



Side view

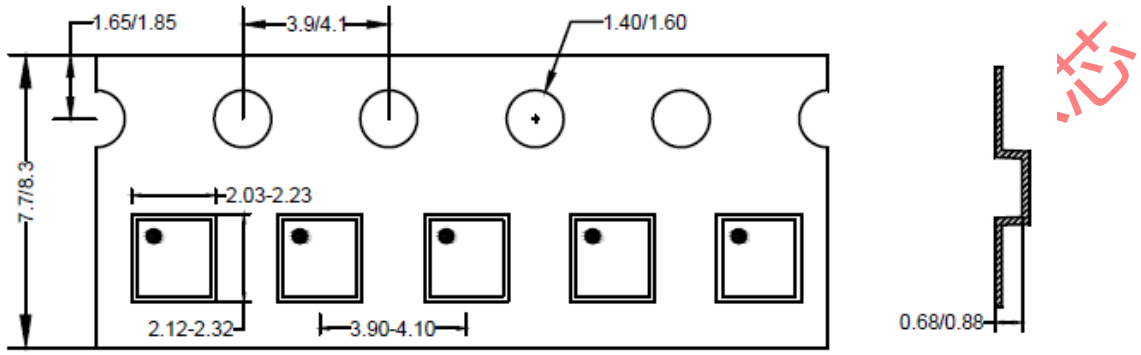


Bottom view

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

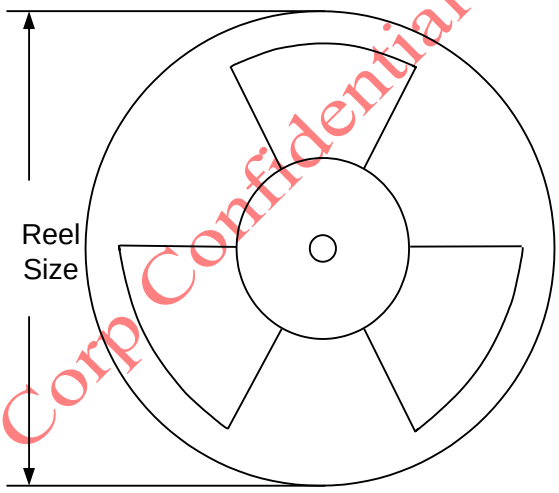
Taping & Reel Specification

1. CSP1.93x2.05



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.93*2.05	8	4	7"	400	160	3000

3. Others: NA

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