



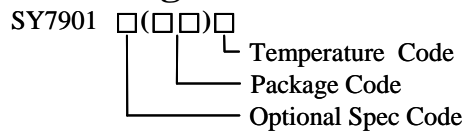
# Application Note: SY7901

## High Efficiency 500kHz, 25V PWM Controller with DC Input Current Limit

### General Description

The SY7901 is a current mode DC/DC controller targeted for Boost, Sepic, Flyback and Forward applications. The SY7901 has an accurate DC input current limit. External compensation provides flexible adjustment of control loops for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current.

### Ordering Information



Ordering Number	Package type	Note
SY7901DBC	DFN3×3-10	----

### Features

- Input Voltage Range 3V to 25V
- 500kHz Fixed Switching Frequency
- An Accurate DC Input Current Limit
- External Compensation
- Internal Soft-start Limits the Inrush Current
- Integrated Low Side Driver: 1.5A Sourcing and 3A Sinking
- RoHS Compliant and Halogen Free
- Compact Package: DFN3×3-10

### Applications

- GPS Navigation Systems
- Handheld Devices
- Portable Media Player

### Typical Applications

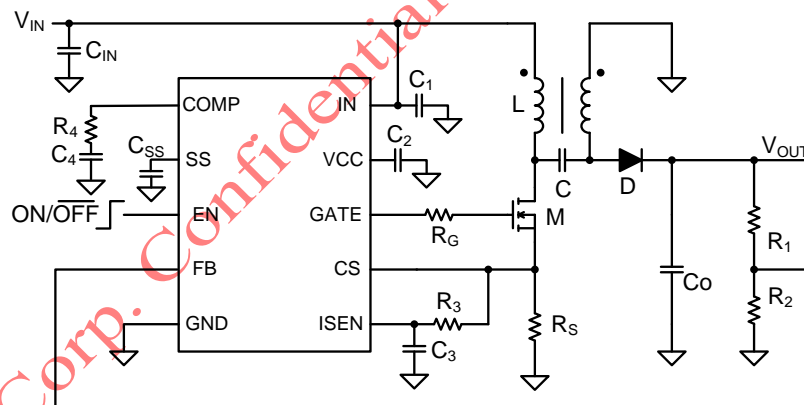
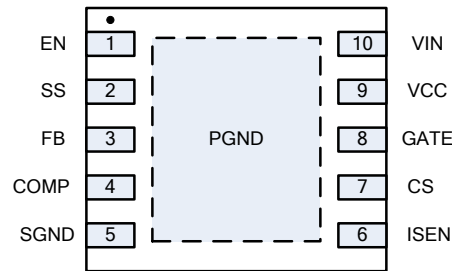


Figure1. Schematic Diagram

## Pinout (top view)



(DFN3×3-10)

**Top Mark: FRxyz for SY7901** (Device code: FR, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
VIN	10	Input pin. Decouple this pin to the PGND pin with at least a 1μF ceramic capacitor.
VCC	9	5V Internal LDO output from VIN. Connect a 4.7 μF capacitor from this pin to PGND.
GATE	8	Driver pin. Connect the gate of the power NFET to this pin.
CS	7	Current sense pin. Connect an external current sensing resistor $R_S$ from this pin to GND. The voltage on this pin is used for providing MOSFET current feedback in the control loop and cycle-by-cycle peak current limit. Peak current limit is triggered when the sensed voltage plus the slope compensation exceed 340mV.
ISEN	6	Connect this pin to CS to program the input average current limit. The input current limit should be $I_{ILIM}=100mV/R_S$
SGND	5	Signal ground pin.
COMP	4	External compensation pin. Connect the RC network from this pin to SGND to compensate the control loop.
FB	3	Output voltage feedback pin. Connect this pin to the output voltage divider to program output voltage: $V_{OUT}=1V \times (1+R_1/R_2)$
SS	2	Connect a capacitor from this pin to SGND to program the soft-start time.
EN	1	Enable pin. Pull it high to turn on the chip. Do not leave this pin floating.
PGND	Exposed Paddle	Power ground pin.

### Absolute Maximum Ratings (Note 1)

IN, EN	26V
GATE	VCC+0.3V
All Other Pins	6V
Power Dissipation, $P_D$ @ $T_A = 25^\circ C$ , DFN3×3-10	2.6W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$	38°C/W
$\theta_{JC}$	8°C/W
Junction Temperature Range	-40 to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

### Recommended Operating Conditions (Note 3)

IN	3V to 25V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		3		25	V
Quiescent Current	$I_Q$	FB=1.1V		170		$\mu A$
Shutdown Current	$I_{SHDN}$	EN=0		0.1		$\mu A$
Feedback Reference Voltage	$V_{REF}$		0.98	1	1.02	V
FB Input Current	$I_{FB}$	$V_{FB}=V_{IN}$	-50		50	nA
Current Sense Limit	$I_{SEN}$		98	100	102	mV
Internal Slope Compensation	$V_{SLOPE}$			40		mV/ $\mu S$
Gm of EA	Gm			300		$\mu A/V$
Gate Driver Output Peak Current	$I_{SOURCE}$			1.5		A
	$I_{SINK}$			3		A
EN Rising Threshold	$V_{ENH}$		1.5			V
EN Falling Threshold	$V_{ENL}$				0.4	V
Input UVLO threshold	$V_{UVLO}$				2.9	V
UVLO hysteresis	$V_{HYS}$			0.3		V
Oscillator Frequency	$F_{OSC}$			500		kHz
Min ON Time				200		ns
Min OFF Time				200		ns
Internal LDO Output	$V_{VCC}$	$V_{IN}=5.5V$	4.9	5	5.1	V
Thermal Shutdown	$T_{SD}$			150		$^\circ C$
Thermal Hysteresis	$T_{HYST}$			20		$^\circ C$

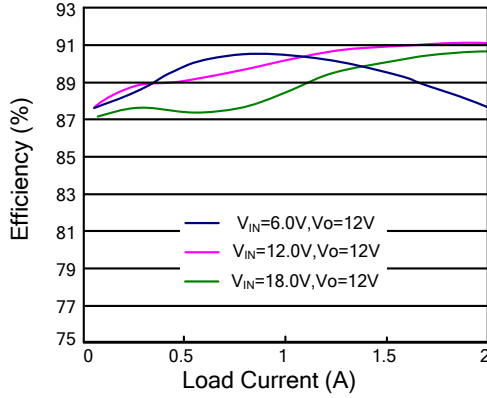
**Note 1:** Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

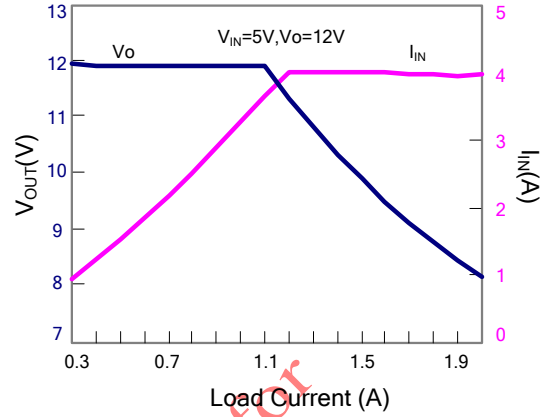
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics

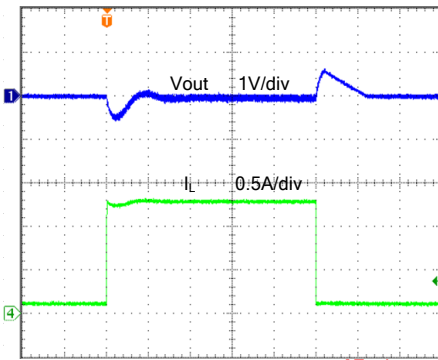
Efficiency vs. Load Current



Input Current Limit

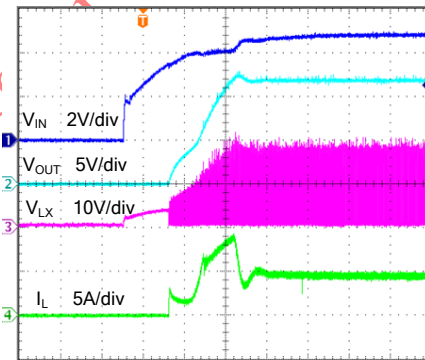


Load Transient  
 $V_{IN}=5.0V, V_{OUT}=12V, I_o=0.1\sim 1.3A$



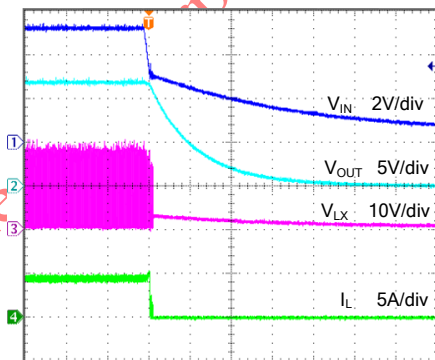
Time (1ms/div)

Startup from  $V_{IN}$   
 $V_{IN}=5.0V, I_o=1.0A$



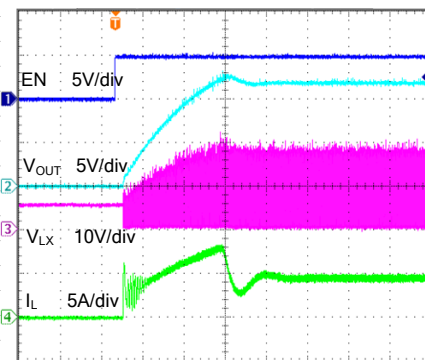
Time (2ms/div)

Startup from  $V_{IN}$   
 $V_{IN}=5.0V, I_o=1.0A$



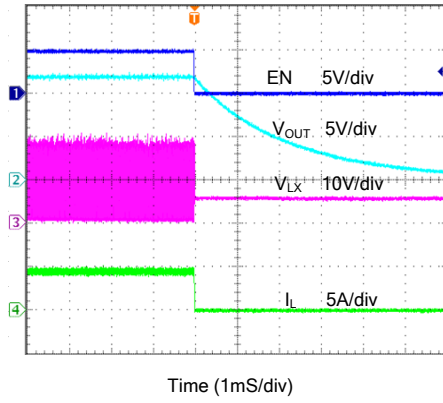
Time (2ms/div)

Startup from Enable  
 $V_{IN}=5.0V, I_o=1.0A$



Time (1ms/div)

Shutdown from Enable  
 $V_{IN}=5.0V$ ,  $I_o=1.0A$



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## Operation

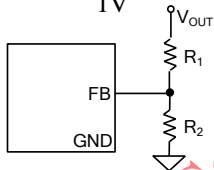
The SY7901 is a current mode DC/DC controller targeted for Boost, Sepic, Flyback and Forward applications. The SY7901 has an accurate DC input current limit. External compensation provides flexible adjustment of control loops for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current. It adopts constant frequency peak current mode control to ensure reliable over current protection and cycle by cycle switch current limit. The input current limit control senses the dc input current via a sense resistor and compares it against the internal threshold. If the input current is below the threshold, the IC operates under the constant output voltage operation mode and the output voltage is regulated by the feedback voltage sensed on the V<sub>OUT</sub>. If the input current meets the threshold, the IC operates in the constant input current mode and the average input current is regulated to a level programmed by the input current sense resistor.

## Applications Information

### Feedback Resistor Dividers R<sub>1</sub> and R<sub>2</sub>:

Choose R<sub>1</sub> and R<sub>2</sub> to program the output voltage under CV mode. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R<sub>1</sub> and R<sub>2</sub>. A value of between 1k and 100k is highly recommended for R<sub>2</sub>. If R<sub>2</sub>=30k is chosen, then R<sub>1</sub> can be calculated to be:

$$R_1 = \frac{(V_{OUT} - 1V) \times R_2}{1V}$$



### Peak Current Sense Resistor

An external sensing resistor R<sub>s</sub> is used to sense the current flow through the MOSFET. The sensed voltage is for peak current mode control and cycle by cycle peak current limit. Peak current limit will be triggered when the voltage on CS pin plus the internal slope compensation exceed 340mV, which is the typical clamping voltage of the PWM comparator. It is desirable to make the maximum value of sensing

voltage plus the slope compensation to be about 70% of the clamping voltage during normal operation. Thus,

$$R_s = \frac{70\% \times 0.34 - V_{slope} \times D \times T_s}{I_{PEAK}}$$

V<sub>SLOPE</sub> is the slew rate of the internal compensation; I<sub>PEAK</sub> is the peak current through MOSFET.

### DC Current Limit

There are two feedback loops inside the controller. When the voltage on ISEN pin meets 100mV threshold, the current feedback loop will take over and regulate the output DC current to the target value. The reference voltage of current feedback loop will be affected by FB pin voltage. When the FB pin voltage is greater than 0.5V, the reference voltage is 100mV. While the FB pin voltage changes from 0.5V to 0.15V, the reference voltage changes from 100mV to 30mV.

### Diode

Average current flowing through the diode is equal to the output current, so the diode current rating should be larger than the maximum output current. Reverse voltage of the diode is equal to V<sub>IN</sub> plus V<sub>O</sub>, so the reverse voltage of the diode should be selected to be larger than the maximum value of V<sub>IN</sub> plus V<sub>O</sub>. It is better to select a Schottky diode to reduce the reverse recovery loss.

### Power MOS

When Power MOS is turned off, the drain to source voltage is equal to V<sub>IN</sub> plus V<sub>O</sub>, so the break down voltage of Power MOS should be larger than the maximum value of V<sub>IN</sub> plus V<sub>O</sub>. When power MOS is turned off, a voltage spike is always generated due to the parasitic inductance, so voltage rating safe margin should be taken into consideration.

### Output Inductor L for Sepic Design:

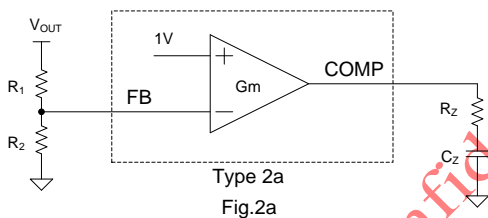
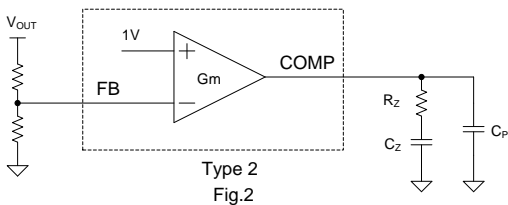
Coupled inductor is recommended for Sepic application to reduce the passive component size. Choose proper inductance to achieve desired current ripple. It is suggested to choose current ripple to be 40% of the maximum value of input current plus output current. Current rating of the inductor should be larger than 1.2×(I<sub>IN\_MAX</sub>+I<sub>O\_MAX</sub>). The inductance is calculated as:

$$L = \frac{V_{IN} \times V_O}{40\% \times F_{SW} \times (I_{OUT} + I_{IN})(V_{IN} + V_O)}$$

## Loop Compensation

The SY7901 incorporates a peak current mode control scheme. The peak current mode control scheme has two feedback loops. The inner loop, current loop, does not require any external compensation component. The outer loop, voltage loop, is compensated with external components.

In most applications, a Type 2 or Type 2a compensation network as show in Fig.2 and Fig.2a can be used to stabilize the voltage loop. The Type 2 is the most widely used and works fine for power stages lagging down to  $-90^\circ$  and where the boost brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected.



To calculate the output voltage sense loop external components, follow the following steps.

1. Select the crossover frequency  $f_c$  of the closed loop. It is recommend that the crossover frequency is chosen 1/5 of right half plane zero ( $f_{RHPZ}$ ) for the tradeoff of stability and transient response of the system. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{\pi \times D_{MAX} \times L2 \times I_{OUT}}$$

2. Select a  $R_z$  value of the R-C series combination connected to the COMP pin.

$$R_z = \frac{V_{OUT}}{G_m \times G_{fc} \times V_{REF}}$$

Where  $G_m$  is the error amplifier gain 300uS,  $G_{fc}$  is gain of the power stage at crossover frequency. For Sepic converter:

$$G_{fc} = \frac{(1-D_{MAX})}{2\pi \times f_c \times C_{OUT} \times R_S \times 4.5}$$

3. Select a  $C_z$  value of the R-C series combination connected to the COMP pin. The capacitor  $C_z$  is for obtaining enough DC gain of loop. A place of compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of  $R_L$  and  $C_O$ .  $R_L$  is the load resistance.

$$C_z = \frac{R_L \times C_O}{R_z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of  $C_{OUT}$

$$C_p = \frac{R_{ESR} \times C_O}{R_z}$$

## Design Example

A design example of typical application is shown below step by step.

### Identify Design Specification

Design Specification			
V <sub>IN</sub>	9V~12V	V <sub>OUT</sub>	12V
I <sub>OUT</sub>	4A	η	90%
I <sub>IN_LIMIT</sub>	6A		

### Inductor Selection

The maximum input current I<sub>IN\_MAX</sub> and duty cycle D<sub>MAX</sub> can be calculated as:

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN\_MIN} \times \eta}$$

$$= \frac{12V \times 4A}{9V \times 0.9} = 5.926A$$

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D}$$

$$= \frac{12V + 0.6V}{9V + 12V + 0.6V} = 0.583$$

If coupled inductor is used, the inductor value is calculated as:

$$L = \frac{V_{OUT} \times D_{MAX}}{40\% \times F_{OSC} \times (I_{OUT} + I_{IN\_MAX})}$$

$$= \frac{12V \times 0.583}{40\% \times 500kHz \times (4A + 5.926A)}$$

$$= 2.8\mu H$$

If two same separate inductors are use, we could calculate the value as:

$$L1 = L2 = 2 \times L = 5.6\mu H$$

The ΔI of inductor current is:

$$\Delta I = \frac{V_{IN\_MIN} \times D_{MAX}}{L1 \times F_{OSC}}$$

$$= \frac{9V \times 0.583}{5.6\mu H \times 500kHz}$$

$$= 1.874A$$

$$I_{PEAK\_L1} = I_{IN\_MAX} + \frac{\Delta I}{2}$$

$$= 5.926 + \frac{1.874A}{2} = 6.863A$$

$$I_{VALLEY\_L1} = I_{IN\_MAX} - \frac{\Delta I}{2}$$

$$= 5.926 - \frac{1.874A}{2} = 4.989A$$

$$I_{PEAK\_L2} = I_{OUT} + \frac{\Delta I}{2}$$

$$= 4 + \frac{1.874A}{2} = 4.937A$$

$$I_{RMS\_L1} = \sqrt{\frac{1}{TS} \times \int_0^{D_{MAX} \cdot TS} (I_{VALLEY\_L1} + \frac{\Delta I \times t}{D_{MAX} \times TS})^2 dt + \frac{1}{TS} \times \int_0^{(1-D_{MAX}) \cdot TS} (I_{PEAK\_L1} - \frac{\Delta I \times t}{(1-D_{MAX}) \times TS})^2 dt}$$

$$= 5.95A$$

It is important that the RMS current and saturation current ratings of the inductor are not exceeded.

### MOSFET Selection

The Peak current, Valley current and RMS current of MOSFET are as follow:

$$I_{PEAK\_M} = I_{IN\_MAX} + I_{OUT} + \Delta I$$

$$= 5.926 + 4 + 1.874A = 11.8A$$

$$I_{VALLEY\_M} = I_{IN\_MAX} + I_{OUT} + \Delta I$$

$$= 5.926 + 4 - 1.874A = 8.05A$$

$$I_{RMS\_M} = \sqrt{\int_0^{D_{MAX} \cdot TS} (I_{VALLEY\_M} + \frac{\Delta I \times t}{D_{MAX} \times TS})^2 dt}$$

$$= 6.88A$$

The SY7901 5V gate driver is optimized for low V<sub>th</sub> and low Q<sub>g</sub> N-MOSFET. BSC093N04LS is used in this design example. The average gate drive current must be less than the 80mA VCC current limit.

The BSC093N04LS have R<sub>DS(on)</sub>=11mΩ, output capacitor C<sub>oss</sub>=340pF, total gate charge Q<sub>g</sub>=11.4nC, gate to drain charge Q<sub>gd</sub>=2nC, series gate resistor R<sub>G</sub>=1Ω, and gate to source voltage threshold V<sub>GS(th)</sub>=2V. We could calculate the gate drive current, MOSFET conduction loss P<sub>CON</sub> and the switching loss P<sub>SW</sub> as follow.

$$I_{GATE} = Q_g \times F_{OSC}$$

$$= 11.4nC \times 500kHz$$

$$= 5.7mA$$

$$P_{CON} = I_{RMS\_M}^2 \times R_{DS(on)}$$

$$= 6.877A^2 \times 11m\Omega = 0.52W$$

$$P_{SW} = \frac{C_{OSS} \times (V_{IN} + V_{OUT})^2 + (V_{IN} + V_{OUT}) \times (I_{PEAK\_M} + I_{VALLEY\_M}) \times \frac{Q_{gd} \times R_G}{V_{CC} - V_{GS(th)}}}{2 \times T_s}$$

$$= 0.107W$$

### Current Sense Resistor Selection

a) Select the R<sub>S</sub> with peak current limit.

$$R_{S1} = \frac{0.34 - V_{SLOPE} \times D_{MAX} \times TS}{I_{PEAK\_M}}$$

$$= \frac{0.34 - 40mV/us \times 0.538 \times 2us}{11.8A}$$

$$= 25m\Omega$$

b) Select the R<sub>S</sub> with input current limit:

$$R_{S2} = \frac{V_{ISEN}}{I_{IN\_LIMIT}}$$

$$= \frac{100mV}{6A} = 16.7m\Omega$$

Set the RS equal to the lower value of RS1 and RS2:

$$R_S = R_{S2} = 16.7m\Omega$$

The maximum power loss on RS:

$$P_{RS\_MAX} = \frac{(340mV - V_{SLOPE} \times T_S)^2}{R_S}$$

$$= \frac{(340mV - 40mV/us \times 2us)^2}{16.7m\Omega} = 4.04W$$

The maximum power loss in RS is 4.04W; nine 0.5W rated sense resistors are used in parallel in this application.

### Couple Capacitor Selection CS

The RMS current of CS can be calculated as follow:

$$I_{RMS\_CS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}}} = 4.6A$$

The voltage ripple on 22uF CS can be calculated as follow:

$$\Delta V_{CS} = \frac{D_{MAX} \times I_{OUT}}{F_{OSC} \times C_S}$$

$$= \frac{0.583 \times 4A}{500kHz \times 22\mu F}$$

$$= 0.212V$$

### Output Capacitor Selection COUT

The RMS current of COUT is:

$$I_{RMS\_OUT} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}}} = 4.6A$$

We suppose the output voltage ripple is 1% of VOUT

$$\Delta V_{OUT} = V_{OUT} \times 1\% = 12 \times 0.01 = 0.12V$$

The ESR of COUT:

$$ESR \leq \frac{\Delta V_{OUT} \times 0.5}{I_{PEAK\_L1} + I_{PEAK\_L2}}$$

$$= \frac{0.12V \times 0.5}{11.852}$$

$$= 5m\Omega$$

$$C_{OUT} \geq \frac{I_{OUT} \times D_{MAX}}{\Delta V_{OUT} \times 0.5 \times F_{OSC}}$$

$$= \frac{4A \times 0.583}{0.12V \times 0.5 \times 500kHz}$$

$$= 77\mu F$$

We could select 4PCS low ESR 22uF ceramic capacitor.

### Control Loop Compensation Design

There is a Right Half Plane Zero (fRHPZ) as follow:

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{\pi \times D_{MAX} \times L_2 \times I_{OUT}}$$

$$= \frac{(1 - 0.583)^2 \times 12V}{3.14 \times 0.583 \times 5.6\mu \times 4A}$$

$$= 50kHz$$

Set the crossover frequency at 1/6 of fRHPZ:

$$f_c = \frac{f_{RHPZ}}{6} = \frac{50kHz}{6} = 8.3kHz$$

The gain of the power stage Gfc could be calculated:

$$G_{fc} = \frac{(1 - D_{MAX})}{2\pi \times f_c \times C_{OUT} \times R_S \times 4.5}$$

$$= \frac{(1 - 0.583)}{2 \times 8.3kHz \times 3.14 \times 88\mu F \times 16.7m\Omega \times 4.5}$$

$$= 1.21$$

$$R_Z = \frac{V_{OUT}}{G_m \times G_{fc} \times V_{REF}}$$

$$= \frac{12V}{300\mu S \times 1.21 \times 1V}$$

$$= 33k\Omega$$

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

$$= \frac{12V \times 88\mu F}{4A \times 33k\Omega}$$

$$= 8nF$$

Set CZ = 10nF

## Other Application Examples

Figure 2 to 5 show other application examples of using SY7901.

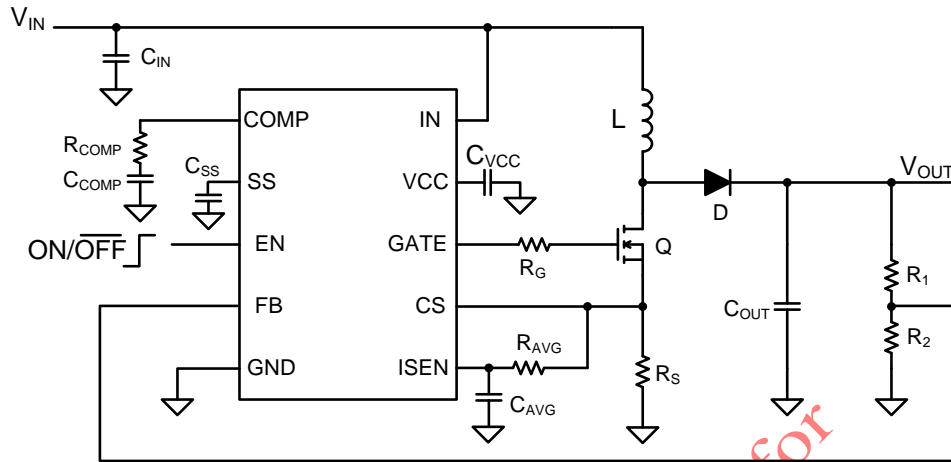


Figure 2. Boost with Power MOS Current Limit

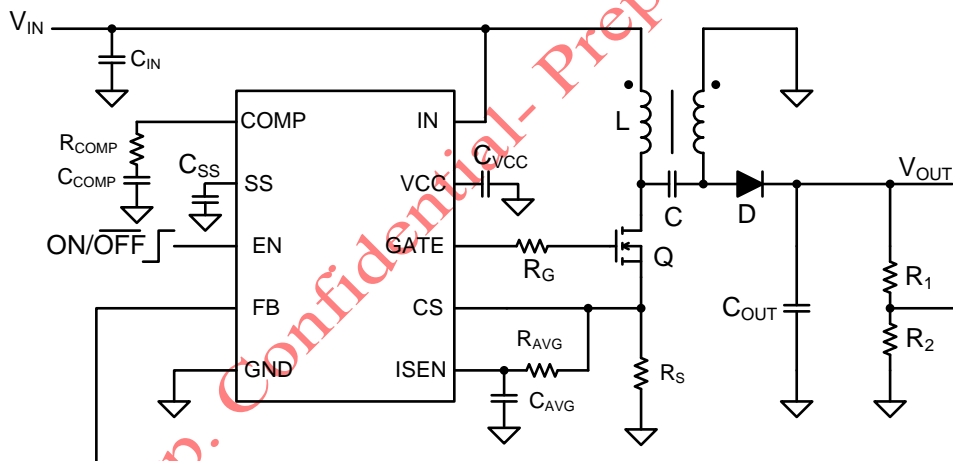


Figure 3. Sepic with Input Current Limit

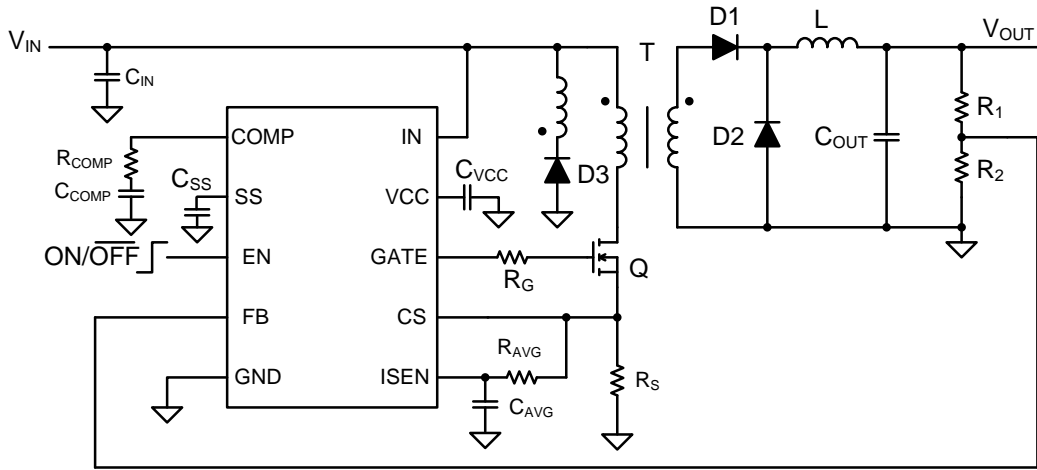


Figure 4 Forward with Input Current Limit

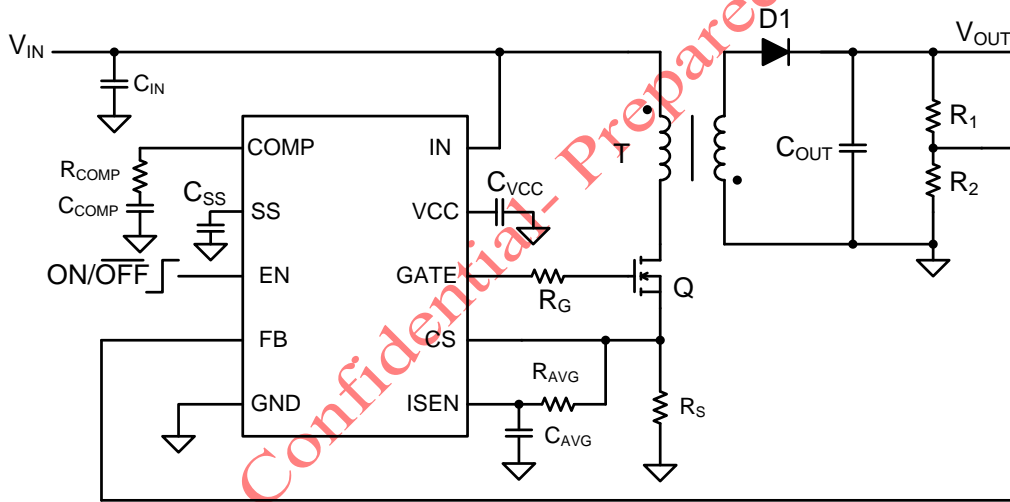
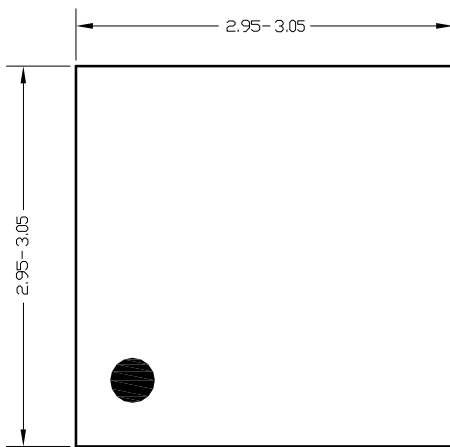
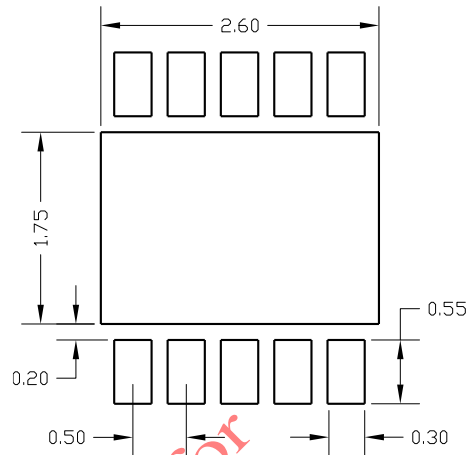


Figure 5 Flyback with Input Current Limit

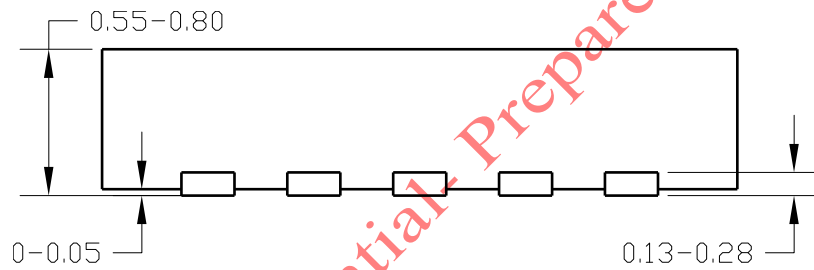
### DFN3×3-10 Package Outline



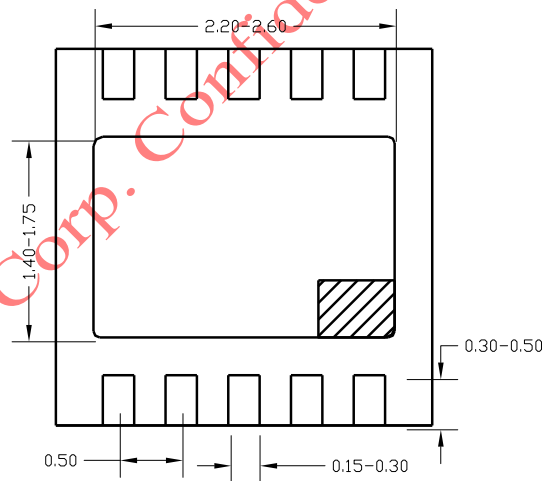
Top View



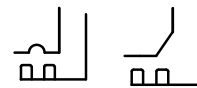
PCB layout (recommended)



Side View



Bottom View

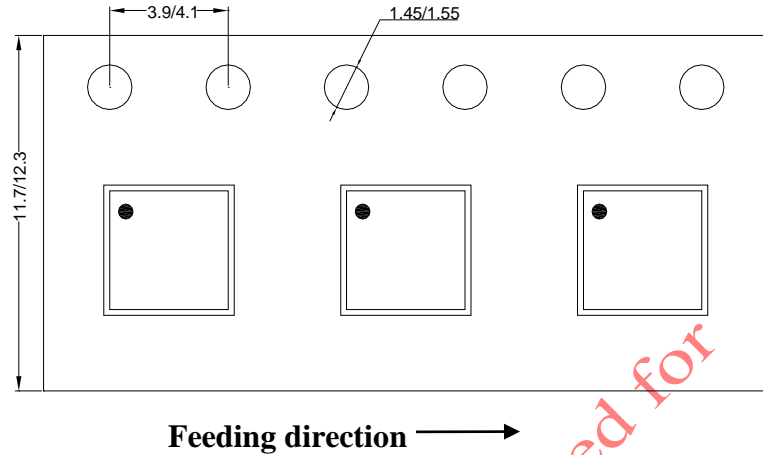


Detail A  
Pin1 identifier: two options

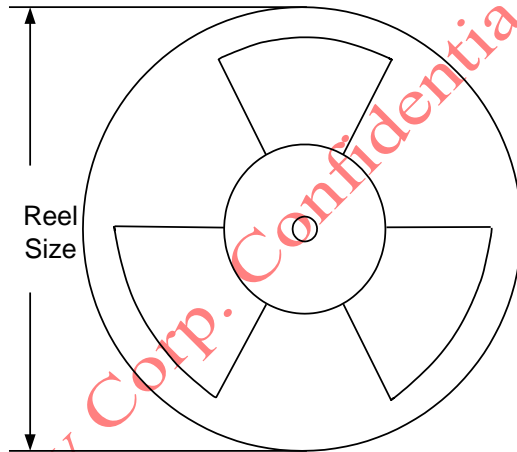
**Notes: All dimensions are in millimeters and exclude mold flash & metal burr.**

## Taping & Reel Specification

### 1. DFN3×3-10 taping orientation



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	10	8	13"	400	400	5000