



P-Channel High Density Trench MOSFET

PRODUCT SUMMARY		
V _{DS}	I _D	R _{DS(on)} (m-ohm) Max
-20V	-2.2	125 @ V _{GS} = 4.5V
	-1.4	170 @ V _{GS} = 2.5V

FEATURES

- Super high dense cell trench design for low R_{DS(on)}.
- Rugged and reliable.
- Surface Mount package.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	± 8	V
Drain Current-Continuous ^a @ T _A = 25 °C -Pulse ^b	I _D	-2.2	A
	I _{DM}	-6	A
Drain-Source Diode Forward Current ^a	I _S	-0.75	A
Maximum Power Dissipation ^a	P _D	T _A =25°C	1.25
		T _A =75°C	0.75
Operating Junction and Storage Temperature Range	T _J , T _{SI} G	- 55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R _{thJA}	100	°C/W
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Note

a. Surface Mounted on FR4 Board , t ≤ 10sec .

b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$			-100	nA
ON CHARACTERISTICS^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.45	-0.65	-0.95	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -2.8A$		75	95	m-ohm
		$V_{GS} = -2.5V, I_D = -2.0A$		90	140	m-ohm
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = -0.75A$			-1.2	V
DYNAMIC CHARACTERISTICS^c						
Input Capacitance	C_{ISS}	$V_{DS} = -6V, V_{GS} = 0V$ $f = 1.0MHz$		658		pF
Output Capacitance	C_{OSS}			150		pF
Reverse Transfer Capacitance	C_{RSS}			125		pF
SWITCHING CHARACTERISTICS^c						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = -6V, I_D = -1A$ $V_{GEN} = -4.5V$ $R_L = 6\text{ ohm}$ $R_{GEN} = 6\text{ ohm}$		8.4		ns
Rise Time	t_r			3.0		ns
Turn-Off Delay Time	$t_{D(OFF)}$			39.1		ns
Fall Time	t_f			11.3		ns
Total Gate Charge	Q_g	$V_{DS} = -6V$ $I_D = -2.8A$ $V_{GS} = -4.5V$		6.70		nC
Gate-Source Charge	Q_{gs}			1.12		nC
Gate-Drain Charge	Q_{gd}			1.02		nC

Note

b. Pulse Test Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

c. Guaranteed by design, not subject to production testing.

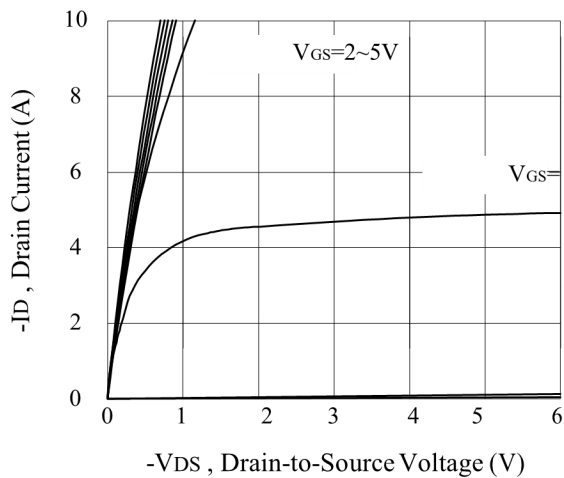


Figure 1. Output Characteristics

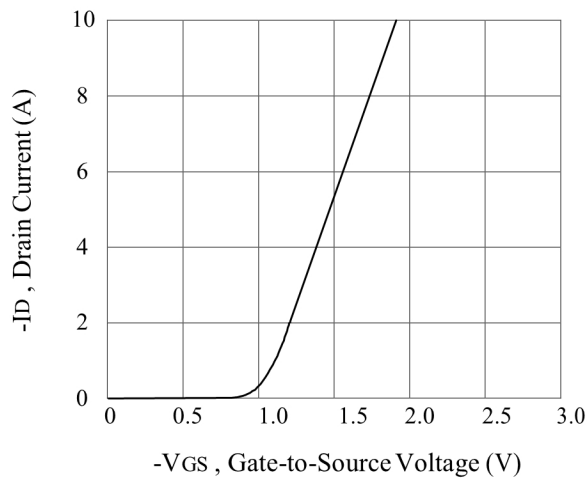


Figure 2. Transfer Characteristics

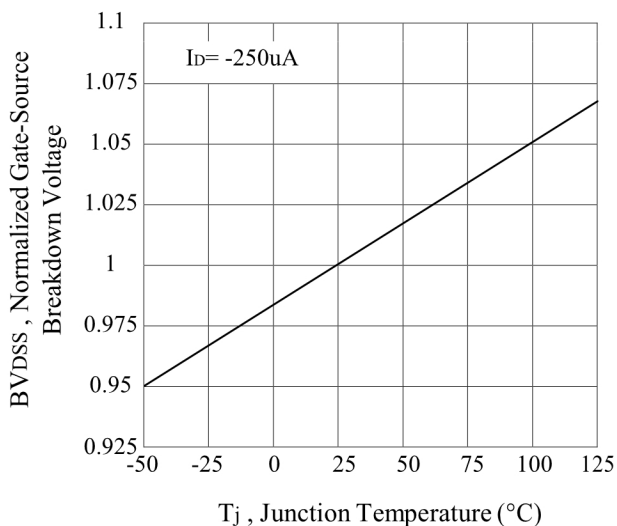


Figure 3. Breakdown Voltage Variation with Temperature

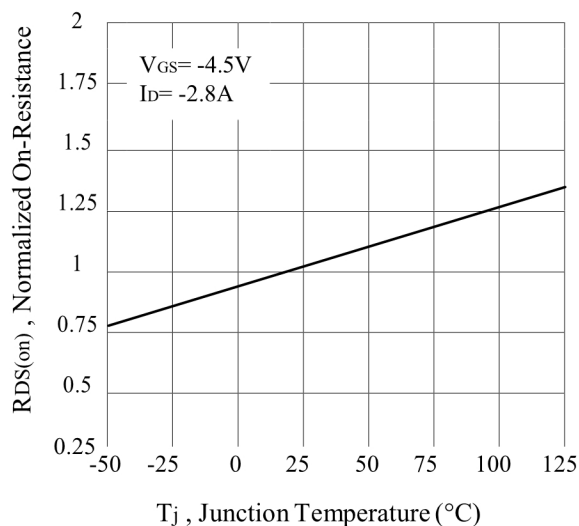


Figure 4. On-Resistance Variation with Temperature

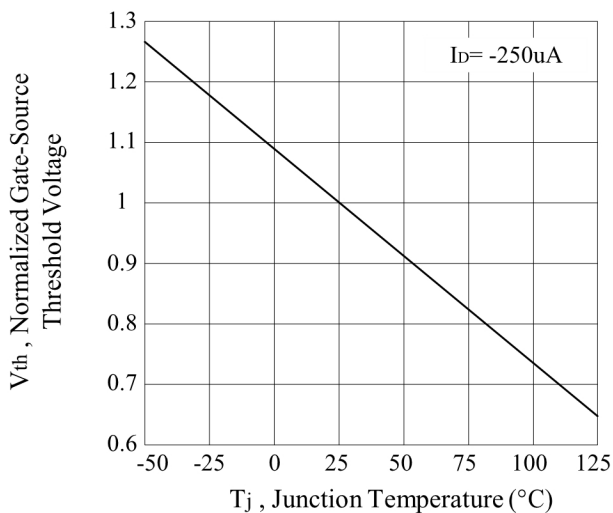


Figure 5. Gate Threshold Variation with Temperature

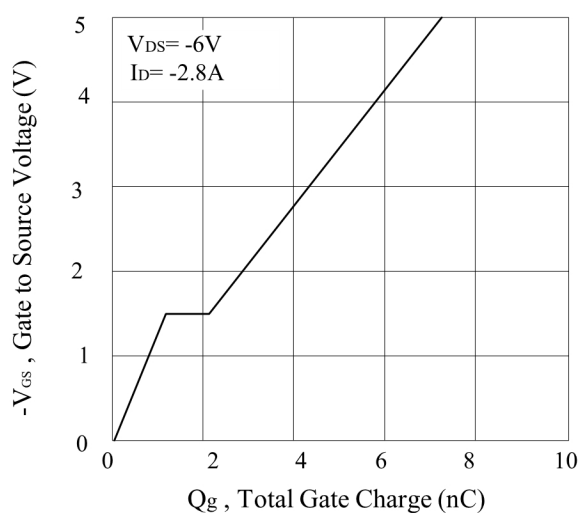
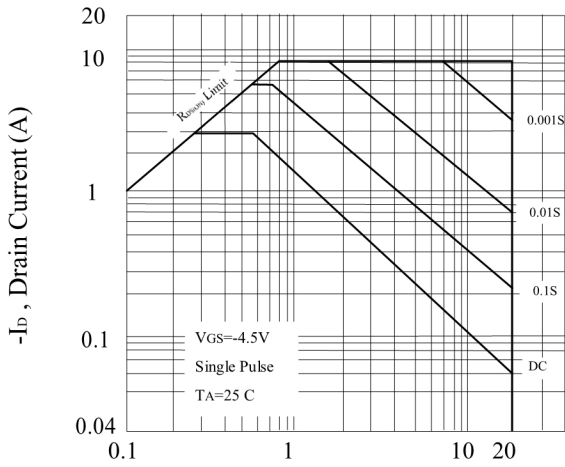
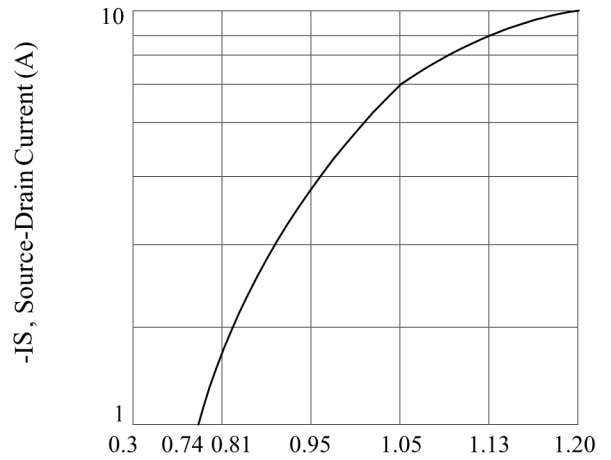


Figure 6. Gate Charge



-VDS, Drain-Source Voltage (V)
Figure 7. Maximum Safe Operating Area



-VSD, Body Diode Forward Voltage (V)
Figure 8. Body Diode Forward Voltage Variation with Source Current

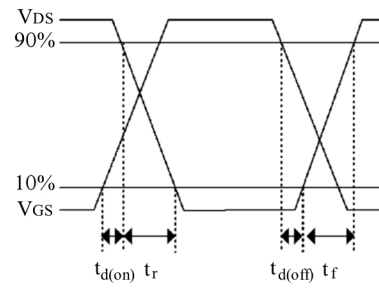
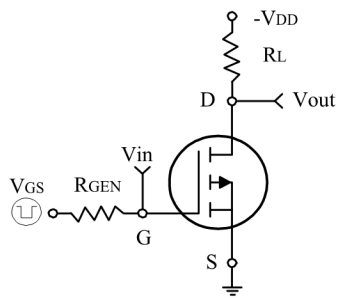


Figure 9. Switching Test Circuit and Switching Waveforms

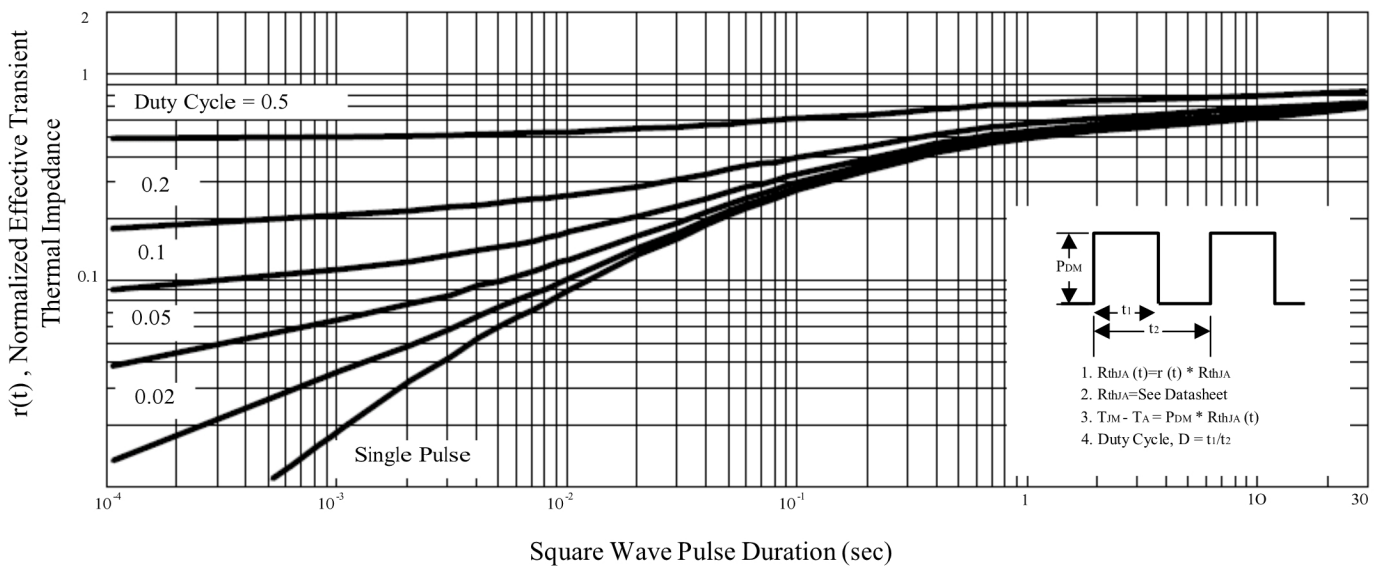


Figure 10. Normalized Thermal Transient Impedance Curve