

# Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

## Features

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low noise figure(NF)=0.7dB;
- High power gain=17.5dB;
- High linearity IIP3oob=0dBm;
- High input 1dB-compression point=-9.5dBm;
- GPS L1 requires only one input matching inductor;
- RF output internally matched to 50 ohm for GPS L1;
- Supply voltage: 1.5V to 3.3V;
- Operating frequencies: 1550~1615MHz; 1164~1300MHz;
- DFN-6L package:1.1mmX0.7mmX0.37mm
- 2000V HBM ESD protection (including RFIN and RFOUT pin)

## Applications

- Smart Phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

## General Description

- The AW15645DNR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW15645DNR can be close to the antenna, requires only one external input matching inductor, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW15645DNR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15645DNR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.
- The AW15645DNR is available in a small lead-free, RoHS-Compliant, DFN 1.1 mm x 0.7 mm x 0.37 mm-6L package.

Typical Application Circuit

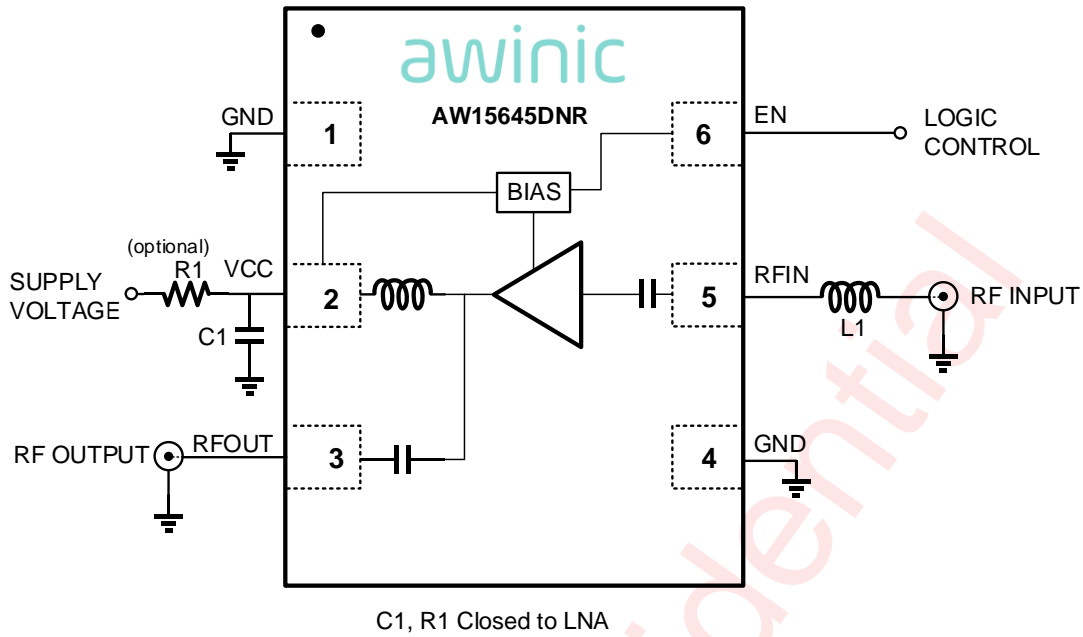


Figure 1(a) Typical Application Circuit of AW15645DNR for GNSS L1

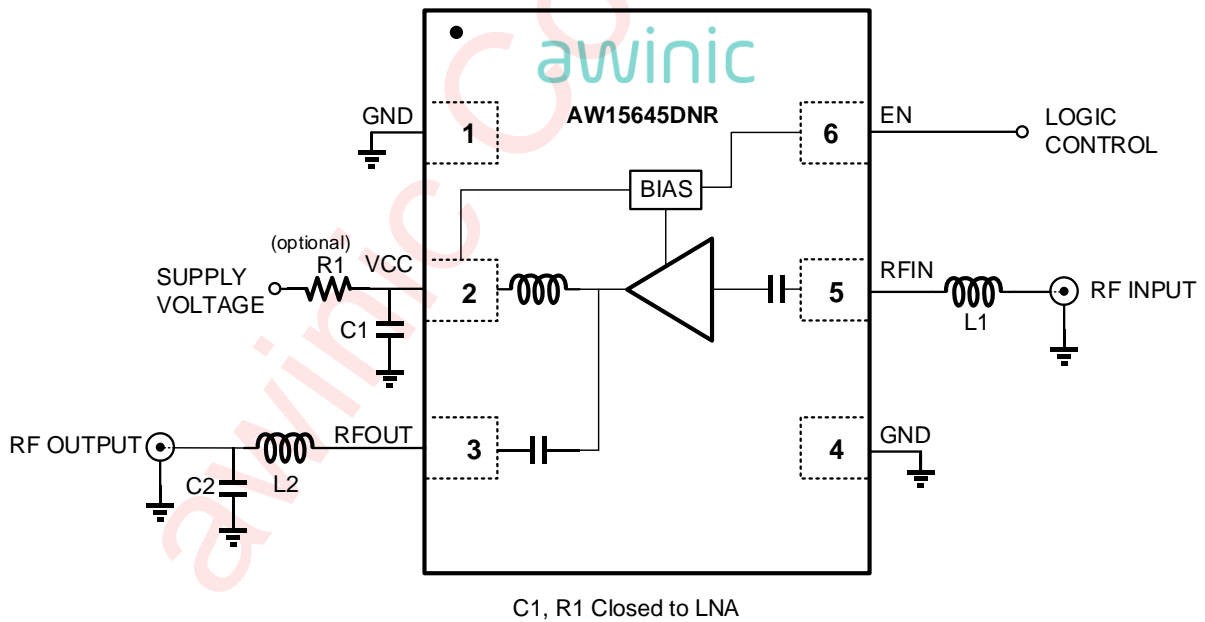


Figure 1(b) Typical Application Circuit of AW15645DNR for GNSS L2/L5

## Recommended Components List

Table1: list of components for GNSS L1

Component	Part Number	Inductance (nH)	Q(min)	Q Test Frequency (MHz)	Supplier	Size
L1	LQW15A	10	25	250	Murata	0402
L1	SDWL1005C	10	24	250	Sunlord	0402
Component	Part Number	Capacitance (pF)	Rated Voltage (V)		Supplier	Size
C1	GRM155	1000	50		Murata	0402

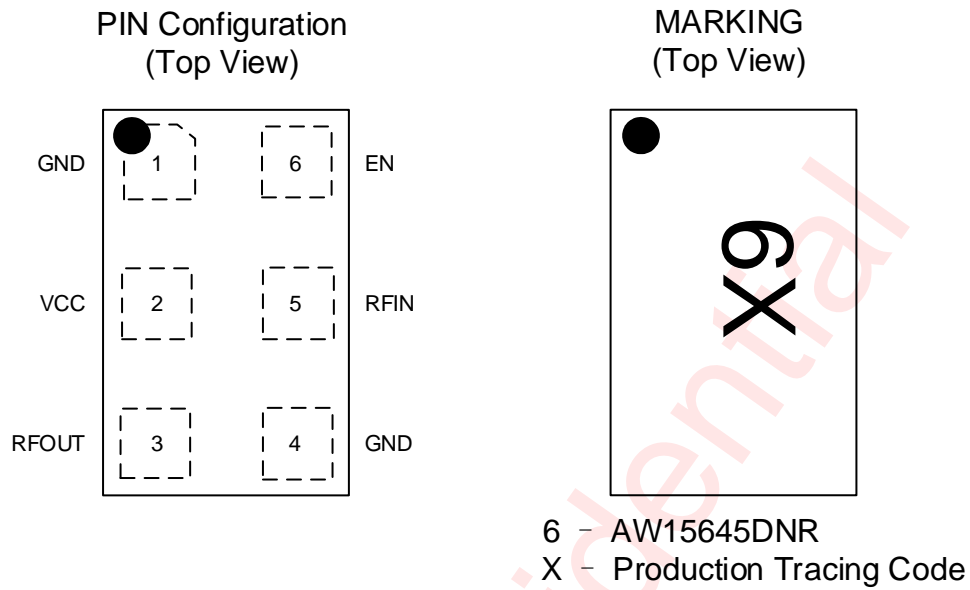
Table2: list of components for GNSS L2

Component	Part Number	Inductance (nH)	Q(min)	Q Test Frequency (MHz)	Supplier	Size
L1	LQW15A	16	25	250	Murata	0402
L2	LQW15A	6.8	25	250	Murata	0402
Component	Part Number	Capacitance (pF)	Rated Voltage (V)		Supplier	Size
C1	GRM155	1000	50		Murata	0402
C2	GRM155	3	50		Murata	0402

Table3: list of components for GNSS L5

Component	Part Number	Inductance (nH)	Q(min)	Q Test Frequency (MHz)	Supplier	Size
L1	LQW15A	16	25	250	Murata	0402
L2	LQW15A	8.7	25	250	Murata	0402
Component	Part Number	Capacitance (pF)	Rated Voltage (V)		Supplier	Size
C1	GRM155	1000	50		Murata	0402
C2	GRM155	3	50		Murata	0402

## Pin Configuration And Top Mark



**Figure 2 Pin Configuration and Top Mark**

## Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

## Functional Block Diagram

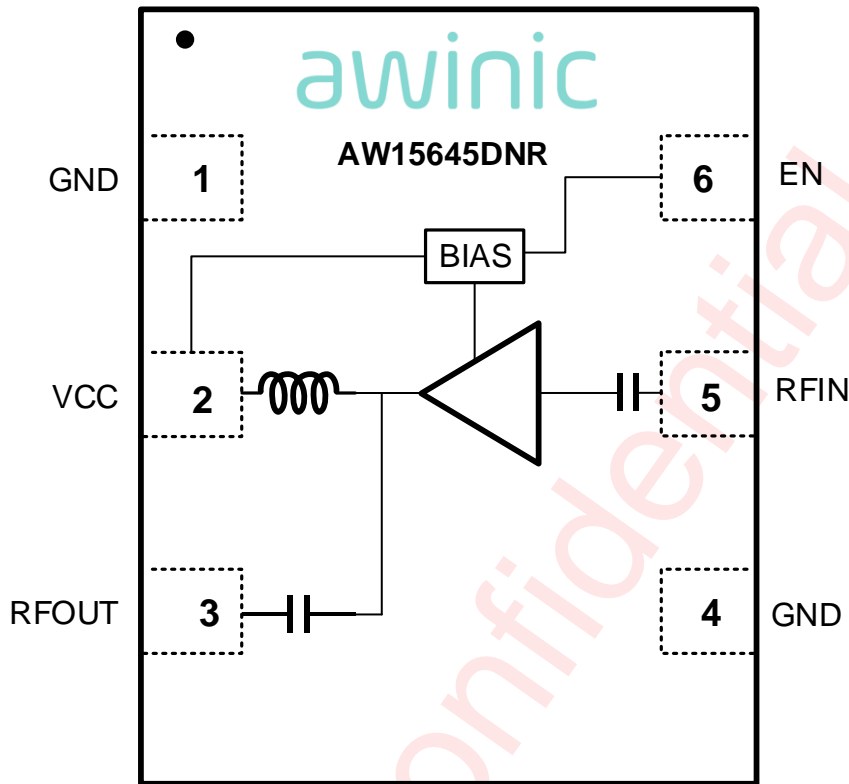


Figure 3 Functional Block Diagram

## Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15645DNR	-40°C ~ 85°C	DFN 1.1mmx0.7mmx0.37mm-6L	6	MSL1	ROHS+HF	9000 units/ Tape and Reel

**Absolute Maximum Ratings**<sup>[1]</sup>

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V <sub>CC</sub>	-0.3	-	3.6	V
Voltage at pin EN <sup>[2]</sup>	V <sub>EN</sub>	-0.3	-	3.6	V
Current into pin VCC	I <sub>CC</sub>	-	-	30	mA
RF input power <sup>[3]</sup>	P <sub>IN</sub>	-	-	15	dBm
Package thermal resistance	θ <sub>JA</sub>	-	148	-	°C/W
Junction temperature	T <sub>J</sub>	-	-	150	°C
Storage temperature range	T <sub>STG</sub>	-65	-	150	°C
Ambient temperature range	T <sub>amb</sub>	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM <sup>[4]</sup>			±2000		V
CDM <sup>[4]</sup>			±1000		V
Latch-up					
Standard: JESD78E			+IT: +200 -IT: -200		mA mA

**Note1:** Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Note2:** Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 5.0V in order to avoid excess current.

**Note3:** The RF input and RF output are AC coupled through internal DC blocking capacitor.

**Note4:** HBM standard: ESDA/JEDEC JS-001-2017. CDM standard: ESDA/JEDEC JS-002-2018.

## Electrical Characteristics

(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=2.8V and TA=+25°C, f=1550-1615MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.9	9.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		16.0	18.0	20.0	dB
R <sub>L</sub> <sub>in</sub>	Input Return Loss		6.0	10.0		dB
R <sub>L</sub> <sub>out</sub>	Output Return Loss		8.0	14.0		dB
ISL	Reverse Isolation		20.0	28.0		dB
NF	Noise Figure <sup>[2]</sup>	Z <sub>s</sub> =50 ohm; No jammer		0.7	1.0	dB
K <sub>f</sub>	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-13.0	-7.0		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1575.42MHz; f2=1576.42MHz; Pin=-30dBm;	-5.0	0.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point <sup>[3]</sup>	f1=1712.7MHz; f2=1850MHz;	-5.0	1.0		dBm
H2-input referred	LTE band-13 2 <sup>nd</sup> Harmonic	f=787.76MHz Pin=-25dBm		-50		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 10nH inductor.

**Note2:** 0.08dB PCB losses are subtracted.

**Note3:** Input power = -20 dBm at f1 and -65 dBm at f2.

(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=1.8V and TA=+25°C, f=1550-1615MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.6	8.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		15.5	17.5	20.0	dB
RL <sub>in</sub>	Input Return Loss		6.0	10.0		dB
RL <sub>out</sub>	Output Return Loss		8.0	12.0		dB
ISL	Reverse Isolation		20.0	28.0		dB
NF	Noise Figure <sup>[2]</sup>	Z <sub>s</sub> =50 ohm; No jammer		0.7	1.0	dB
K <sub>f</sub>	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-13.0	-9.5		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1575.42MHz; f2=1576.42MHz; Pin=-30dBm;	-7.0	-2.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point <sup>[3]</sup>	f1=1712.7MHz; f2=1850MHz;	-5.0	0		dBm
H2-input referred	LTE band-13 2 <sup>nd</sup> Harmonic	f=787.76MHz Pin=-25dBm		-50		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 10nH inductor.

**Note2:** 0.08dB PCB losses are subtracted.

**Note3:** Input power = -20 dBm at f1 and -65 dBm at f2.

(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=2.8V and TA=+25°C, f=1164-1215MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.9	9.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		15.5	18	20.5	dB
RL <sub>in</sub>	Input Return Loss		6.0	8.0		dB
RL <sub>out</sub>	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	30.0		dB
NF	Noise Figure <sup>[2]</sup>	Zs=50 ohm; No jammer		0.7	1.0	dB
Kf	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-15.0	-9.0		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1176.45MHz; f2=1177.45MHz; Pin=-30dBm;	-6.0	-4.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point	f1=1800MHz; f2=2400MHz; Pin=-20dBm;	-3	15		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 16nH inductor. Output matching using 8.7nH inductor and 3pF capacitor.

**Note2:** 0.08dB PCB losses are subtracted.

(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=1.8V and TA=+25°C, f=1164-1215MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.6	8.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		15.5	17.5	20.5	dB
RL <sub>in</sub>	Input Return Loss		6.0	8.0		dB
RL <sub>out</sub>	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	30.0		dB
NF	Noise Figure <sup>[2]</sup>	Z <sub>s</sub> =50 ohm; No jammer		0.7	1.0	dB
K <sub>f</sub>	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-17.0	-12.0		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1176.45MHz; f2=1177.45MHz; Pin=-30dBm;	-10.0	-5.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point	f1=1800MHz; f2=2400MHz; Pin=-30dBm;	-3	15		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 16nH inductor. Output matching using 8.7nH inductor and 3pF capacitor.

**Note2:** 0.08dB PCB losses are subtracted.

(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=2.8V and TA=+25°C, f=1215-1300MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.9	9.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		15.5	18	20.5	dB
RL <sub>in</sub>	Input Return Loss		6.0	8.0		dB
RL <sub>out</sub>	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	30.0		dB
NF	Noise Figure <sup>[2]</sup>	Z <sub>s</sub> =50 ohm; No jammer		0.7	1.0	dB
K <sub>f</sub>	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1227.6MHz	-15.0	-9.0		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1227.6MHz; f2=1228.6MHz; Pin=-30dBm;	-6.0	-4.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point	f1=1850MHz; f2=2485MHz; Pin=-25dBm;	-3	13.5		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 16nH inductor. Output matching using 6.8nH inductor and 3pF capacitor.

**Note2:** 0.08dB PCB losses are subtracted.

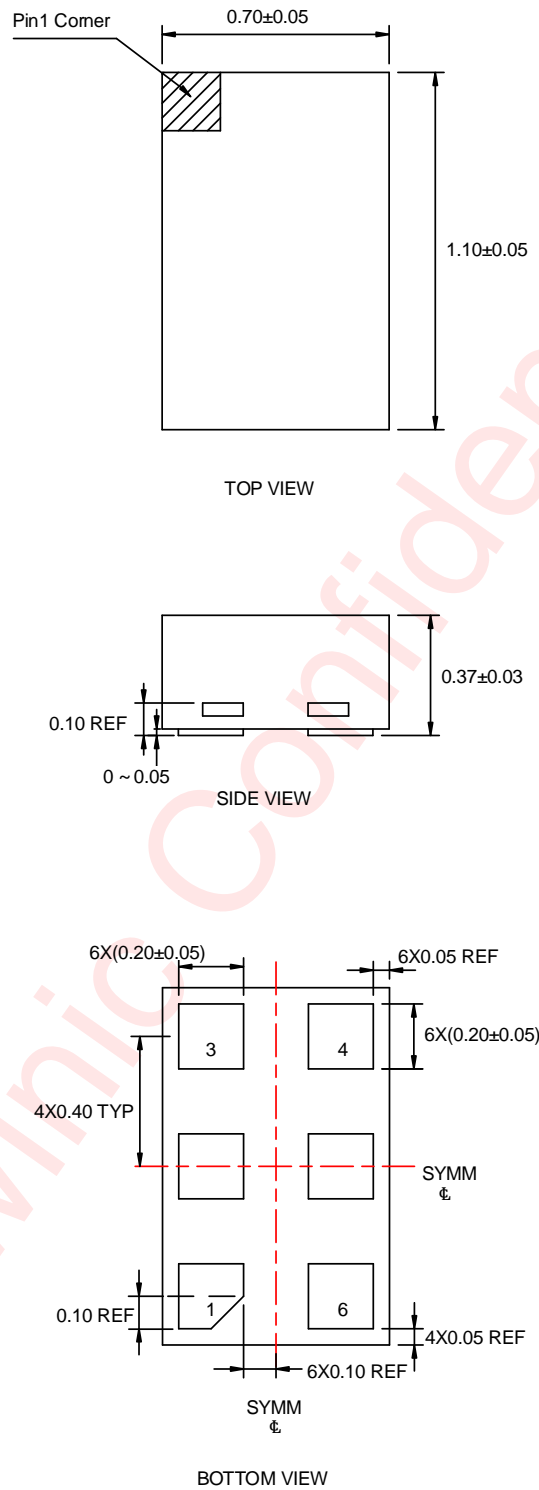
(AW15645DNR EVB<sup>[1]</sup>; Typical values are at VCC=1.8V and TA=+25°C, f=1215-1300MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
V <sub>CC</sub>	Supply Voltage		1.5	-	3.3	V
I <sub>SD</sub>	Shut-Down Current	EN=Low			1	μA
I <sub>CC</sub>	Supply Current	EN=High		5.6	8.0	mA
V <sub>EN</sub>	Digital Input-Logic High		1.0		3.3	V
V <sub>EN</sub>	Digital Input-Logic Low				0.4	V
I <sub>EN</sub>	Digital Input-Logic High				10	μA
<b>AC ELECTRICAL CHARACTERISTICS</b>						
G <sub>p</sub>	Power Gain		15.5	17.5	20.5	dB
RL <sub>in</sub>	Input Return Loss		6.0	8.0		dB
RL <sub>out</sub>	Output Return Loss		6.0	14.0		dB
ISL	Reverse Isolation		20.0	30.0		dB
NF	Noise Figure <sup>[2]</sup>	Z <sub>s</sub> =50 ohm; No jammer		0.7	1.0	dB
K <sub>f</sub>	Stability factor	f=20MHz...10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1227.6MHz	-17.0	-12.0		dBm
IIP3 <sub>ib</sub>	Inband input 3 <sup>rd</sup> -order intercept point	f1=1227.6MHz; f2=1228.6MHz; Pin=-30dBm;	-10.0	-5.0		dBm
IIP3 <sub>oob</sub>	Out-of-band input 3 <sup>rd</sup> -order intercept point	f1=1850MHz; f2=2485MHz; Pin=-25dBm;	-3	13		dBm
t <sub>on</sub>	turn-on time	time from V <sub>EN</sub> ON to 90% of the final gain		2.2	3.0	μs
t <sub>off</sub>	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.4	3.0	μs

**Note1:** input matched to 50 ohm using a high quality-factor 16nH inductor. Output matching using 6.8nH inductor and 3pF capacitor.

**Note2:** 0.08dB PCB losses are subtracted.

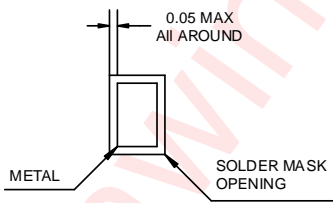
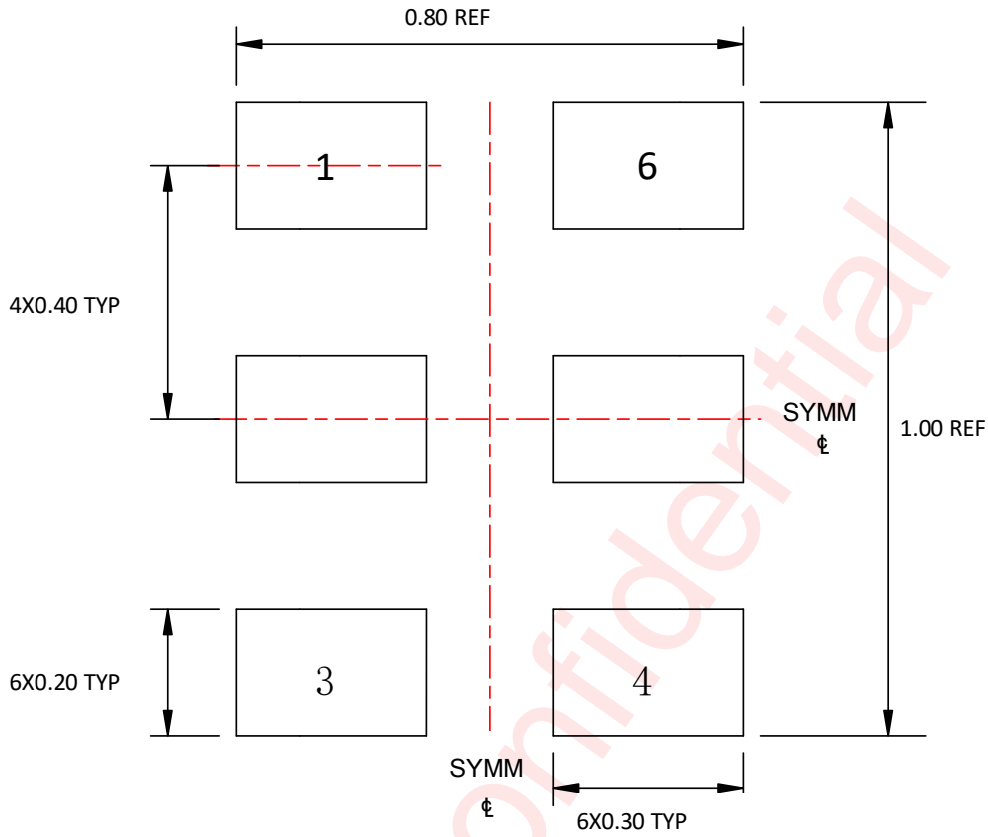
Package Description



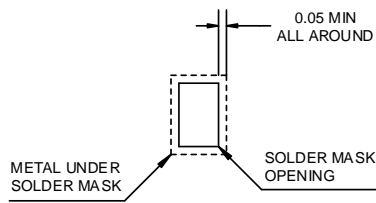
Unit: mm

Figure 8 Package Outline

Land Pattern



NON-SOLDER MASK DEFINED

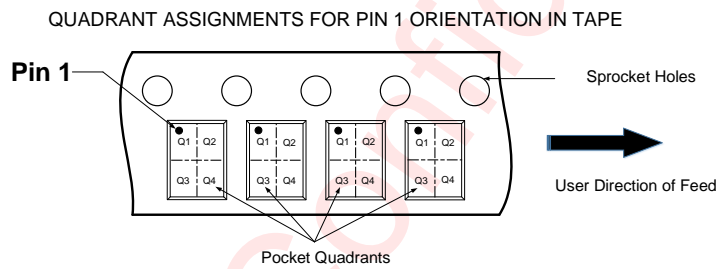
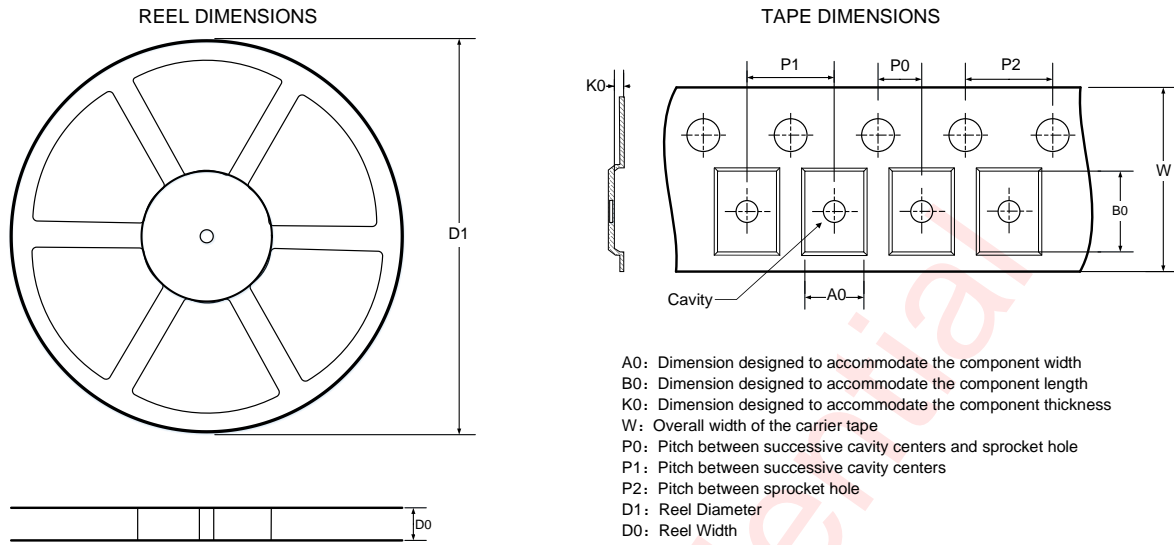


SOLDER MASK DEFINED

Unit: mm

Figure 9 Land Pattern

## Tape & Reel Description



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.46	2	2	4	8	Q1

All dimensions are nominal

Figure 10 Tape & Reel Description

## Revision History

Version	Date	Change Record
V1.0	Feb. 2022	Officially Released
V1.1	Aug. 2022	Update format
V1.2	Aug. 2022	Add the electrical characteristics of L2
V1.3	Aug. 2022	Update format
V1.4	Aug. 2022	Update format

awinic Confidential

## Disclaimer

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.