2A 6-Channel Load Switch with Slew Rate Control

FEATURES

- Integrated 6 P-channel MOSFETs
- Supply voltage: 1.5V to 5.5V
- Input voltage: 1.2V to 5.5V
- Typical on-state resistance R_{ON} (V_{VSYS}=1.8V):
  R_{ON}=56mΩ at V_{INX}=5.0V
  R_{ON}=71mΩ at V_{INX}=3.3V
  R_{ON}=122mΩ at V_{INX}=1.8V
- Ultra-low quiescent and shutdown current
- I^2C configuration (per channel):
  On/Off control & power sequence
  Programmable slew rate control (4 options)
  Selectable quick output discharge (QOD)
  Selectable reverse current blocking
- 2A maximum continuous current for V_{INX}>1.8V
- FOWLP 1.50mm x 1.50mm x 0.495mm - 16B package

APPLICATIONS

- Smartphones and tablets
- Portable and wearable devices

GENERAL DESCRIPTION

The AW35206 is a 6-channel, low R_{ON} load switch with user programmable features. The device integrates six P-channel MOSFETs that operates over the input voltage from 1.2V to 5.5V. While the supply voltage range of the system is 1.5V ~5.5V. All load switches are controlled through I^2C BUS which makes it realizable for usage with processors having limited GPIO available.

The rising time of output voltage is programmable to avoid inrush current. Each output integrates a quick output discharge (QOD) function block that can be disabled via I^2C BUS. Also every load switch has the ability that cuts off current when the output voltage is higher than the input while it can be disabled for low quiescent current. Single switch supports the maximum current 2A for V_{INX}>1.8V.

The AW35206 is available in FOWLP package (0.35-mm pitch) and characterized for operation over the free-air temperature range of -40°C to 85°C.

TYPICAL APPLICATION CIRCUIT

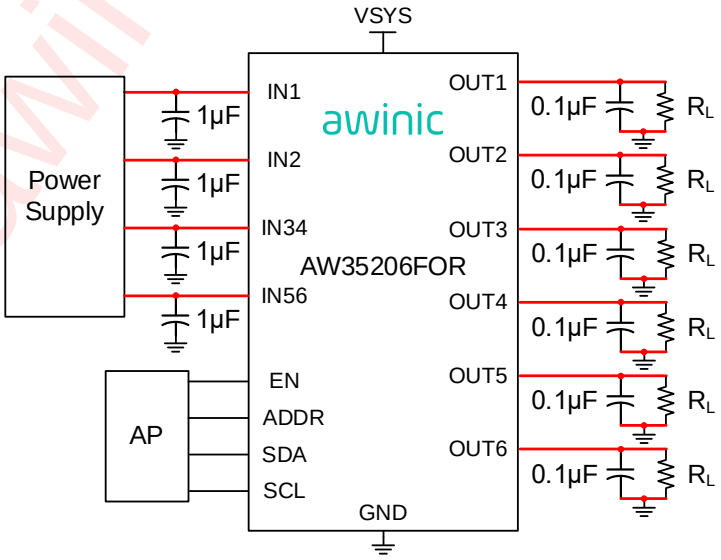


Figure 1 Typical application circuit of AW35206

PIN CONFIGURATION AND TOP MARK

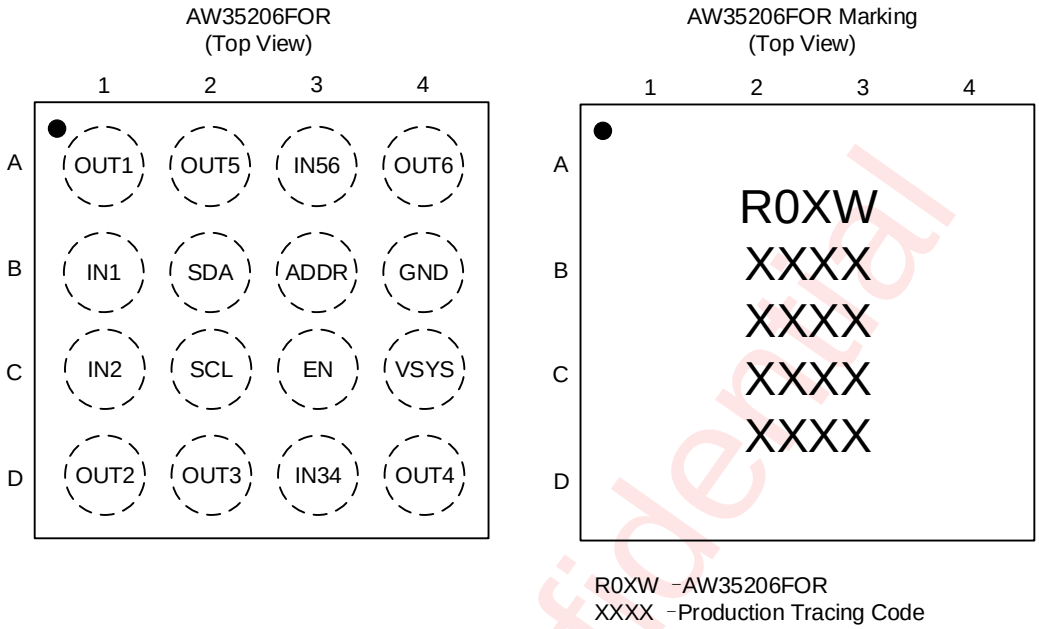
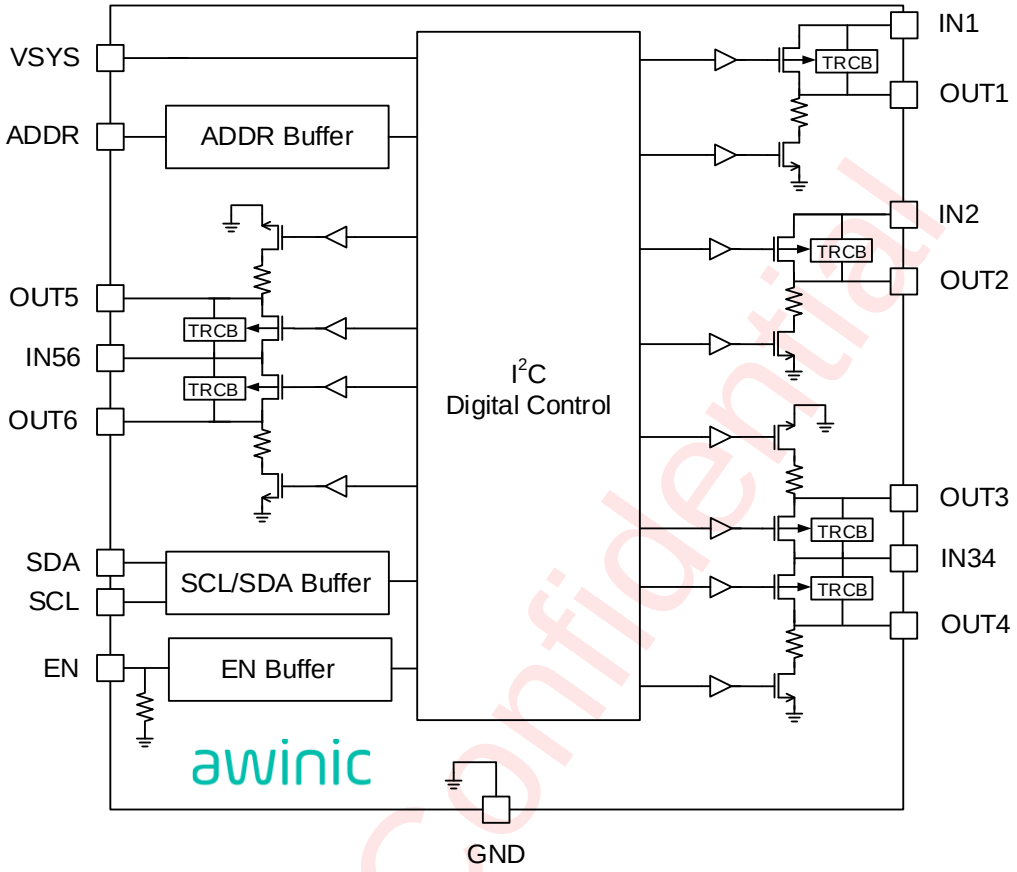


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
A1	OUT1	Load switch 1 output
A2	OUT5	Load switch 5 output
A3	IN56	Load switch 5 and 6 input
A4	OUT6	Load switch 6 output
B1	IN1	Load switch 1 input
B2	SDA	Serial data input or output
B3	ADDR	Device address pin
B4	GND	Device ground
C1	IN2	Load switch 2 input
C2	SCL	Serial clock input
C3	EN	Load switch enable pin (actively high)
C4	VSYS	Power supply to the device
D1	OUT2	Load switch 2 output
D2	OUT3	Load switch 3 output
D3	IN34	Load switch 3 and 4 input
D4	OUT4	Load switch 4 output

FUNCTIONAL BLOCK DIAGRAM



NOTE: TRCB is "True Reverse Current Blocking", this block cuts off current when V_{OUT} > V_{IN} if this function is enabled by I²C.

Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

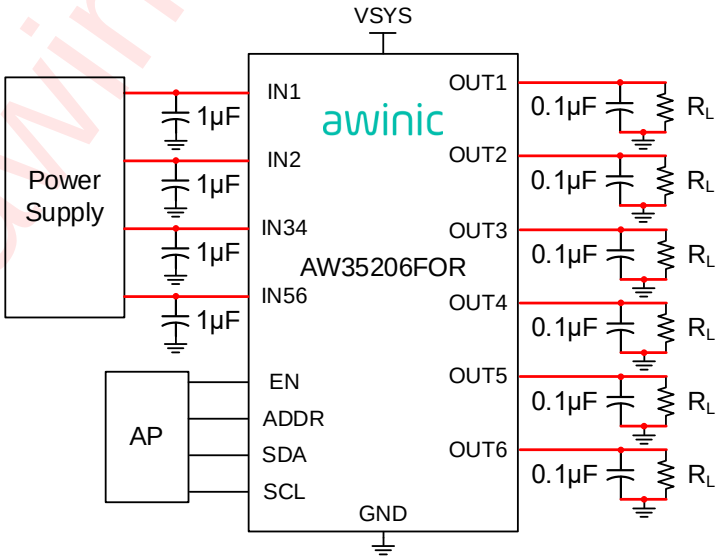


Figure 4 Typical Application circuit of AW35206

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35206FOR	-40°C~85°C	FOWLP 1.50mm×1.50mm×0.495mm-16B	R0XW	MSL1	ROHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Power IN/OUT Pins and Supply Pin Voltage Range	IN1, IN2, IN34, IN56, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, VSYS	-0.3V to 6V
Other Pins Voltage Range	EN, ADDR, SCL, SDA	-0.3V to V_{VSYS}+0.3V
Each Load Switch Maximum Continuous Current for V_{INX}>1.8V (NOTE 2)		2A
Maximum Peak Switch Current for V_{INX}>2V (NOTE 3)		2.5A
Junction-to-ambient Thermal Resistance θ_{JA}(NOTE 4)		122°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD & Latch-Up		
HBM (Human Body Model) (NOTE 5)		±2kV
CDM(Charged Device Model) (NOTE 6)		±1.5kV
Latch-Up(NOTE 7)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE7: Test Condition: JESD78E.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{VSYS}	VSYS voltage	1.5		5.5	V
V_{IN}	Input voltage	1.2		5.5	V
V_{OUT}	Output voltage	0		V_{IN}	V
V_{EN}	EN voltage	0		5.5	V
V_{ADDR}	ADDR voltage	0		5.5	V
V_{SCL}/V_{SDA}	SCL/SDA voltage	0		5.5	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance		0.1		μF

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

V_{VSYS}=1.8V, V_{INX}=3.3V, R_L=150Ω, C_{IN}=1μF, C_{OUT}=0.1μF, T_A=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
POWER SUPPLY CURRENTS AND LEAKAGES							
I_{Q_VSYS}	Quiescent current for VSYS when reverse current blocking of all channels off	V_{VSYS}=V_{EN}=5.0V, all switches on			0.3	0.5	μA
		V_{VSYS}=V_{EN}=3.3V, all switches on			0.2	0.5	
		V_{VSYS}=V_{EN}=1.8V, all switches on			0.1	0.5	
I_{QB_VSYS}	Quiescent current for VSYS when reverse current blocking of all channels on	V_{VSYS}=V_{EN}=5.0V, all switches on			1.9	4	μA
		V_{VSYS}=V_{EN}=3.3V, all switches on			1.5	3	
		V_{VSYS}=V_{EN}=1.8V, all switches on			1.1	2	
I_{SD_VSYS}	Shutdown current for VSYS	V_{VSYS}=V_{SDA}=V_{SCL}=5.0V, V_{EN}=0V			10	500	nA
		V_{VSYS}=V_{SDA}=V_{SCL}=3.3V, V_{EN}=0V			3	200	
		V_{VSYS}=V_{SDA}=V_{SCL}=1.8V, V_{EN}=0V			2	150	
I_{Q_INX}	Quiescent current for the input of any channel when reverse current blocking off	V_{INX}=5.0V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			125	550	nA
		V_{INX}=3.3V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			30	500	
		V_{INX}=1.8V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			5	150	
I_{QB_INX}	Quiescent current for the input of any channel when reverse current blocking on	V_{INX}=5.0V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			0.62	1.5	μA
		V_{INX}=3.3V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			0.49	1.3	
		V_{INX}=1.8V, V_{VSYS}=V_{EN}=1.8V, I_{OUTX}=0A			0.47	1.2	
I_{SD_INX}	Shutdown current for the input of any channel	V_{INX}=5.0V, V_{VSYS}=1.8V, V_{EN}=0V	T_A=25°C		30	800	nA
			T_A=85°C		390		
		V_{INX}=3.3V, V_{VSYS}=1.8V, V_{EN}=0V	T_A=25°C		6	500	
			T_A=85°C		143		
		V_{INX}=1.8V, V_{VSYS}=1.8V, V_{EN}=0V	T_A=25°C		2	400	
			T_A=85°C		115		
I_{EN}	EN leakage current	V_{VSYS}=1.5V~5.5V, V_{EN}=0V~5.5V				0.3	μA
I_{ADDR}	ADDR leakage current	V_{VSYS}=1.5V~5.5V, V_{ADDR}=0V~5.5V				0.3	μA
I_{SCL}	SCL leakage current	V_{VSYS}=1.5V~5.5V, V_{SCL}=5V				0.1	μA
I_{SDA}	SDA leakage current	V_{VSYS}=1.5V~5.5V, V_{SDA}=5V				0.1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	on-state resistance of any channel	V_{INX}=5.0V, I_{OUTX}=200mA			56	80	mΩ
		V_{INX}=3.3V, I_{OUTX}=200mA			71	100	
		V_{INX}=1.8V, I_{OUTX}=200mA			122	150	
R_{PD}	OUT port discharge resistance	V_{VSYS}=1.8V, V_{IN}=3.3V, V_{OUT}=1.0V			68		Ω

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{EN}	EN pin pull-down resistance	V_{VSYS}=1.5V~5.5V	8			MΩ
R_{ADDR}	ADDR pin pull-down resistance	V_{VSYS}=1.5V~5.5V	8			MΩ
THERSHOLD CHARACTERISTICS						
V_{IH}	High-level input voltage for EN/ADDR		1.0			V
V_{IL}	Low-level input voltage for EN/ADDR				0.4	V
TRUE REVERSE CURRENT BLOCKING CHARACTERISTICS						
V_{T_RCB}	RCB protection trip point	V_{IN}=3.3V, V_{T_RCB}=V_{OUT}-V_{INX}		70	125	mV
V_{R_RCB}	RCB protection release point	V_{IN}=3.3V, V_{R_RCB}=V_{INX}-V_{OUT}		70	105	mV
V_{H_RCB}	RCB hysteresis voltage	V_{IN}=3.3V, V_{H_RCB}= V_{T_RCB}+V_{R_RCB}		140		mV
I_{SD_OUT}	Shutdown current for OUT when RCB on	V_{IN}=0V, V_{OUT}=3.3V		280		nA
I^2C CHARACTERISTICS						
V_{IH_IIC}	High-level input voltage for SCL/SDA		1.0			V
V_{IL_IIC}	Low-level input voltage for SCL/SDA				0.4	V
V_{OL_SDA}	Low output voltage for SDA	I_{Sink_SDA}=3mA			0.3	V
f_{SCL}	Clock frequency			400		kHz

Switch Characteristics(NOTE1)

V_{VSYS}=1.8V, V_{INX}=3.3V, R_L=150Ω, C_{OUT}=0.1μF, T_A=25°C

PARAMETER		REG04h[x]=0 REG09h[x]=0	REG04h[x]=1 REG09h[x]=0	REG04h[x]=0 REG09h[x]=1	REG04h[x]=1 REG09h[x]=1	UNIT
		TYP	TYP	TYP	TYP	
t_{ON}	Turn-on delay	512	56	244	1571	μs
t_{OFF}	Turn-off delay	4	4	6	4	μs
t_R	V_{OUT} rising time	380	46	175	1100	μs
t_F	V_{OUT} falling time	12	10	13	12	μs

V_{VSYS}=1.8V, V_{INX}=3.3V, R_L=500Ω, C_{OUT}=0.1μF, T_A=25°C

PARAMETER		REG04h[x]=0 REG09h[x]=0	REG04h[x]=1 REG09h[x]=0	REG04h[x]=0 REG09h[x]=1	REG04h[x]=1 REG09h[x]=1	UNIT
		TYP	TYP	TYP	TYP	
t_{ON}	Turn-on delay	472	54	223	1487	μs
t_{OFF}	Turn-off delay	5	4	6	5	μs
t_R	V_{OUT} rising time	364	39	165	1026	μs
t_F	V_{OUT} falling time	14	11	17	15	μs

NOTE1: x=0,1,2,3,4,5.

TIMING DIAGRAM

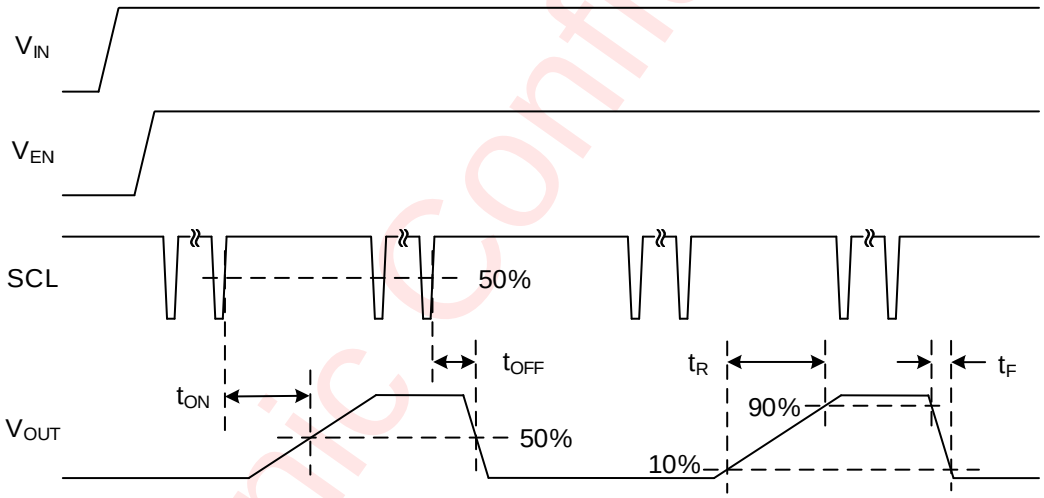


Figure 5 AW35206 Timing Diagram

I2C INTERFACE TIMING

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock Frequency				400	kHz
$t_{DEGLITCH}$	Deglitch Time	SCL		83		ns
		SDA		115		ns
$t_{HD:STA}$	(Repeat-Start) Start Condition Hold Time		0.6			μs
t_{LOW}	Low Level Width of SCL		1.3			μs
t_{HIGH}	High Level Width of SCL		0.6			μs
$t_{SU:STA}$	(Repeat-Start) Start Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		0			μs
SYMBOL	**DESCRIPTION**		**MIN**	**TYP**	**MAX**	**UNIT**
$t_{SU:DAT}$	Data Setup Time		0.1			μs
t_R	Rising Time of SDA and SCL				0.3	μs
t_F	Falling Time of SDA and SCL				0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{BUF}	Time Between Start and Stop Condition		1.3			μs

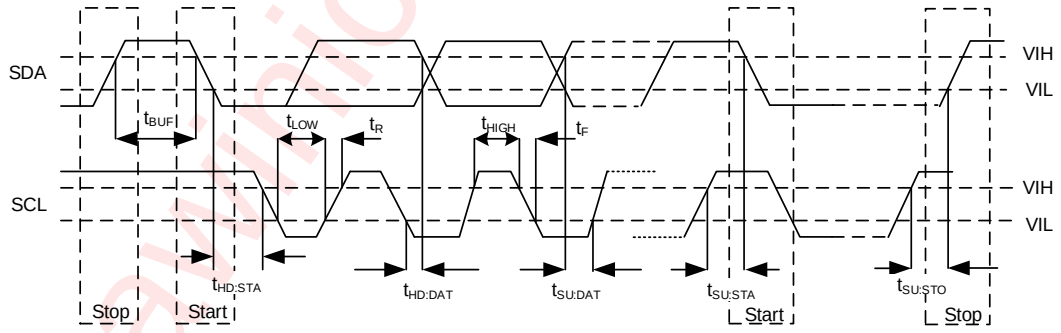


Figure 6 I²C Interface Timing

TYPICAL CHARACTERISTICS

Ambient temperature is 25°C, C_{IN} = 1μF, C_{OUT} = 0.1μF, unless otherwise noted.

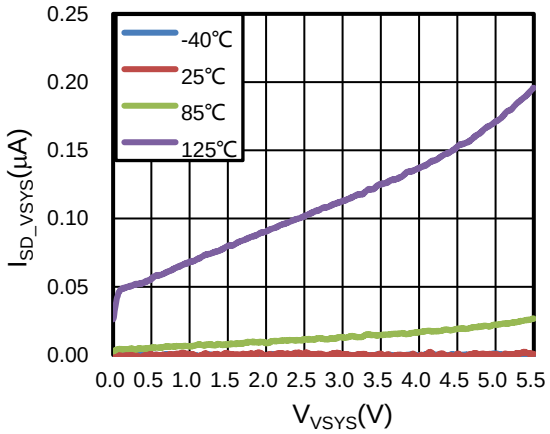


Figure 7 I_{SD_VSYS} vs. V_{VSYS}

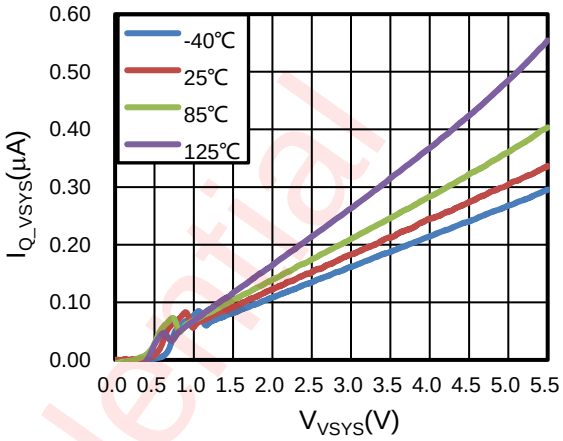


Figure 8 I_{Q_VSYS} vs. V_{VSYS}

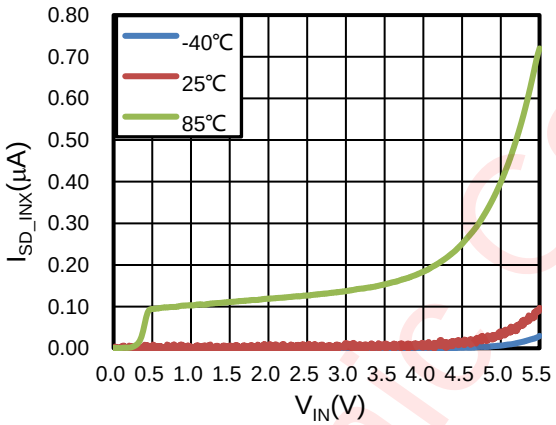


Figure 9 I_{SD_INX} vs. V_{IN}

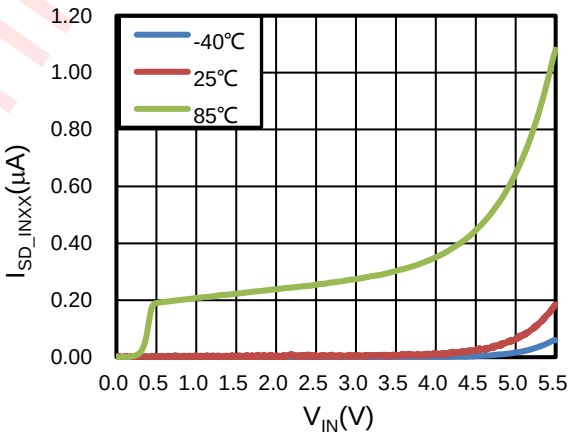


Figure 10 I_{SD_INXX} vs. V_{IN}

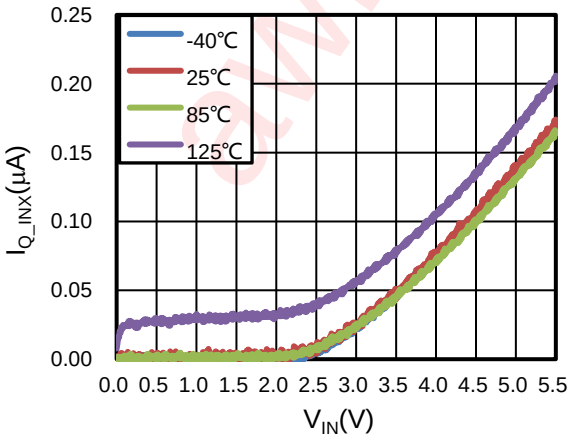


Figure 11 I_{Q_INX} vs. V_{IN} (V_{VSYS}=1.5V)

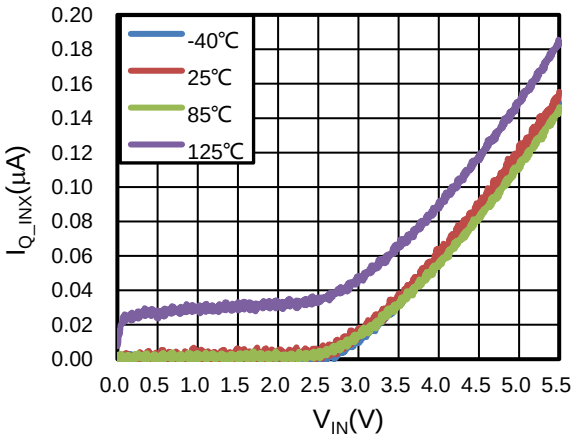


Figure 12 I_{Q_INX} vs. V_{IN} (V_{VSYS}=1.8V)

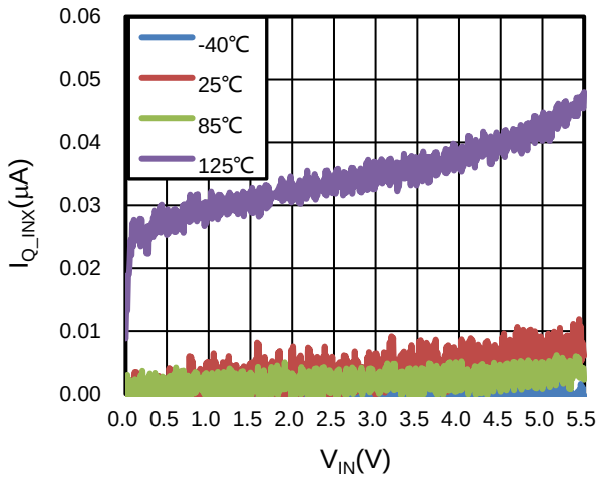


Figure 13 I_{Q_INX} vs. V_{IN} (V_{VSYS}=5.5V)

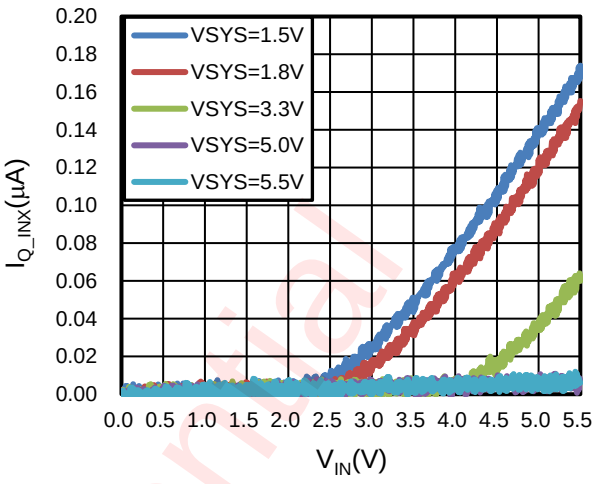


Figure 14 I_{Q_INX} vs. V_{IN} (T_A=25°C)

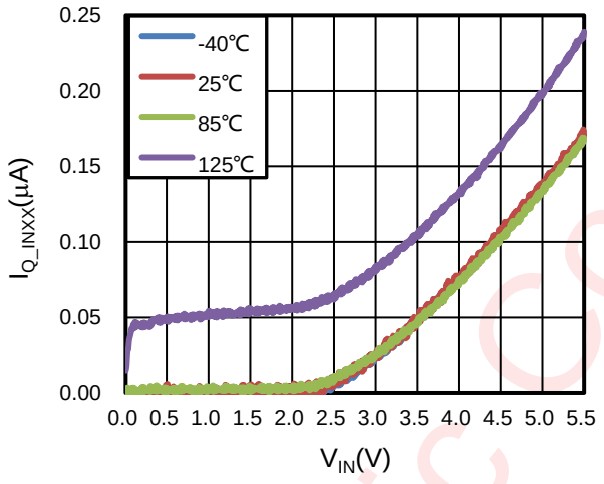


Figure 15 I_{Q_INXX} vs. V_{IN} (V_{VSYS}=1.5V)

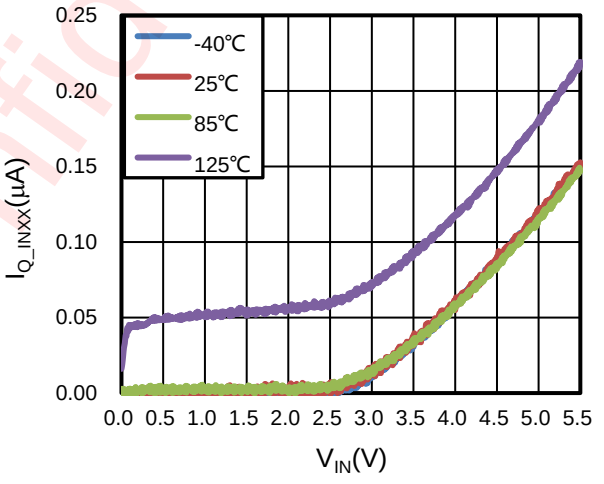


Figure 16 I_{Q_INXX} vs. V_{IN} (V_{VSYS}=1.8V)

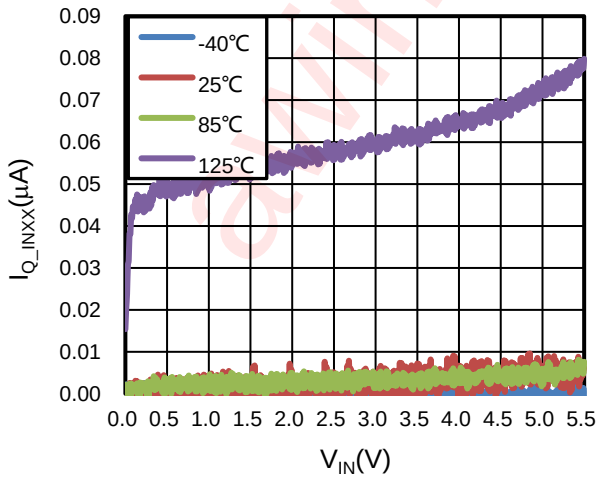


Figure 17 I_{Q_INXX} vs. V_{IN}(V_{VSYS}=5.5V)

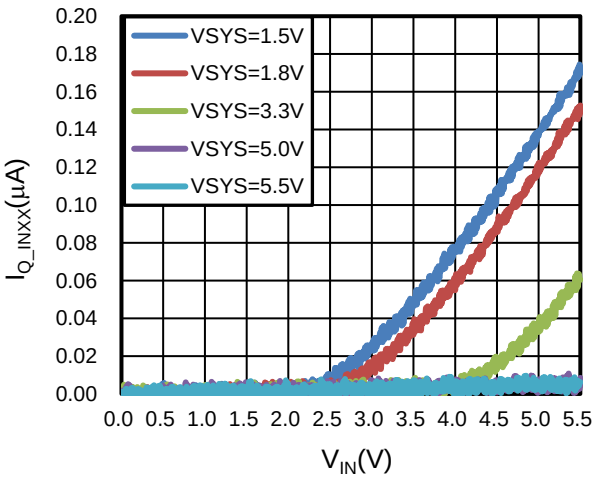


Figure 18 I_{Q_INXX} vs. V_{IN}(T_A=25°C)

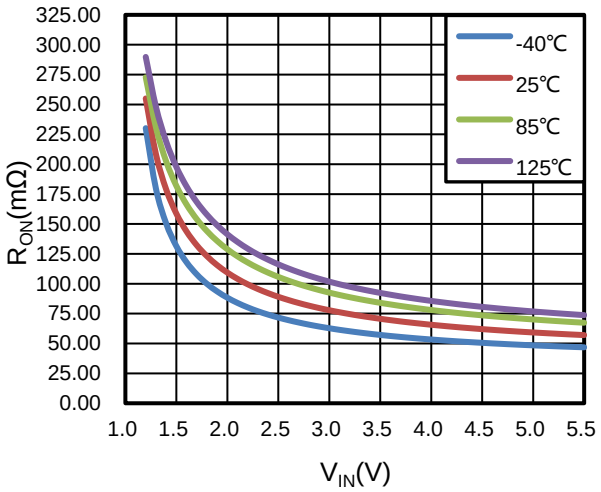


Figure 19 R_{ON} vs. V_{IN} (I_{OUT}=200mA)

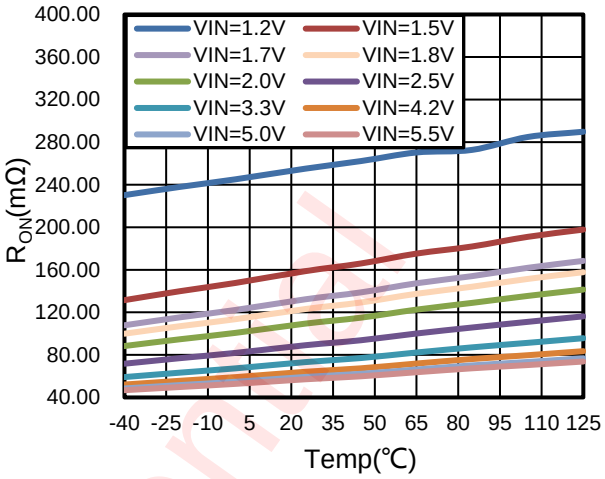


Figure 20 R_{ON} vs. Temperature (I_{OUT}=200mA)

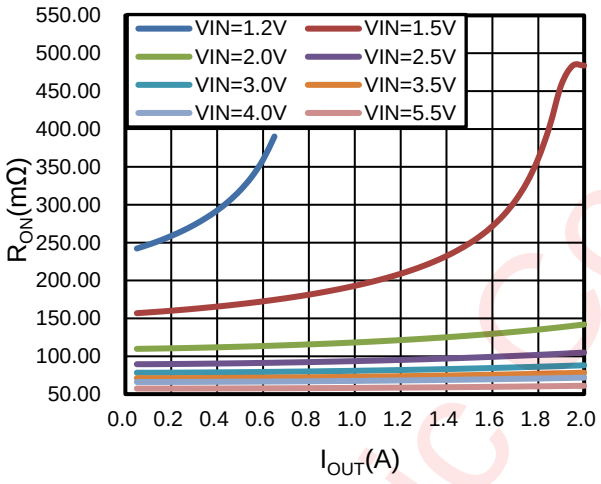


Figure 21 R_{ON} vs. I_{OUT} (T_A=25°C)

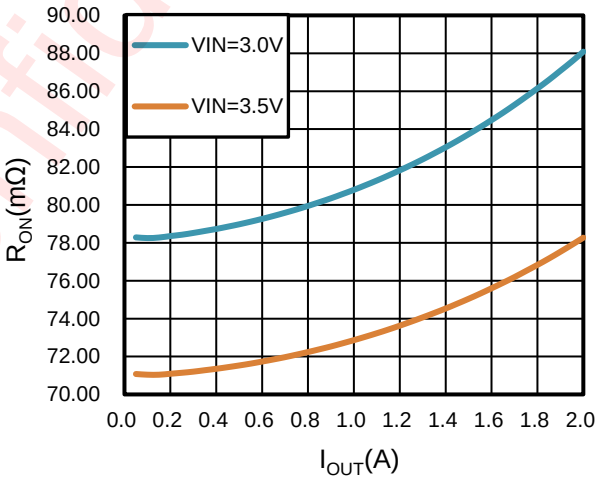
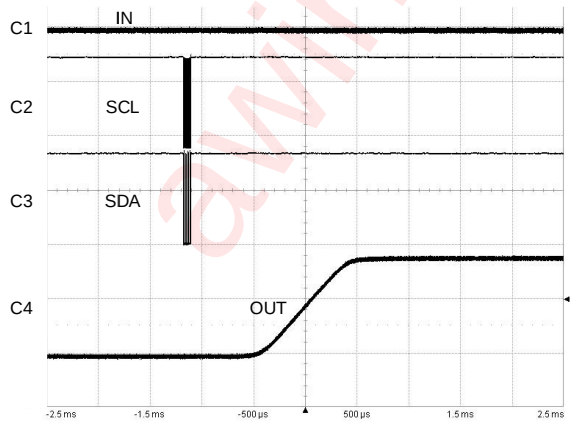


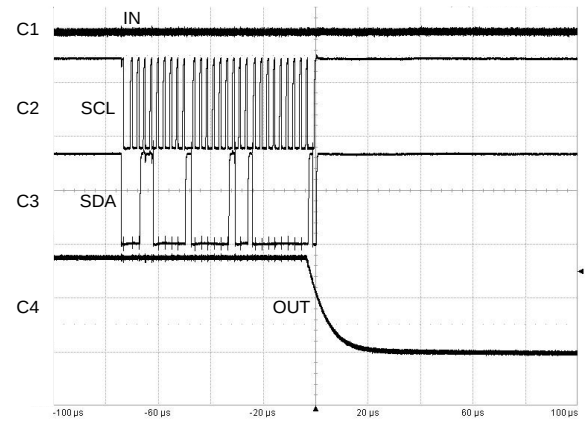
Figure 22 R_{ON} vs. I_{OUT} (T_A=25°C)



C1: 2.00V/div C2: 2.00V/div t=500µs/div
C3: 2.00V/div C4: 1.00V/div

V_{IN}=1.8V, C_{IN}=1µF, C_{OUT}=0.1µF, R_L=150Ω

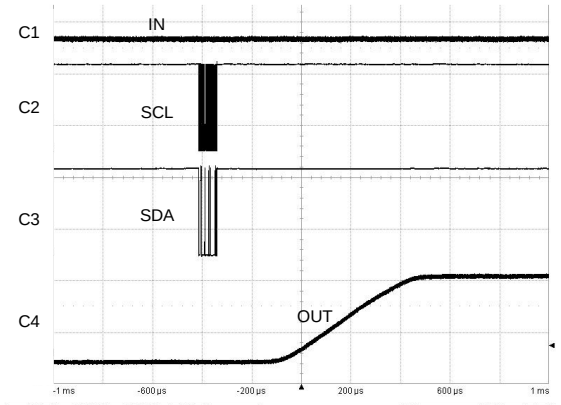
Figure 23 Turn On Response



C1: 2.00V/div C2: 2.00V/div t=20µs/div
C3: 2.00V/div C4: 1.00V/div

V_{IN}=1.8V, C_{IN}=1µF, C_{OUT}=0.1µF, R_L=150Ω

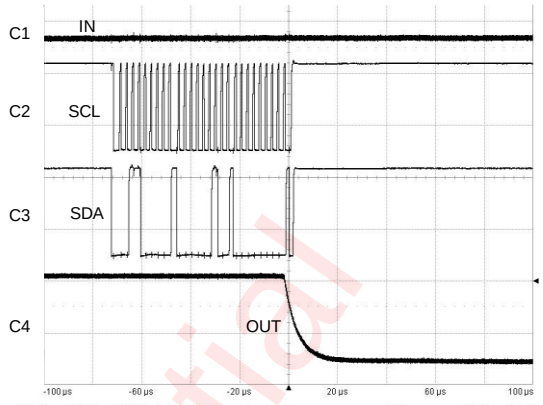
Figure 24 Turn Off Response



C1: 2.00V/div C2: 2.00V/div t=200μs/div
C3: 2.00V/div C4: 2.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

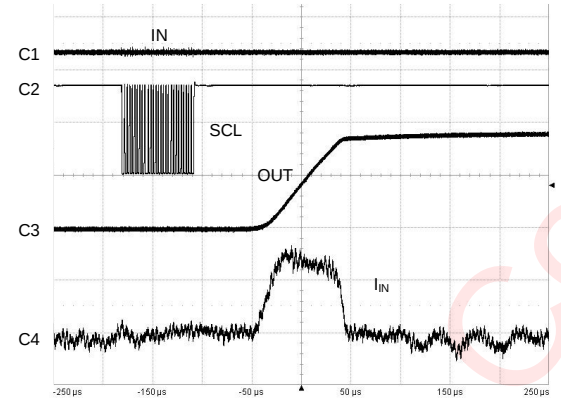
Figure 25 Turn On Response



C1: 2.00V/div C2: 2.00V/div t=20μs/div
C3: 2.00V/div C4: 2.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

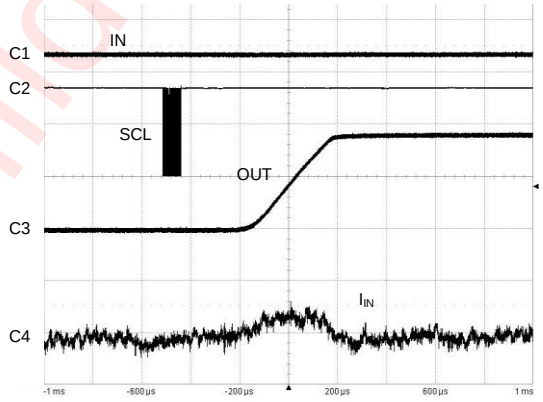
Figure 26 Turn Off Response



C1: 1.00V/div C2: 2.00V/div t=50μs/div
C3: 1.00V/div C4: 2.0mA/div

V_{IN}=1.8V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

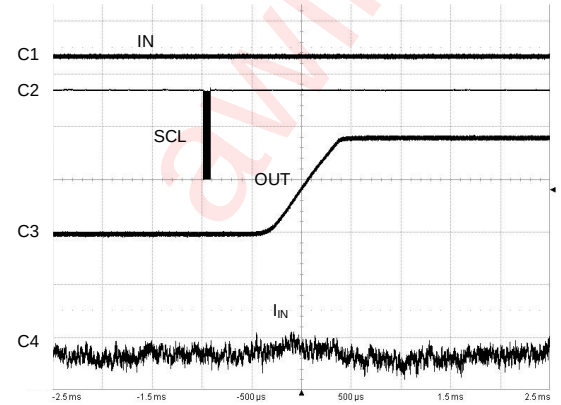
Figure 27 Inrush Current (ldsw_tr1/0=01)



C1: 1.00V/div C2: 2.00V/div t=200μs/div
C3: 1.00V/div C4: 2.0mA/div

V_{IN}=1.8V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

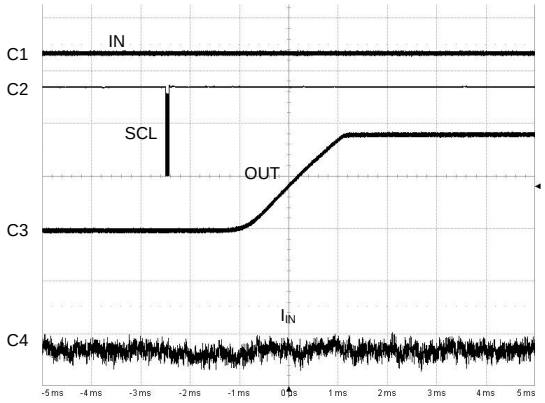
Figure 28 Inrush Current (ldsw_tr1/0=10)



C1: 1.00V/div C2: 2.00V/div t=500μs/div
C3: 1.00V/div C4: 2.0mA/div

V_{IN}=1.8V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

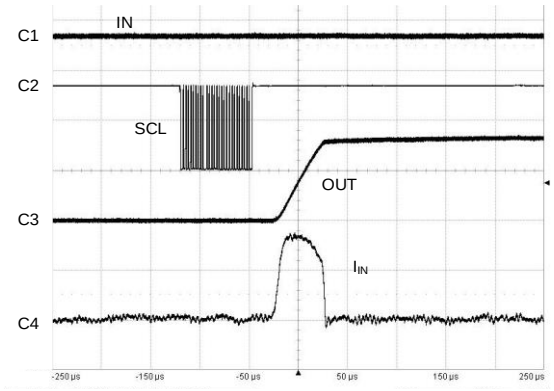
Figure 29 Inrush Current (ldsw_tr1/0=00)



C1: 1.00V/div C2: 2.00V/div t=1ms/div
C3: 1.00V/div C4: 2.0mA/div

V_{IN}=1.8V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

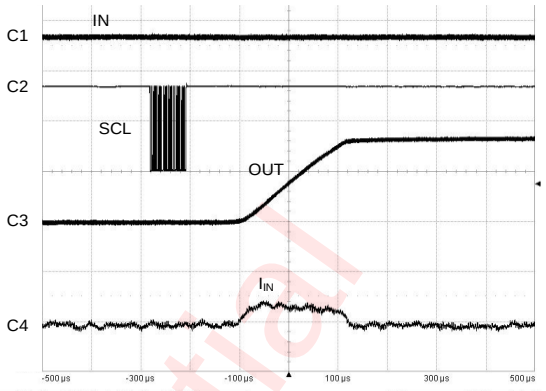
Figure 30 Inrush Current (ldsw_tr1/0=11)



C1: 2.00V/div C2: 2.00V/div t=50μs/div
C3: 2.00V/div C4: 5.0mA/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

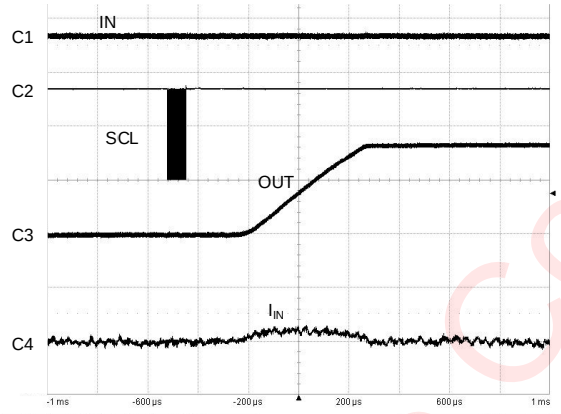
Figure 31 Inrush Current (Idsw_tr1/0=01)



C1: 2.00V/div C2: 2.00V/div t=100μs/div
C3: 2.00V/div C4: 5.0mA/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

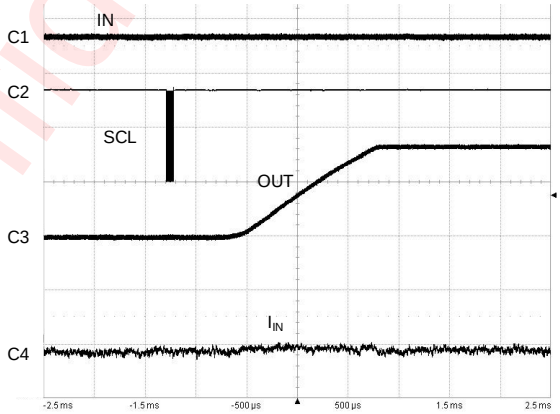
Figure 32 Inrush Current (Idsw_tr1/0=10)



C1: 2.00V/div C2: 2.00V/div t=200μs/div
C3: 2.00V/div C4: 5.0mA/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

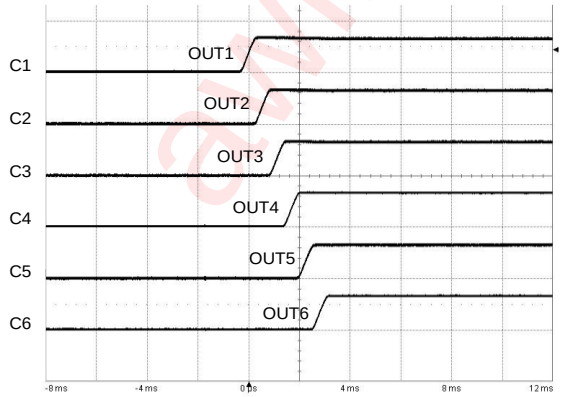
Figure 33 Inrush Current (Idsw_tr1/0=00)



C1: 2.00V/div C2: 2.00V/div t=200μs/div
C3: 2.00V/div C4: 5.0mA/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, no R_L

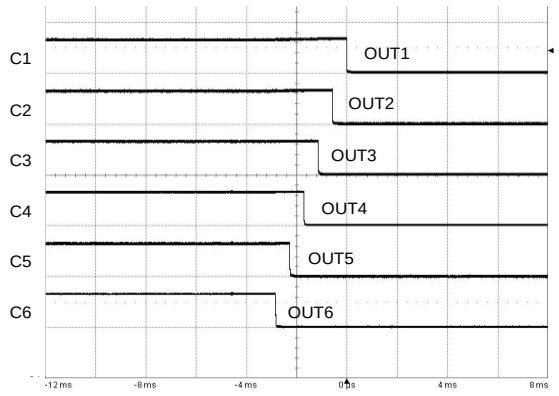
Figure 34 Inrush Current (Idsw_tr1/0=11)



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=2.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF，R_L=150Ω

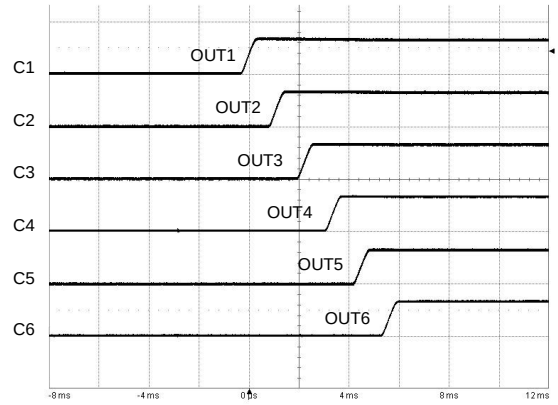
Figure 35 Power up with seq_speed<1:0>=00



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=2.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF，R_L=150Ω

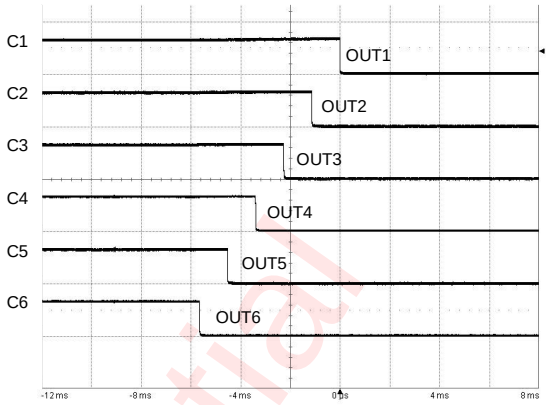
Figure 36 Power down with seq_speed<1:0>=00



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=2.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

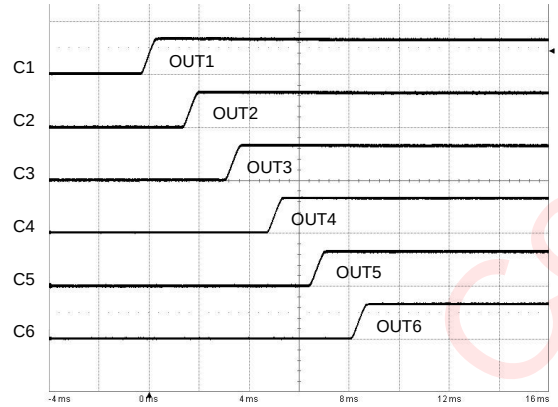
Figure 37 Power up with seq_speed<1:0>=01



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=2.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

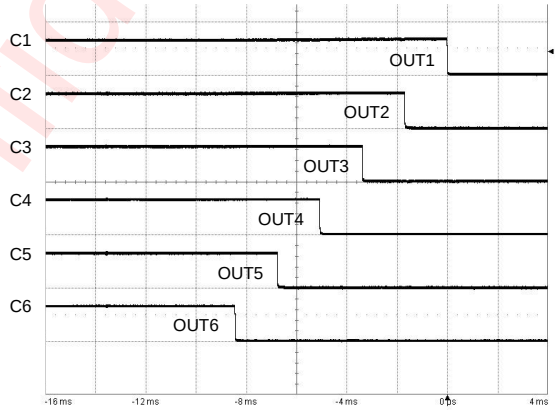
Figure 38 Power down with seq_speed<1:0>=01



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=4.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

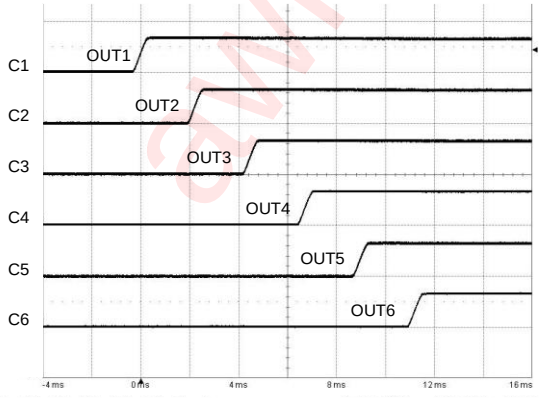
Figure 39 Power up with seq_speed<1:0>=10



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=4.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

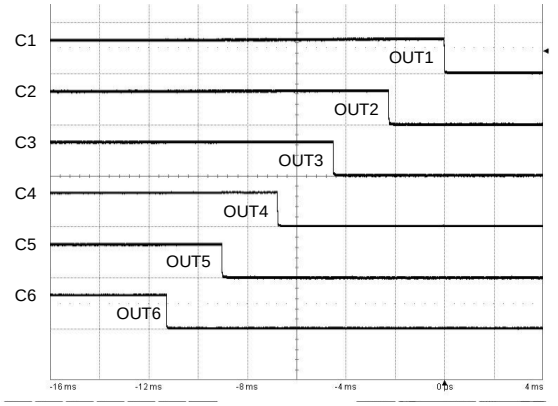
Figure 40 Power down with seq_speed<1:0>=10



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=4.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

Figure 41 Power up with seq_speed<1:0>=11



C1: 5.00V/div C2: 5.00V/div C3: 5.00V/div t=4.0ms/div
C4: 5.00V/div C5: 5.00V/div C6: 5.00V/div

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=150Ω

Figure 42 Power down with seq_speed<1:0>=11

DETAILED FUNCTIONAL DESCRIPTION

The AW35206 integrates six PMOS load switches, and provides a low on-resistance for a low voltage drop across the device. The supply voltage of the device is from 1.5V to 5.5V and the input of the load switch is 1.2V~5.5V. All channels are controlled through I²C BUS for processors. Each output integrates a selectable quick discharge function block for necessity. A controlled slew rate is used in applications to limit the inrush current. Any load switch has the ability to block reverse current when the output voltage is higher than the input. Also this function can be disabled by I²C for low quiescent current.

TURN ON/OFF CONTROL

All channels of the device are opened when EN pin is tied low (disable) or pulled down by internal 12MΩ resistor, forcing PMOS switch off. The IN/OUT path is activated under a minimum input voltage of 1.2V if the corresponding channel is closed. Each load switch of the AW35206 can be enabled in two ways using the I²C interface if the EN pin is pulled high.

1. Setting ldswx_seq<2:0>=000 in 0x05(LDSW12_SEQ) or 0x06(LDSW34_SEQ) or 0x07(LDSW56_SEQ), making ldswx_en=1 assigned to the load switch in register can enable the corresponding channel otherwise disable it.

Table 1. Functional Table when LDSWXX_SEQ Registers are 0x00

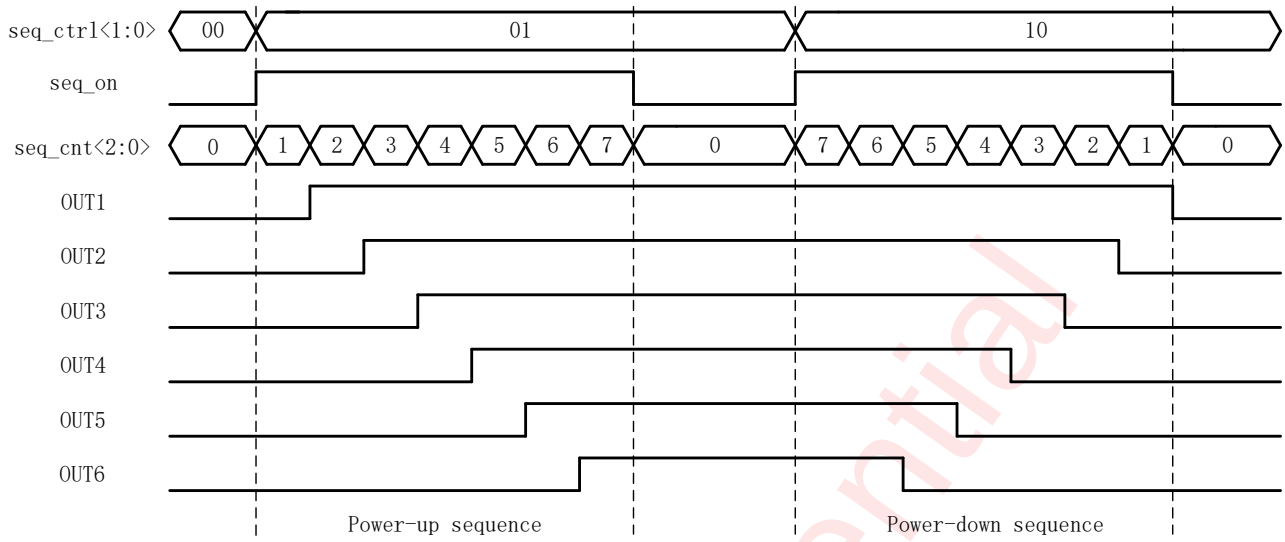
EN	ldswx_en	INX to OUTX
Low	-	OFF
High	Low	OFF
	High	ON

2. Setting ldswx_seq<2:0>≠000 in 0x05(LDSW12_SEQ) or 0x06(LDSW34_SEQ) or 0x07(LDSW56_SEQ), the corresponding load switch is controlled by power sequence in the register “SEQ_CTR”.

   Writing “01” in seq_ctrl<1:0> when seq_on=“0” executes a power-up sequence and seq_cnt<2:0> will increase from “000” to “111”, and the value of the seq_cnt<2:0> is defined as slot. The bit seq_on will be set “1” until the power-up sequence is finished, the load switch x turns on when the value of seq_cnt<2:0> equals that of ldswx_seq<2:0> after the time interval set by seq_speed<1:0>. Seq_on will be reset to “0” after seq_cnt<2:0> finishes an increasing counting and seq_cnt<2:0> is also reset to “000”, which indicates the power-up sequence is over.

   Similarly, a power-down sequence is triggered when the seq_ctrl<1:0> is wrote “10”, and seq_cnt<2:0> will decrease from “111” to “000”. The bit seq_on will be set “1” until the power-down sequence is finished, the load switch x turns off when the value of seq_cnt<2:0> equals that of ldswx_seq<2:0> after the time interval defined by seq_speed<1:0>. Seq_on will be reset to “0” after seq_cnt<2:0> finishes a decreasing counting and seq_cnt<2:0> is also reset to “000”, which indicates the power-down sequence is over.

   A typical power-up/down sequence is illustrated in the figure 43 below, provided voltages of all the input pins are good enough.



NOTE: The register bit ldswx_seq<2:0>(x=1,2,…,6) is set "001" to "110" by I²C interface.

Figure 43 A typical power-up/down sequence

SLEW RATE CONTROL

When the switch is enabled, the device regulates the gate voltage of MOSFET, and controls the V_{OUT} slew rate during t_R to avoid a large input inrush current. The rising time of the V_{OUT} can be set in four levels through I²C BUS. The feature reduces the interference to the power supply.

QUICK OUTPUT DISCHARGE

The AW35206 includes the Quick Output Discharge (QOD) feature for the output of every load switch, in order to discharge the application capacitor connected on OUT pin. This function can be disabled by I²C and is turned on by default. When EN pin or the control bit in register LDSW_EN is set to low level (disable state), a discharge resistance with a typical value of 68Ω connected between the output and ground, pulls down the output and prevents it from floating.

REVERSE CURRENT BLOCKING

The AW35206 integrates a function block that can block reverse current for each load switch, which can prevent the current from flowing through the P-FET or the body diode when the output voltage is higher than the input. This ability can be turned off for low current consumption in the register LDSW_RCB.

GENERAL I²C OPERATION

The AW35206 is compatible with I²C interface. The SCL line is an input and the SDA line is a bi-directional open-drain output. The I²C salve address of AW35206 is 0011000b (ADDR pin connected to GND) or 0011001b (ADDR pin connected to VSYS). The I²C interface is accessible as long as the supply voltage is above 1.5V.

Table 2. Device Address

A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	ADDR	R/W

ADDR=0: slave address=0x18H;

ADDR=1: slave address=0x19H.

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

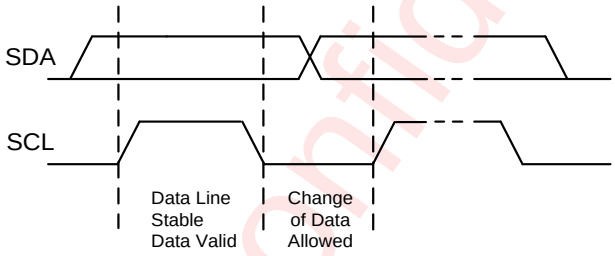


Figure 44 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

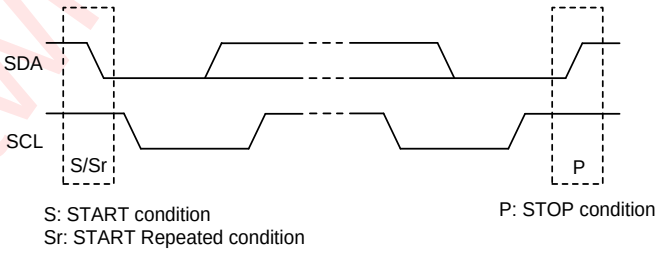


Figure 45 Start and Stop Conditions

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

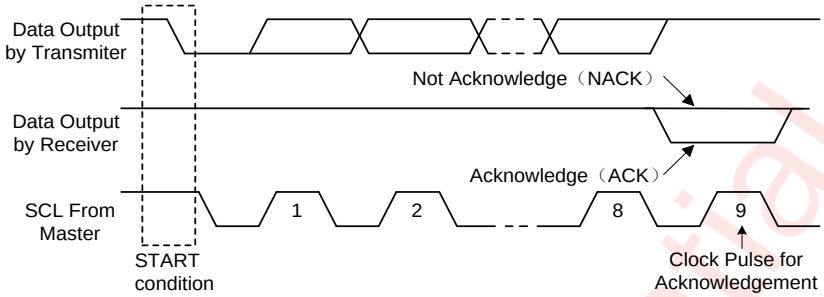


Figure 46 Acknowledgement Diagram

WRITE PROCESS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat steps f and g)

i) Master generates STOP condition to indicate write cycle end

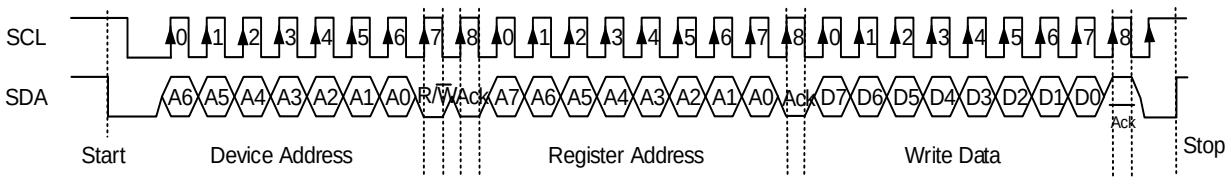


Figure 47 I²C Write Timing

READ PROCESS

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

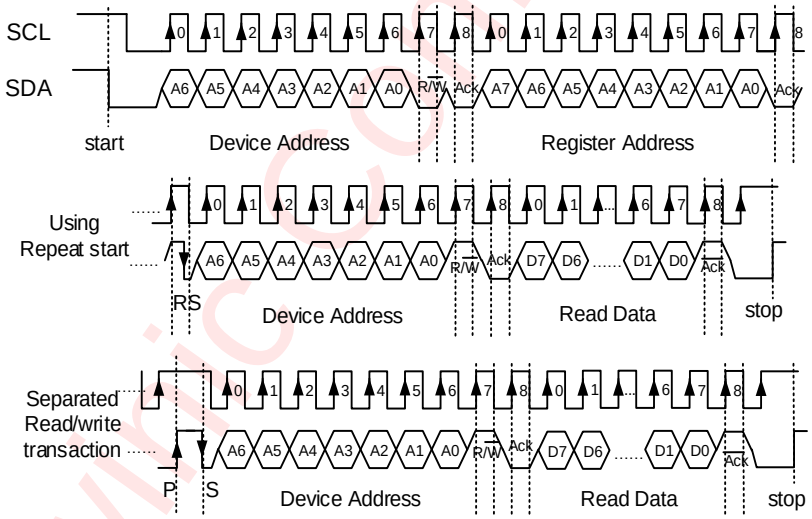


Figure 48 I²C Read Timing

APPLICATION INFORMATION

POWER SUPPLY RECOMMENDATIONS

The device is designed to operate with a V_{VSYS} range of 1.5V to 5.5V while the input voltage of each load switch is 1.2V~5.5V. The supply must be well regulated and placed as close to the device VSYS terminal as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of 1μF if necessary. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10μF may be sufficient.

MANAGING INRUSH CURRENT

When the switch is enabled, the output capacitors must be charged up from 0V to V_{IN}. An input inrush current will appear. The Inrush current can be calculated using Equation 1:

$$I_{inrush} = C_{OUT} \frac{dV_{OUT}}{dt} \quad (1)$$

where:

- C_{OUT} = Output capacitance
- dV_{OUT} = Change of output voltage, equals to V_{IN}
- dt = Rise time t_R.

The AW35206 offers a controlled slew rate for minimizing inrush current.

POWER DISSIPATION

The power dissipation produced by the power MOSFET in on-state can be calculated with the following equation:

$$P_D = R_{ON} \times I_{OUT}^2 \quad (2)$$

Where:

- P_D = Power dissipation (W)
- R_{ON} = Power MOSFET on-state resistance (Ω)
- I_{OUT} = Output current (A)

THERMAL CONSIDERATIONS

Main contributor in term of junction temperature T_J(max) is the power dissipation, and T_J(max) should be restricted to 125˚C under on-state. Junction temperature is directly proportional to power dissipation in the device, it can be calculated by the following equation:

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Where:
- T_J = Junction temperature of the device
- T_A = Ambient temperature
- P_D = Power dissipation of the device
- $R_{\theta JA}$ = Junction to ambient thermal resistance. This parameter is highly dependent on board layout.

Register Configuration

Register List

ADDR	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00h	CHIPID	0	0	1	1	0	0	chip_id<1:0>		0x33
01h	VERID	0	0	0	0	0	0	ver_id<1:0>		0x00
02h	LDSW_EN	0	0	ldsw6_en	ldsw5_en	ldsw4_en	ldsw3_en	ldsw2_en	ldsw1_en	0x00
03h	LDSW_DIS	0	0	ldsw6_dis	ldsw5_dis	ldsw4_dis	ldsw3_dis	ldsw2_dis	ldsw1_dis	0x3F
04h	LDSW_TR0	0	0	ldsw6_tr0	ldsw5_tr0	ldsw4_tr0	ldsw3_tr0	ldsw2_tr0	ldsw1_tr0	0x00
05h	LDSW12_SEQ	0	0	ldsw2_seq<2:0>			ldsw1_seq<2:0>			0x00
06h	LDSW34_SEQ	0	0	ldsw4_seq<2:0>			ldsw3_seq<2:0>			0x00
07h	LDSW56_SEQ	0	0	ldsw6_seq<2:0>			ldsw5_seq<2:0>			0x00
08h	SEQ_CTR	seq_speed<1:0>		seq_ctrl<1:0>		seq_on	seq_cnt<2:0>			0x00
09h	LDSW_TR1	0	0	ldsw6_tr1	ldsw5_tr1	ldsw4_tr1	ldsw3_tr1	ldsw2_tr1	ldsw1_tr1	0x00
0Ah	LDSW_RCB	0	0	ldsw6_rcb	ldsw5_rcb	ldsw4_rcb	ldsw3_rcb	ldsw2_rcb	ldsw1_rcb	0x00
0Bh	LDSW_ON	0	0	ldsw6_on	ldsw5_on	ldsw4_on	ldsw3_on	ldsw2_on	ldsw1_on	0x00
69h	RSTN	0	0	0	0	0	0	0	0	0x00

Register Detailed Description

- **CHIPID: Chip ID register(Address 00h)**

Bit	Symbol	R/W	Description	Default
7:2	Chip_id<7:2>	R	The product ID with revision	001100
1:0	Chip_id<1:0>	R		11

- **VERID: Version ID register(Address 01h)**

Bit	Symbol	R/W	Description	Default
7:2	Ver_id<7:2>	R	The device ID with revision	000000
1:0	Ver_id<1:0>	R		00

- **LDSW_EN: Load switch enable register(Address 02h)**

This is load switch enable control register by I²C while the EN pin is pulled high. This register can be written to enable or disable the corresponding load switch.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5	Ldsw6_en	R/W	Load switch 6 control: 0: Disable 1: Enable	0
4	Ldsw5_en	R/W	Load switch 5 control: 0: Disable 1: Enable	0
3	Ldsw4_en	R/W	Load switch 4 control: 0: Disable 1: Enable	0

2	Ldsw3_en	R/W	Load switch 3 control: 0: Disable 1: Enable	0
1	Ldsw2_en	R/W	Load switch 2 control: 0: Disable 1: Enable	0
0	Ldsw1_en	R/W	Load switch 1 control: 0: Disable 1: Enable	0

- **LDSW_DIS: Load switch output discharge selecting register(Address 03h)**

This register sets the discharge function of each load switch output.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5	Ldsw6_dis	R/W	Load switch 6 discharge function: 0: Disable. OUT6 discharge will not be activated when load switch 6 is disabled by any event. 1: Enable. OUT6 discharge will be activated when load switch 6 is disabled.	1
4	Ldsw5_dis	R/W	Load switch 5 discharge function: 0: Disable. OUT5 discharge will not be activated when load switch 5 is disabled by any event. 1: Enable. OUT5 discharge will be activated when load switch 5 is disabled.	1
3	Ldsw4_dis	R/W	Load switch 4 discharge function: 0: Disable. OUT4 discharge will not be activated when load switch 4 is disabled by any event. 1: Enable. OUT4 discharge will be activated when load switch 4 is disabled.	1
2	Ldsw3_dis	R/W	Load switch 3 discharge function: 0: Disable. OUT3 discharge will not be activated when load switch 3 is disabled by any event. 1: Enable. OUT3 discharge will be activated when load switch 3 is disabled.	1
1	Ldsw2_dis	R/W	Load switch 2 discharge function: 0: Disable. OUT2 discharge will not be activated when load switch 2 is disabled by any event. 1: Enable. OUT2 discharge will be activated when load switch 2 is disabled.	1
0	Ldsw1_dis	R/W	Load switch 1 discharge function: 0: Disable. OUT1 discharge will not be activated when load switch 1 is disabled by any event. 1: Enable. OUT1 discharge will be activated when load switch 1 is disabled.	1

- **LDSW_TR0 & LDSW_TR1: Load switch output voltage rising time setting register(Address 04h & 09h)**

Typically, V_{INX} =3.3V, R_L=150Ω, C_{OUT}=0.1μF, T_A=25°C.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5	Ldsw6_tr1 Ldsw6_tr0	R/W	Load switch 6 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0
4	Ldsw5_tr1 Ldsw5_tr0	R/W	Load switch 5 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0
3	Ldsw4_tr1 Ldsw4_tr0	R/W	Load switch 4 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0
2	Ldsw3_tr1 Ldsw3_tr0	R/W	Load switch 3 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0
1	Ldsw2_tr1 Ldsw2_tr0	R/W	Load switch 2 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0
0	Ldsw1_tr1 Ldsw1_tr0	R/W	Load switch 1 output voltage (from 10% to 90%) rising time setting: 00: 380μs; 01: 46μs; 10: 175μs; 11: 1100μs	0/0

- **LDSW_SEQ12: Load switch power sequence setting register(Address 05h)**

There are 7 time slots for every load switch to turn on/off. The power-up sequence starts from slot1 to slot7, and the power-down sequence is on the contrary. Turning on and off of each load switch can be set at any time slot as defined below.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5:3	Ldsw2_seq<2:0>	R/W	000: Controlled by the bit ldsw2_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000
2:0	Ldsw1_seq<2:0>	R/W	000: Controlled by the bit ldsw1_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000

- **LDSW_SEQ34: Load switch power sequence setting register(Address 06h)**

There are 7 time slots for every load switch to turn on/off. The power-up sequence starts from slot1 to slot7, and the power-down sequence is on the contrary. Turning on and off of each load switch can be set at any time slot as defined below.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5:3	Ldsw4_seq<2:0>	R/W	000: Controlled by the bit ldsw4_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000
2:0	Ldsw3_seq<2:0>	R/W	000: Controlled by the bit ldsw3_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000

- **LDSW_SEQ56: Load switch power sequence setting register(Address 07h)**

There are 7 time slots for every load switch to turn on/off. The power-up sequence starts from slot1 to slot7, and the power-down sequence is on the contrary. Turning on and off of each load switch can be set at any time slot as defined below.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5:3	Ldsw6_seq<2:0>	R/W	000: Controlled by the bit ldsw6_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000
2:0	Ldsw5_seq<2:0>	R/W	000: Controlled by the bit ldsw5_en; 001: slot1; 010: slot2; 011: slot3; 100: slot4; 101: slot5; 110: slot6; 111: slot7	000

- **SEQ_CTR: Power sequence setting and status register(Address 08h)**

This register enables the power sequence function and reveals the relevant information at present.

Bit	Symbol	R/W	Description	Default
7:6	Seq_speed<1:0>	R/W	Time interval between two adjacent slots: 00: 0.5ms; 01: 1.0ms; 10: 1.5ms; 11: 2.0ms	00
5:4	Seq_ctrl<1:0>	R/W	Power sequence controlling bits: 00: Suspend the current sequence event 01: Execute a power-up sequence 10: Execute a power-down sequence 11: No effect Note: the chip responds once after writing to these two bits, which are always read out “00”.	00
3	Seq_on	R	Indicator of the power sequence: 0: Indicates that the sequence is not in progress	0

			1: Indicates that the chip is carrying out a power sequence and will return to “0” automatically after the sequence is finished.	
2:0	Seq_cnt<2:0>	R	Indicates the slot number at present: 000: Power Sequence is not in progress or has finished 001: slot 1 during the power sequence 010: slot 2 during the power sequence 011: slot 3 during the power sequence 100: slot 4 during the power sequence 101: slot 5 during the power sequence 110: slot 6 during the power sequence 111: slot 7 during the power sequence	000

- **LDSW_RCB: Load switch reserve current blocking function selecting register(Address 0Ah)**

This register enables the function that blocks the current of load switch when the output voltage is higher than input.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5	Ldsw6_rcb	R/W	Load switch 6 reverse current blocking function: 0: Disable; 1: Enable	0
4	Ldsw5_rcb	R/W	Load switch 5 reverse current blocking function: 0: Disable; 1: Enable	0
3	Ldsw4_rcb	R/W	Load switch 4 reverse current blocking function: 0: Disable; 1: Enable	0
2	Ldsw3_rcb	R/W	Load switch 3 reverse current blocking function: 0: Disable; 1: Enable	0
1	Ldsw2_rcb	R/W	Load switch 2 reverse current blocking function: 0: Disable; 1: Enable	0
0	Ldsw1_rcb	R/W	Load switch 1 reverse current blocking function: 0: Disable; 1: Enable	0

- **LDSW_ON: Load switch status indicator register(Address 0Bh)**

This register indicates the status (ON or OFF) of each load switch.

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R	Reserved	00
5	Ldsw6_on	R	Load switch 6 status indicator: 0: Off; 1: On	0
4	Ldsw5_on	R	Load switch 5 status indicator: 0: Off; 1: On	0
3	Ldsw4_on	R	Load switch 4 status indicator:	0

			0: Off; 1: On	
2	Ldsw3_on	R	Load switch 3 status indicator: 0: Off; 1: On	0
1	Ldsw2_on	R	Load switch 2 status indicator: 0: Off; 1: On	0
0	Ldsw1_on	R	Load switch 1 status indicator: 0: Off; 1: On	0

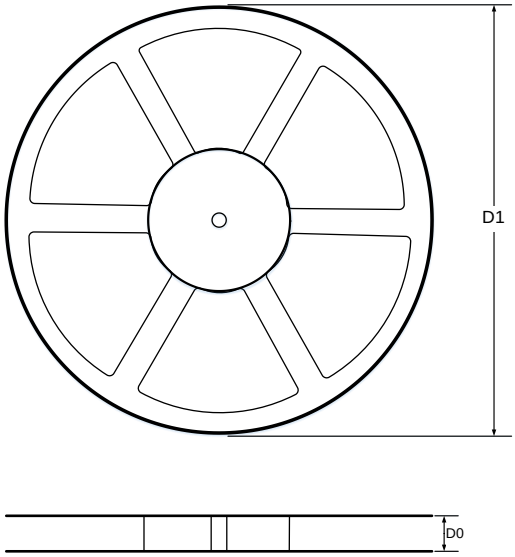
- **RSTN: Reset register(Address 69h)**

  Writing “0xAE” to this register can reset all registers and disable all load switches when the chip works out of control or other unusual circumstances come out.

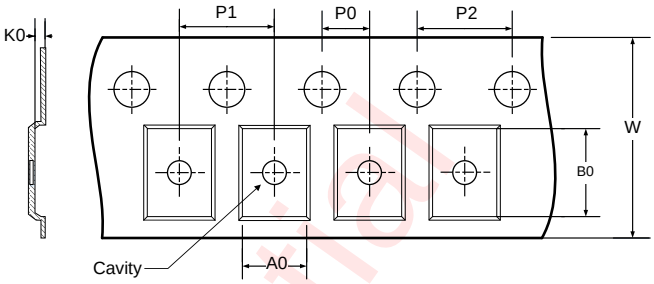
Bit	Symbol	R/W	Description	Default
7:0	Reserved	R/W	Read always 00 Write “0xAE” to reset all registers	00

TAPE AND REEL INFORMATION

REEL DIMENSIONS

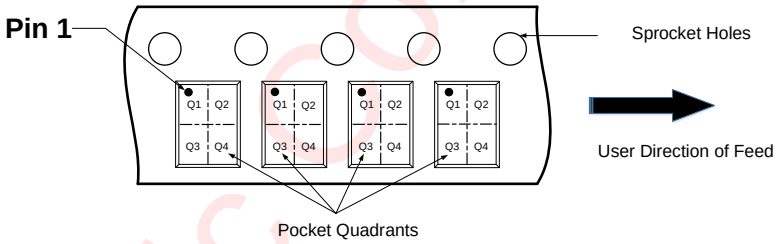


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



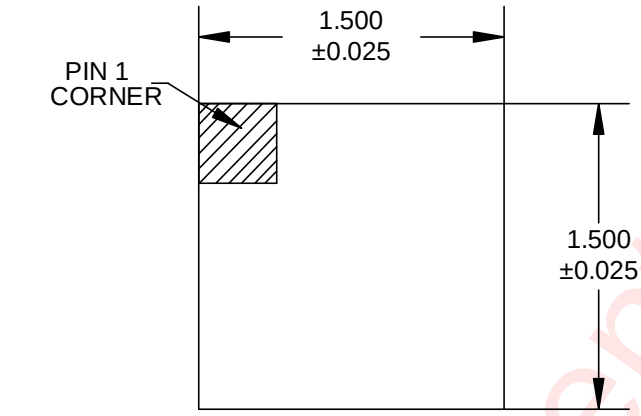
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

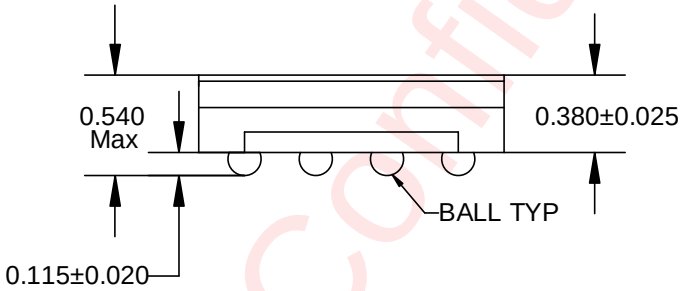
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.63	1.63	0.67	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

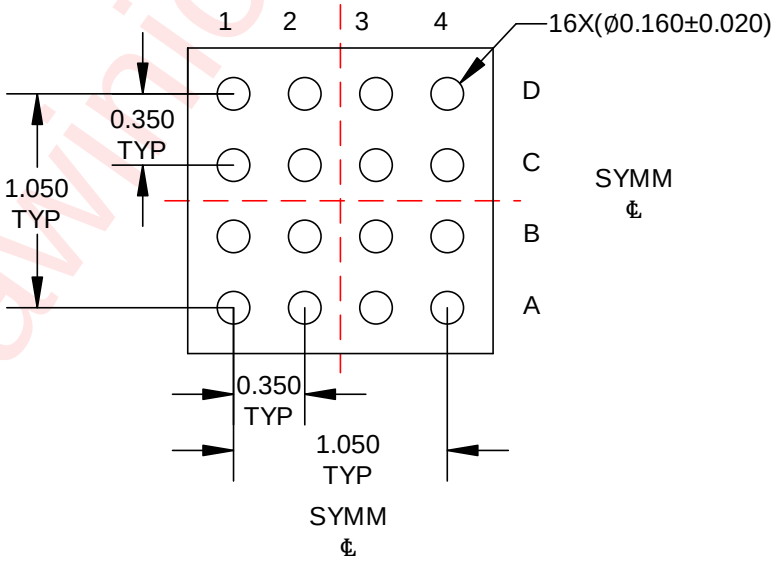
PACKAGE DESCRIPTION



Top View



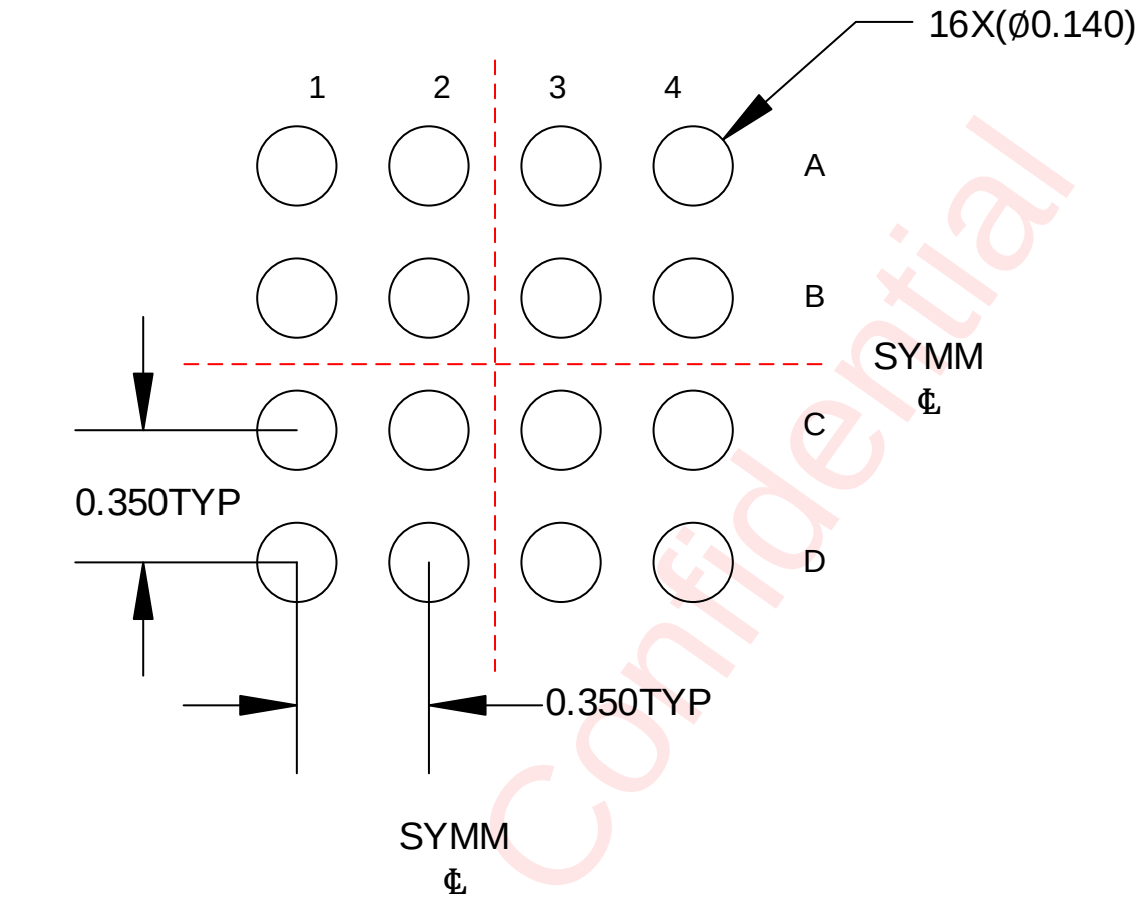
Side View

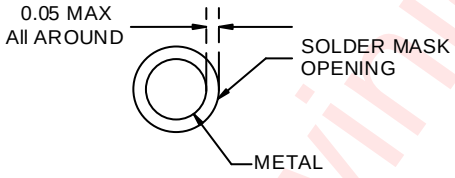


Bottom View

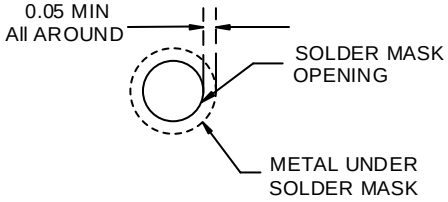
Unit: mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Dec. 2020	Datasheet V1.0 Released
V1.1	Oct.2021	1. Modified the definition of Production Tracing Code (Page 2) 2. Changed the upper limit ranges of I_{Q_INX} , I_{QB_INX} and I_{SD_VSYS} in Electrical Characteristics table (Page 6) 3. Added the test condition of I_{SD_INX} in Electrical Characteristics table (Page 6) 4. Added the upper limit ranges of V_{T_RCB} and V_{R_RCB} in Electrical Characteristics table (Page 7) 5. Changed the lower limit of V_{IH_IIC} in Electrical Characteristics table (Page 7) 6. Modified the description of Device Address (Page 17) 7. Modified the description of CHIPID (Page 21) 8. Modified the description of LDSW_SEQ (Page 23 and Page 24) 9. Changed Side view (Page 27)
V1.2	Nov.2021	1. Modified the Figure 5(Page 8) 2. Added the SWITCHING CHARACTERISTICS in Electrical Characteristics table (Page 7 and Page 8)
V1.3	Jul.2022	1. Changed the upper limit range of V_{OL_SDA} from 0.2V to 0.3V (Page 7) 2. Added I2C INTERFACE TIMING in Electrical Characteristics table (Page 9) 3. Updated figure index number from Figure 6 to Figure 48 (Page 9 to Page 20) 4. Added Ron vs. Temperature curves in Figure 20 with VIN=1.7V and 1.8V (Page 12) 5. Added package thickness in ORDERING INFORMATION (Page 4) 6. Added description table of reset register (Page 27)

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