USB Type-C Low Speed and High Speed Ports Protection IC

FEATURES

- IEC61000-4-5 surge protection
  - ±80V surge protection on CON_LSP1/2
  - ±30V surge protection on CON_HSP1/2
- USB Type-C LSP1/2 and HSP1/2 DC protection
  - CON_LSP1/CON_LSP2: 24V DC
  - CON_HSP1/CON_HSP2: 28V DC
- Dead battery circuits in CON_LSP1/CON_LSP2
- Integrated low R_{dson} switch
  - LSP switch: 340mΩ typical
  - HSP switch: 4.4 Ω typical
- IEC61000-4-2 ESD protection for CON_LSP1/2
  - Contact discharge: ±8kV
  - Air discharge: ±12kV
- Default Over-Voltage Protection (OVP) threshold
  - CON_LSP1/CON_LSP2: 5.8V typical
  - CON_HSP1/CON_HSP2: 4.8V typical
- Low supply current: 26μA typical
- LSP1/2 leakage current: 0.5μA typical
- Fast OVP turn off time: 70ns typical
- Over-temperature protection (OTP)
- Under-voltage lockout (UVLO)
- WLCSP 1.82mm×1.27mm-12B package

APPLICATIONS

- Smartphones
- Tablets
- Laptop

GENERAL DESCRIPTION

AW35602 is a single chip USB Type-C port protection solution, it integrates four channels of switches with OVP protection. CON_LSP1/2 pins can tolerate up to 24V DC, and CON_HSP1/2 pins can tolerate up to 28V DC. LSP switch can be used to protect CC of Type-C, and HSP switch can be used to protect D+/D- or SBU of Type-C.

AW35602 will disconnect all four channels of switches when any pin of CON_LSP1/2 or CON_HSP1/2 is above the OVP threshold, LSP1, LSP2, HSP1 and HSP2 in system side are protected from the high voltage. When OVP is detected, FLAGB pin is pulled down.

AW35602 integrates dead battery circuits in CON_LSP1 and CON_LSP2.

AW35602 integrates ±80V IEC61000-4-5 surge protection on CON_LSP1 and CON_LSP2, and also provides ±8kV contact discharge and ±12kV air discharge IEC61000-4-2 ESD protection on CON_LSP1 and CON_LSP2.

TYPICAL APPLICATION CIRCUIT

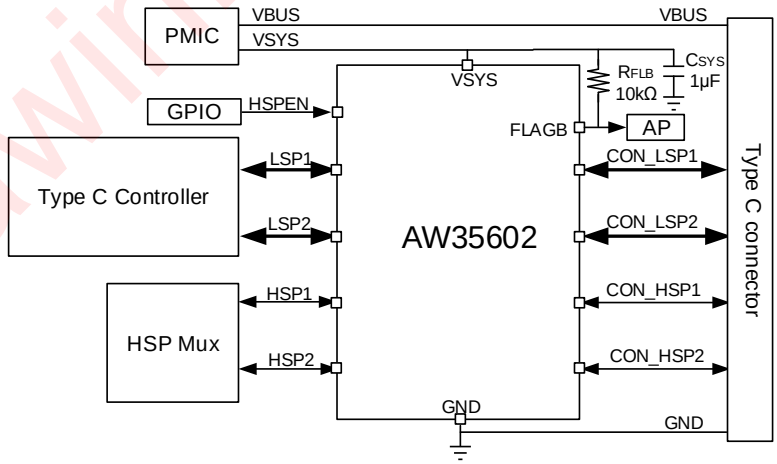

Figure 1 AW35602 typical application circuit

NOTE: Type-C CC channels can only use LSP switches.

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PIN CONFIGURATION

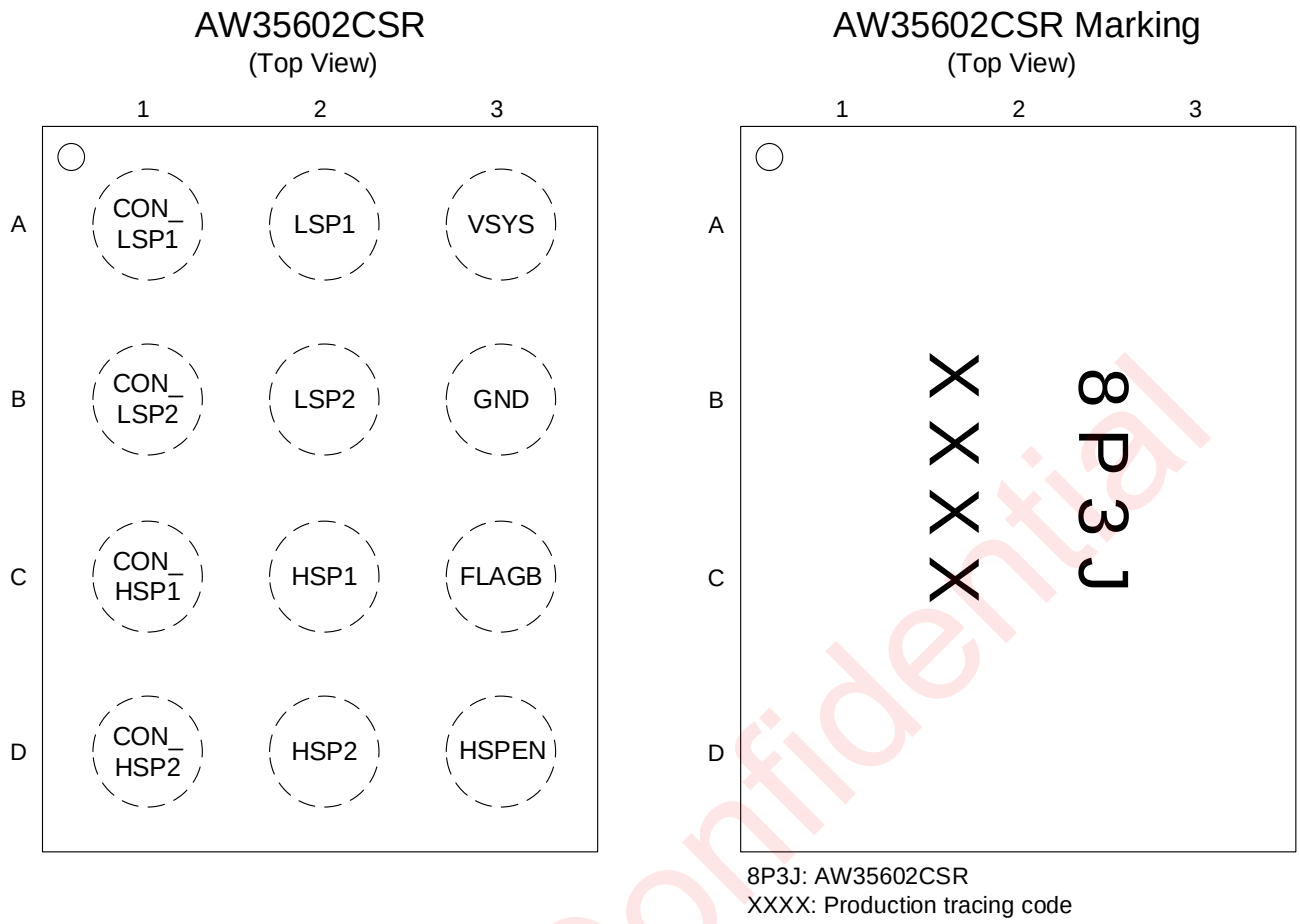

Figure 2 Pin Configuration

PIN DEFINITION

Pin	Name	Description
A1	CON_LSP1	Connector side of the LSP1 OVP FET.
A2	LSP1	System side of the LSP1 OVP FET.
A3	VSYS	2.7V to 5.5V power supply.
B1	CON_LSP2	Connector side of the LSP2 OVP FET.
B2	LSP2	System side of the LSP2 OVP FET.
B3	GND	Ground.
C1	CON_HSP1	Connector side of the HSP1 OVP FET.
C2	HSP1	System side of the HSP1 OVP FET.
C3	FLAGB	OVP flag, active-low, open-drain. FLAGB is logic low when OVP occurs, otherwise it is logic high.
D1	CON_HSP2	Connector side of the HSP2 OVP FET.
D2	HSP2	System side of the HSP2 OVP FET.
D3	HSPEN	HSP switch enable.

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FUNCTIONAL BLOCK DIAGRAM

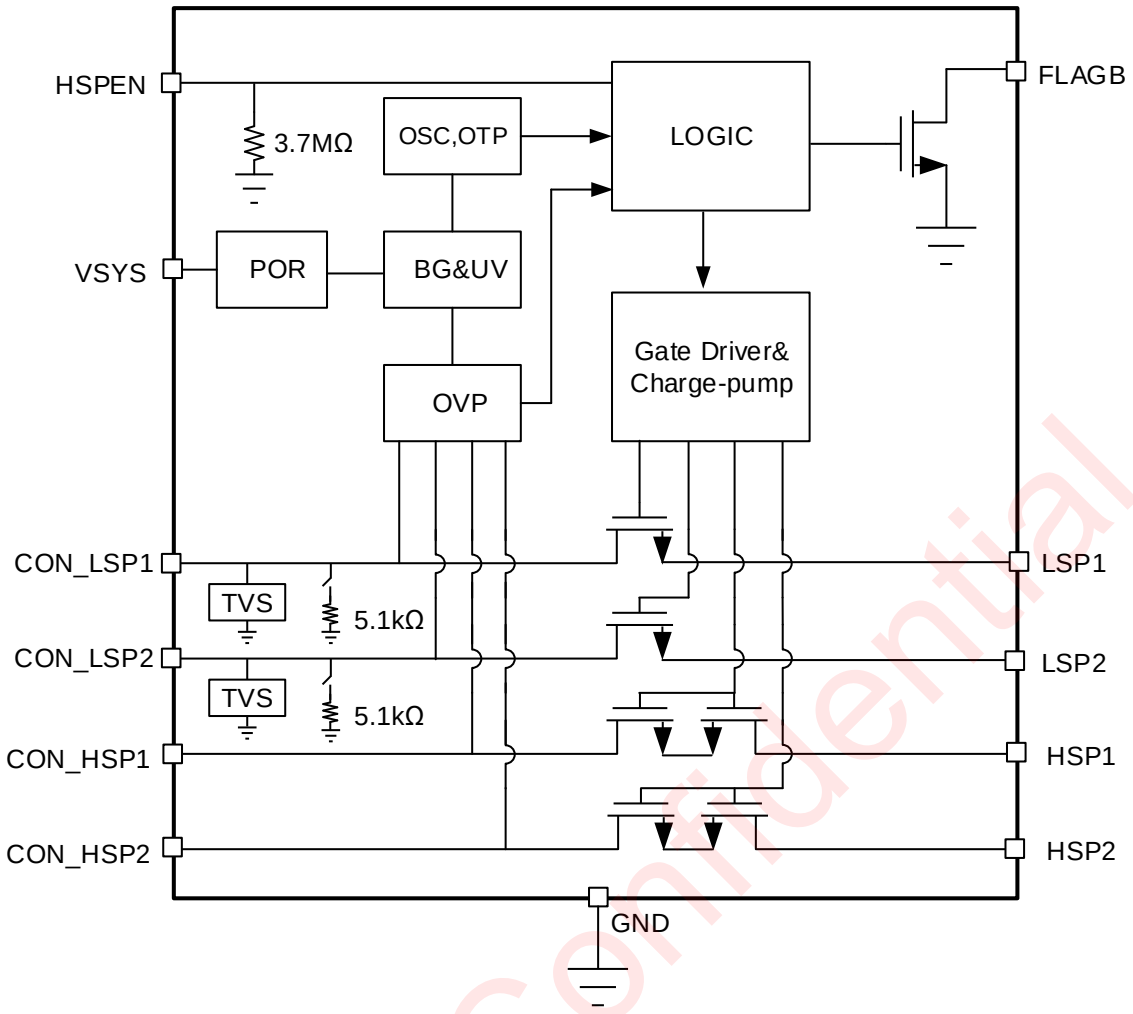

Figure 3 Functional Block Diagram

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TYPICAL APPLICATION CIRCUITS

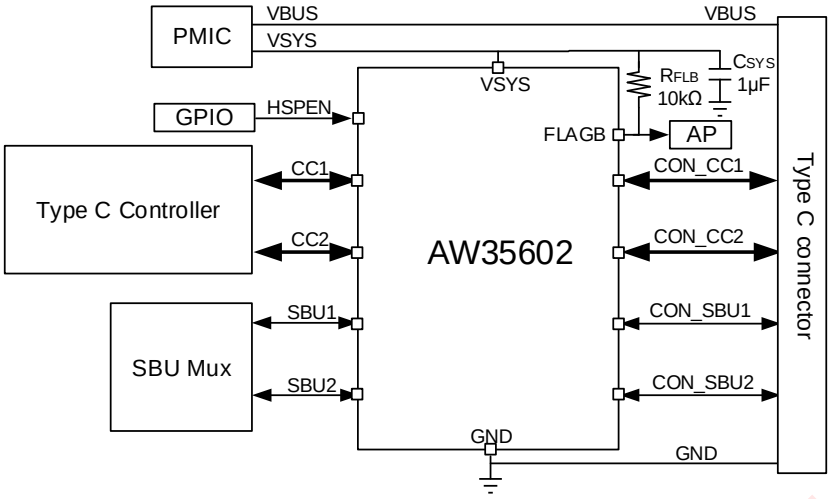

Figure 4 AW35602 application circuit (HSP switch used for SBU switch)

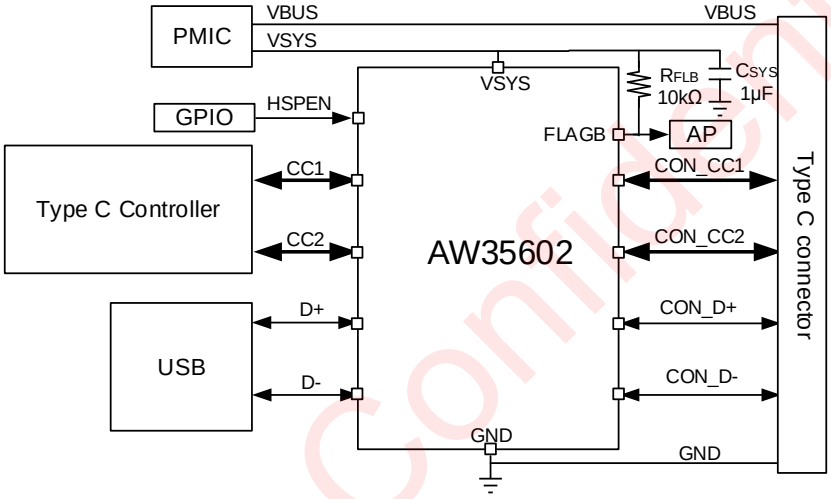

Figure 5 AW35602 application circuit (HSP switch used for D+/D- switch)

Notice for Typical Application Circuits:

1. Place C_{SYS} as close as possible to the chip.
2. Internal pull-down resistor on HSPEN pin ensures the D+/SBU1 and D-/SBU2 channels are disabled by default. When HSPEN is logic high, D+/SBU1 and D-/SBU2 channels are active.
3. If FLAGB is not used, it can be left floating.
4. CC1, CC2 channels support ±1A current, the connection lines should be as wide as possible.
5. Type-C CC channels can only use LSP switches.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35602CSR	-40℃ ~ 85℃	WLCSP 1.82mm×1.27mm-12B	8P3J	MSL1	ROHS+HF	3000 units/ Tape and Reel

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ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{VSYS}	Power voltage		-0.3	6	V
V_{CON_LSPX}	CON_LSP1, CON_LSP2 input voltage		-0.3	24	V
V_{CON_HSPX}	CON_HSP1, CON_HSP2 input voltage		-0.3	28	V
V_{LSPX}	LSP1, LSP2 output voltage		-0.3	6	V
V_{HSPX}	HSP1, HSP2 output voltage		-0.3	6	V
V_{FLAGB}	FLAGB voltage		-0.3	6	V
V_{HSPEN}	HSPEN voltage		-0.3	6	V
I_{CON_LSPX}	CON_LSP1,CON_LSP2 DC current		-1	1	A
I_{CON_HSPX}	CON_HSP1,CON_HSP2 DC current		-100	100	mA
T_{JMAX}	Maximum operating junction temperature			150	°C
T_{STG}	Storage temperature		-65	150	°C
T_{LEAD}	Soldering temperature	At leads, 10 seconds		260	°C
CON_LSPX Surge	CON_LSP1,CON_LSP2 surge immunity	IEC61000-4-5 test with 2Ω equivalent series resistance	-80	80	V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Thermal resistance from junction to ambient (NOTE 1)	In free air	90	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

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ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{ESD}	IEC61000-4-2 system ESD on CON_LSP1,CON_LSP2	Contact discharge	±8	kV
		Air gap discharge	±12	kV
	Human body model	ESDA/JEDEC JS-001-2017	±2	kV
	Charged device model	ESDA/JEDEC JS-002-2018	±1.5	kV
$I_{Latch-up}$	Latch up	JESD78E	±200	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SYS}	Input DC voltage	2.7		5.5	V
V_{HSPEN}	HSPEN input voltage	0		5.5	V
V_{FLAGB}	FLAGB output voltage	0		5.5	V
V_{CON_LSPX}, V_{LSPX}	CON_LSP1,CON_LSP2,LSP1,LSP2 voltage	0		5.5	V
V_{CON_HSPX},V_{HSPX}	CON_HSP1,CON_HSP2,HSP1,HSP2 voltage	0		5.5	V
T_A	Ambient temperature	-40		85	°C

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ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{VSYS} = 3.3V, C_{SYS} = 1μF, T_A = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Power supply and leakage current						
V_{UVLO}	Power under voltage lockout	VSYS rising	1.60	2.50	2.70	V
V_{UVLO_HYS}	Power under voltage lockout hysteresis			100		mV
I_{VSYS}	VSYS supply current	V_{VSYS}=3.3V, V_{HSPEN}=3.3V		26	60	μA
I_{LSP_Leak}	Leakage current for LSP pins	V_{VSYS}=3.3V, V_{LSPX}=3.3V, CON_LSPX floating.		0.5	3	μA
I_{HSP_Leak}	Leakage current for HSP pins	V_{VSYS}=3.3V, V_{HSPEN}=3.3V, V_{HSPX}=3.3V, CON_HSPX floating.		0.4	3	μA
LSP switches						
R_{ON}	Switch on resistance	V_{VSYS}=3.3V, V_{LSPX}=3.3V, I_{OUT}= 100mA, T_A = 25°C		340	600	mΩ
R_{ON_Flat}	On resistance flatness	CON_LSPX input 100mA, sweep LSPX voltage between 0V and 3.3V, T_A = 25°C			20	mΩ
R_D	Dead battery pull-down resistance	V_{CON_LSPX}=3.3V	4.1	5.1	6.1	kΩ
V_{CLAMPH}	CON_LSPX clamp voltage	External current 330μA in CON_LSPX	1.35	1.75	2.00	V
V_{CLAMPM}	CON_LSPX clamp voltage	External current 180μA in CON_LSPX	0.75	1.00	1.20	V
V_{CLAMPL}	CON_LSPX clamp voltage	External current 80μA in CON_LSPX	0.55	0.87	1.10	V
V_{OVPLSP}	OVP threshold on CON_LSPX	CON_LSPX rising	5.5	5.8	6.0	V
V_{OVPLSP_HYS}	OVP threshold hysteresis			100		mV
CON_LSP	Equivalent on capacitance	Capacitance from CON_LSPX or LSPX to GND when device is powered. VCON_LSPX= 0V to 1.2V, f = 240kHz		200		pF
$V_{CLAMPLSP}$	Maximum clamp voltage on system side.	8/20μs surge, Vsurge=+80V		7		V
HSP switches						
R_{ON}	Switch on resistance	V_{SYS}=3.3V,V_{HSPEN}=3.3V, V_{HSPX}=3.3V, I_{OUT}=10mA, T_A=25°C		4.4	8	Ω
R_{ON_Flat}	On resistance flatness	Sweep HSPX voltage between 0V and 3.3V			100	mΩ
V_{OVPHSP}	OVP threshold on CON_HSPX	CON_HSPX rising	4.5	4.8	5.0	V
V_{OVPHSP_HYS}	OVP threshold hysteresis			100		mV

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ELECTRICAL CHARACTERISTICS（CONTINUED）

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{VSYS} = 3.3V, C_{SYS} = 1μF, T_A = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{ON_HSP}	Equivalent on capacitance	Capacitance from CON_HSPX or HSPX to GND when device is powered. V_{CON_HSPX} =0V to 1.2V, f=240MHz		6		pF
BW_{HSP}	Single ended on bandwidth (-3dB)	R_L=50Ω		800		MHz
$V_{CLAMPHSP}$	Maximum clamp voltage on system side.	8/20μs surge, Vsurge=+30V		7		V
FLAGB						
V_{OL}	Output low voltage	I_{OL}=5mA		0.08	0.3	V
I_{OH}	High level leakage current	V_{FLAGB}=5.5V			1	μA
HSPEN						
V_{IH}	Valid input high		1.2			V
V_{IL}	Valid input low				0.4	V
R_{PD}	Pull down resistance			3.7		MΩ
Thermal shutdown						
T_{SDN}	Shutdown temperature	Temperature rising		135		°C
T_{SDN_HYS}	Shutdown temperature hysteresis			10		°C
Timings requirements						
t_{ON_FET}	Power on delay time	Time from VSYS valid to LSP and HSP OVP FETs are on, V_{HSPEN}=3.3V		2.4		ms
$t_{ON\_FET\_DB}$	Dead battery resistors valid time	Time from VSYS valid to the internal dead battery resistors are turned off		4.5		ms
t_{ovp_res}	OVP response time	Time from crossing rising CON_LSPX/CON_HSPX at OVP voltage until LSPX/HSPX stop rising. Rising rate is70V/μs		70		ns
$t_{ovp\_deb\_LSP}$	LSP switch recovery time after OVP removed			50		μs
$t_{ovp\_deb\_HSP}$	HSP switch recovery time after OVP removed			25		μs

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T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{SYS} = 3.3V, C_{SYS} = 1μF, T_A = 25°C.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{HSP_ON}	HSP switch enable time from HSPEN to high			40		μs
$t_{off\_thermal}$	Time to shut down from over-temperature			20		μs
t_{OTP_deb}	OTP recovery time			20		ms
t_{FLAGB_ass}	Time to FLAGB assertion from OVP detected			5		μs
t_{FLAGB_deass}	Time from switches turn on after OVP to FLAGB de-assertion			4.5		ms

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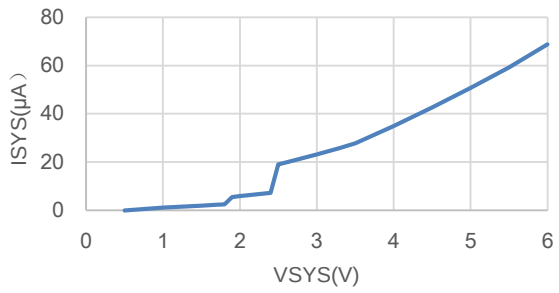
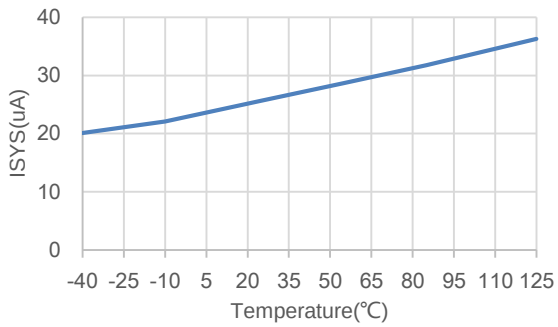
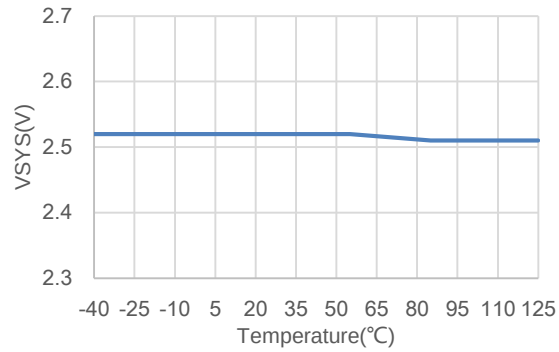
TYPICAL CHARACTERISTICS



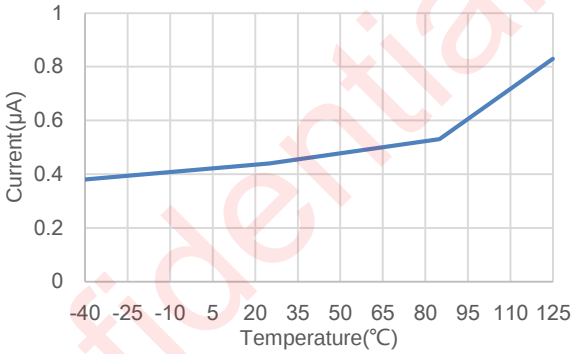
Supply Current vs Supply Voltage
Temperature=25℃,HSPEN=VSYS



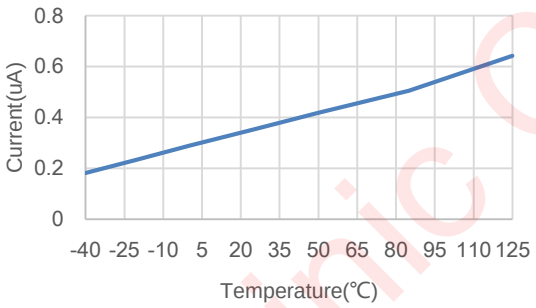
Supply Current vs Temperature
VSYS=3.3V,HSPEN=VSYS



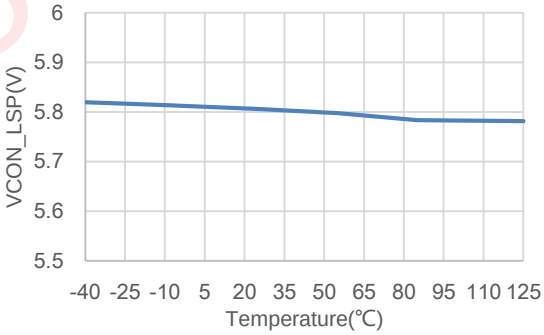
UVLO Voltage vs Temperature



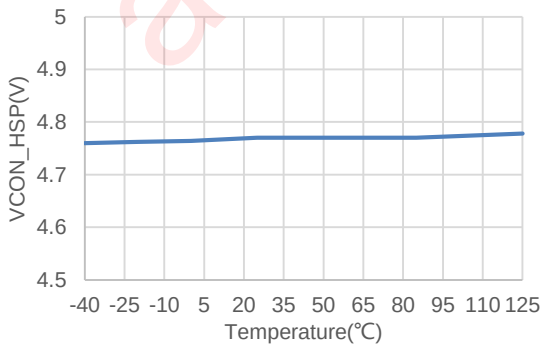
LSP Path Leakage Current vs Temperature
VSYS=3.3V



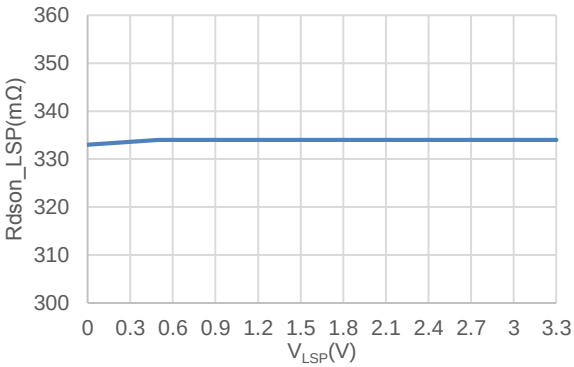
HSP Path Leakage Current vs Temperature
VSYS=3.3V



CON_LSP OVP Threshold Voltage vs Temperature
VSYS=3.3V



CON_HSP OVP Threshold Voltage vs Temperature
VSYS=3.3V



LSP Path Rdson vs LSP Voltage

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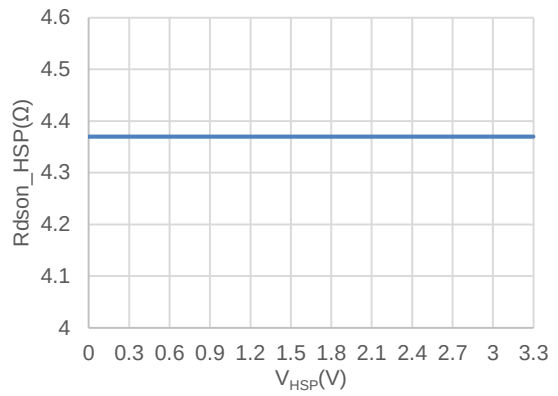
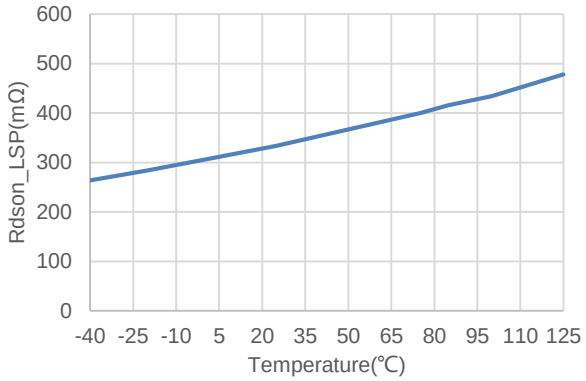
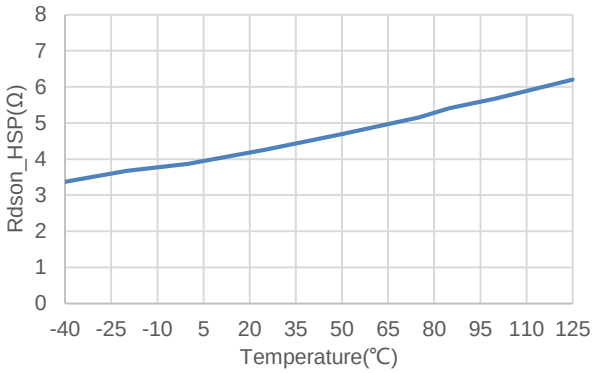


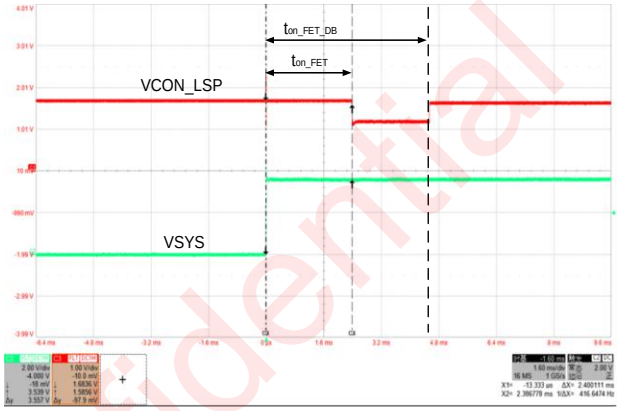
HSP Path Rdson vs HSP Voltage



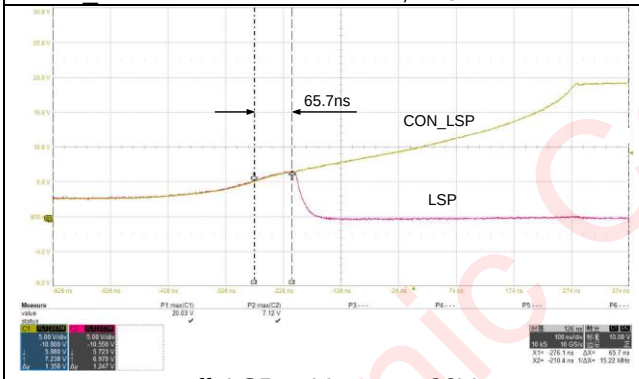
LSP Path Rdson vs Temperature
CON_LSP sink current is 100mA,V_{LSP}=VSYS=3.3V



HSP Path Rdson vs Temperature
CON_HSP sink current is 10mA, V_{HSP}=VSYS=3.3V

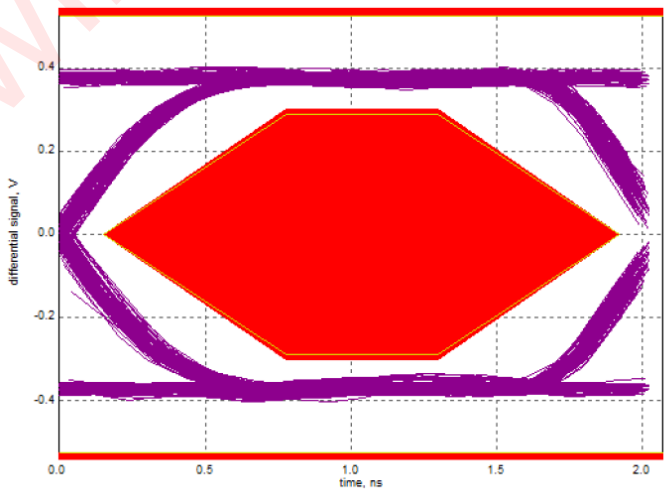


Power On Delay Time



toff_LSP at Vsurge=+80V

toff_HSP at Vsurge=+30V



USB 2.0 High Speed Eye Diagram

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TIMING DIAGRAM

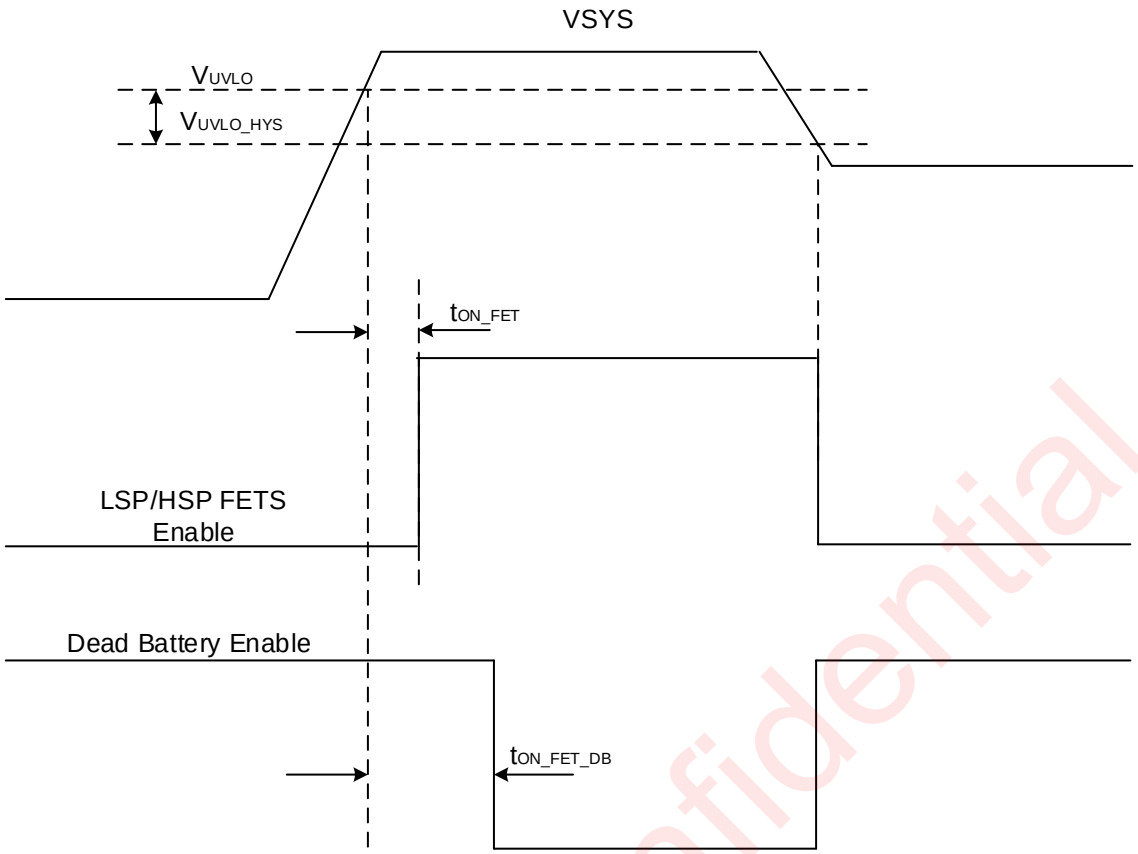

Figure 6 Power on and off Timing diagram

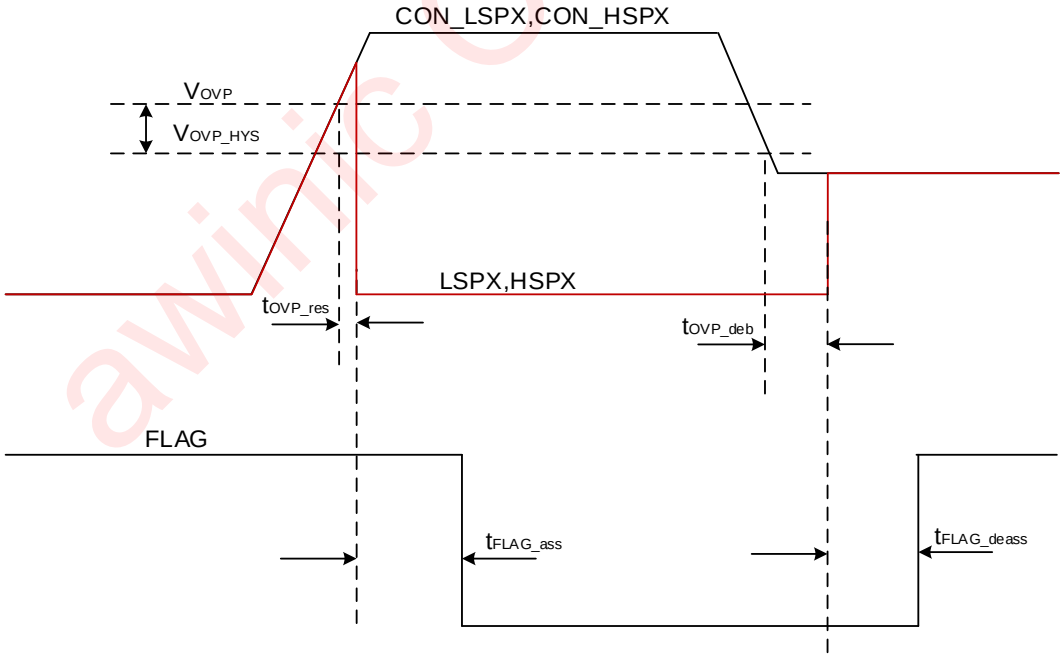

Figure 7 Over Voltage Protection Timing diagram

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DETAILED FUNCTIONAL DESCRIPTION

The AW35602 is a single chip USB Type-C port protection solution, it integrates four channels of switches with over-voltage protection function that protect LSP1, LSP2, HSP1 and HSP2. The CON_LSP1 and CON_LSP2 pins of AW35602 are 24V DC tolerant, CON_HSP1 and CON_HSP2 pins are 28V DC tolerant, so they can be well protected if they are shorted to USB VBUS by accident or moisture. The LSP switches are always on while the HSP switches are controlled by HSPEN pin. When HSPEN is logic high, HSP switches are turned on. When HSPEN is logic low, HSP switches are turned off.

Surge and ESD Protection

AW35602 integrates ±80V IEC61000-4-5 surge protection on CON_LSP1 and CON_LSP2, and also provides ±8kV contact discharge and ±12kV air discharge IEC61000-4-2 ESD protection on CON_LSP1 and CON_LSP2, so no external TVS are needed on these two pins, which helps to reduce external BOM cost. AW35602 also integrates ±30V IEC61000-4-5 surge protection on CON_HSP1 and CON_HSP2.

LSP Switch Power Delivery

The typical on-resistance of the integrated switches of LSP1 and LSP2 is 340mΩ, the two switches are both able to deliver 1A DC current, which is compliant with the USB Type-C specification.

LSP Dead Battery Resistors

AW35602 integrates dead battery pull-down resistors on CON_LSP1 and CON_LSP2 pins to allow dead battery charging. In dead battery condition, the AW35602 is unpowered, the pull-up resistor from a power adaptor will activate the pull-down resistor inside the AW35602. Once power delivery is established from power adaptor to the system and AW35602 has power supply on its VSYS pin, after about 2.4ms the AW35602 turns on its LSP switches and after about another 2.1ms it removes its RD pull-down resistors.

High Bandwidth HSP Switch

The HSP1 and HSP2 switches have typically 800MHz -3dB bandwidth, which can be used to transmit SBU signal or high speed signal, e.g. USB 2.0 data.

Over-Voltage Protection

The four channels of integrated switches of AW35602 all have over-voltage protection function, when over-voltage event is detected on any pin of CON_LSP1, CON_LSP2, CON_HSP1 or CON_HSP2，device will shut off all the switches within 70ns (typical)，as well as pull down the FLAGB to indicate there is over-voltage event to system. The typical OVP threshold voltage of CON_LSP1 and CON_LSP2 is 5.8V, typical OVP threshold voltage of CON_HSP1 and CON_HSP2 is 4.8V.

FLAGB Fault Report

FLAGB pin is the over-voltage fault report pin, it's recommended to be pulled up by 10kΩ pull-up resistor to I/O voltage. During normal operation, FLAGB is pulled up to logic high by pull-up resistor, when over-voltage event happens, FLAGB will output logic low.

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PCB LAYOUT CONSIDERATION

To obtain the optimal performance of AW35602, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to V_{SYS} pin as possible and avoid placing the bypass capacitors near the HSP1/HSP2 traces.
2. The differential characteristic impedance of HSP1 and HSP2 traces is suggested to be 90Ω, and it's better to shield HSP1 and HSP2 traces by ground planes.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. Place the high-speed lines as straight as possible, and avoid any sharp bends as possible to reduce EMI coupling.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals because they cause signal reflections.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Keep the high-speed lines trace in the same layer.
8. LSP1,LSP2 channels support ±1A current, the PCB routing lines should be as wide as possible.

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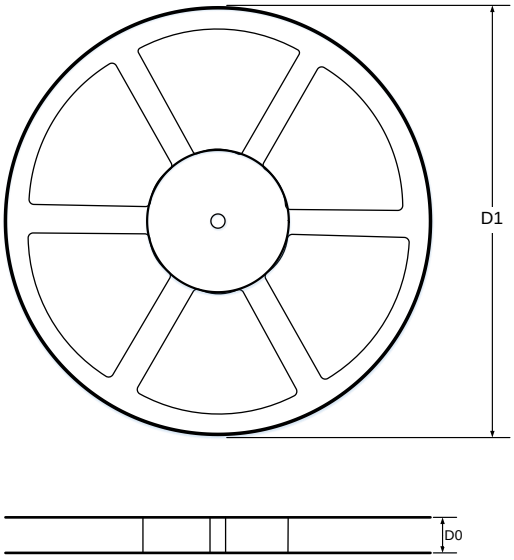
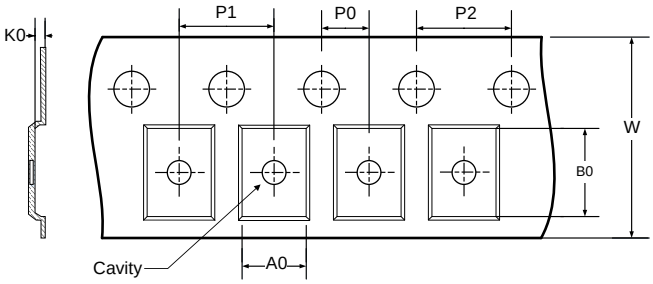
TAPE AND REEL INFORMATION

REEL DIMENSIONS

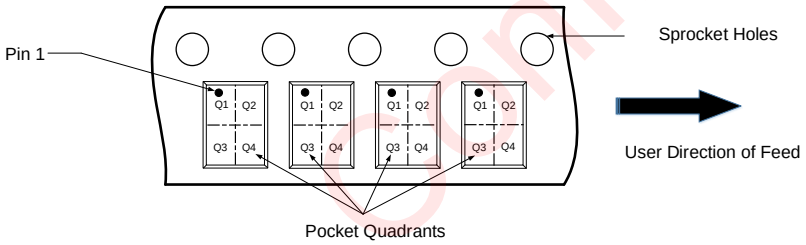


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.37	1.94	0.69	2.00	4.00	4.00	8.00	Q1

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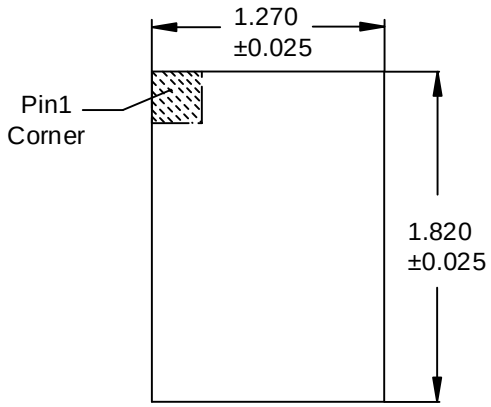
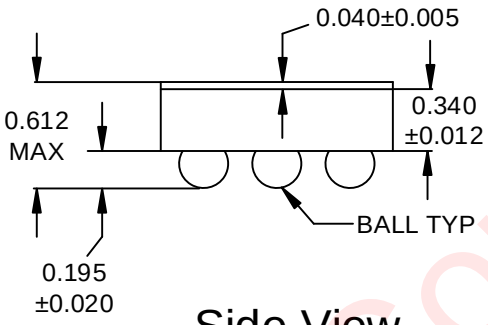
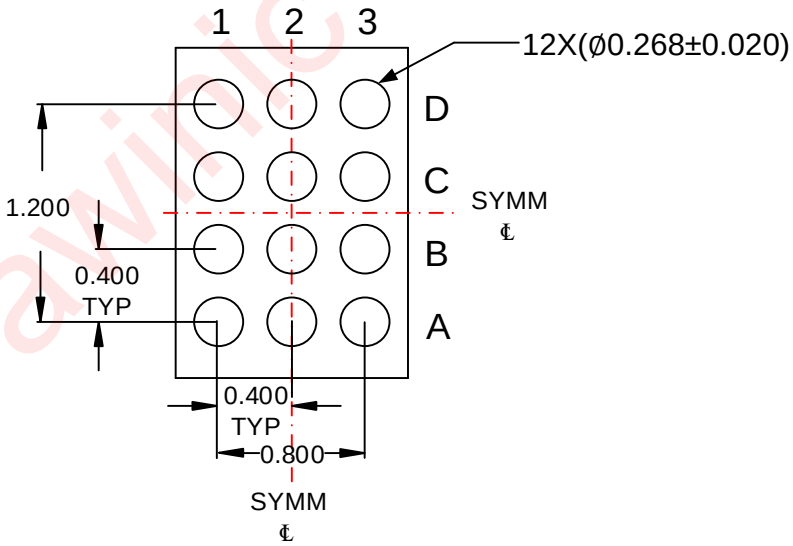
PACKAGE DESCRIPTION



Top View



Side View



Bottom View

Unit: mm

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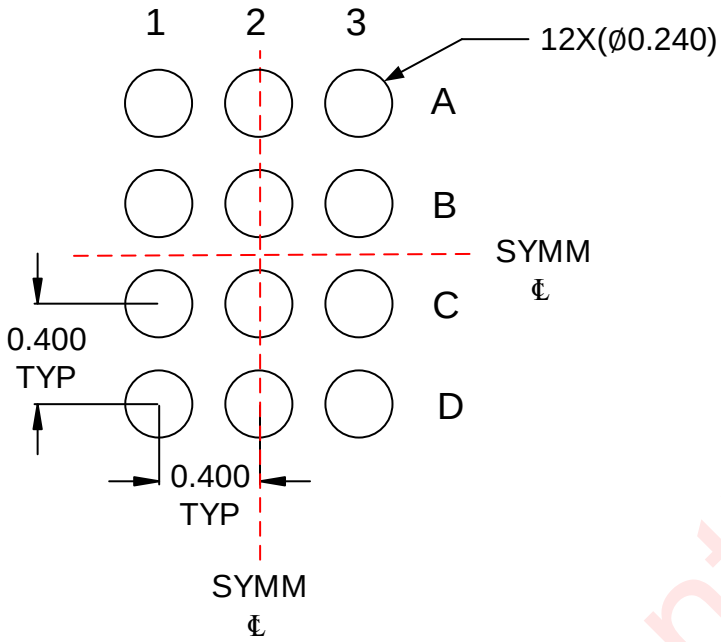
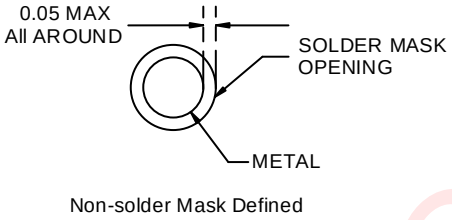
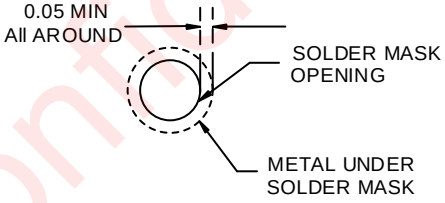
LAND PATTERN DATA





Non-solder Mask Defined



Solder Mask Defined

Unit: mm

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REVISION HISTORY

Version	Date	Change Record
V1.0	May.2019	First version
V1.1	Sep.2019	Update V_{CLAMPH}, V_{CLAMPM}, V_{CLAMPL},
V1.2	Sep.2020	Update UVLO_H low limit, R_{ON_FLAT}

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