

USB Type-C Low Speed Ports Protection IC

FEATURES

- IEC61000-4-5 surge protection
 - $\pm 80\text{V}$ surge protection on CON_LSP1/2
- USB Type-C LSP1/2 DC protection
 - CON_LSP1/CON_LSP2: 24V DC
- Dead battery circuits in CON_LSP1/CON_LSP2
- Integrated low R_{dson} switch
 - LSP switch: 340m Ω typical
- IEC61000-4-2 ESD protection for CON_LSP1/2
 - Contact discharge: $\pm 8\text{kV}$
 - Air discharge: $\pm 12\text{kV}$
- Default Over-Voltage Protection (OVP) threshold
 - CON_LSP1/CON_LSP2: 5.8V typical
- Low supply current: 20 μA typical
- LSP1/2 leakage current: 0.5 μA typical
- Fast OVP turn off time: 70ns typical
- Over-temperature protection (OTP)
- Under-voltage lockout (UVLO)
- WLCSP 1.82mm \times 1.27mm-12B package

APPLICATIONS

- Smartphones
- Tablets
- Laptop

GENERAL DESCRIPTION

AW35612 is a single chip USB Type-C port protection solution, it integrates two channels of switches with OVP protection. CON_LSP1/2 pins can tolerate up to 24V DC. LSP switch can be used to protect CC of Type-C.

AW35612 will disconnect both two channels of switches when any pin of CON_LSP1/2 is above the OVP threshold, LSP1, LSP2 in system side are protected from the high voltage.

AW35612 integrates dead battery circuits in CON_LSP1 and CON_LSP2.

AW35612 integrates $\pm 80\text{V}$ IEC61000-4-5 surge protection on CON_LSP1 and CON_LSP2, and also provides $\pm 8\text{kV}$ contact discharge and $\pm 12\text{kV}$ air discharge IEC61000-4-2 ESD protection on CON_LSP1 and CON_LSP2.

TYPICAL APPLICATION CIRCUIT

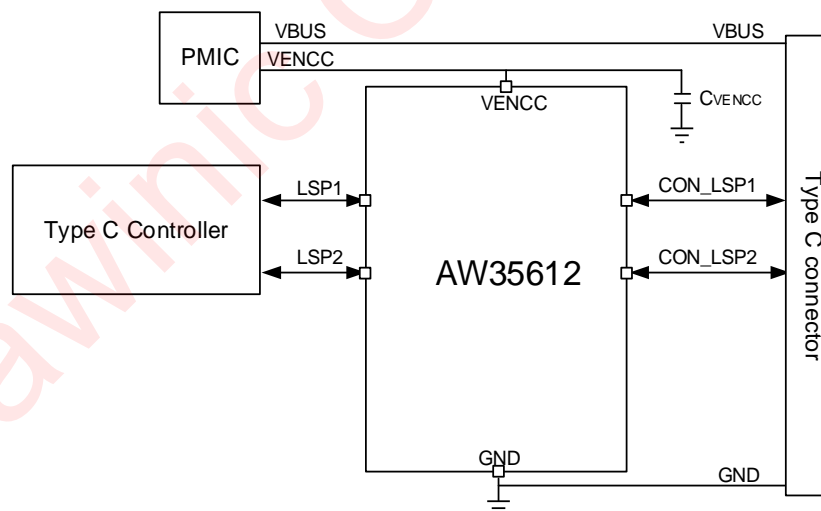


Figure 1 AW35612 typical application circuit

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PIN CONFIGURATION

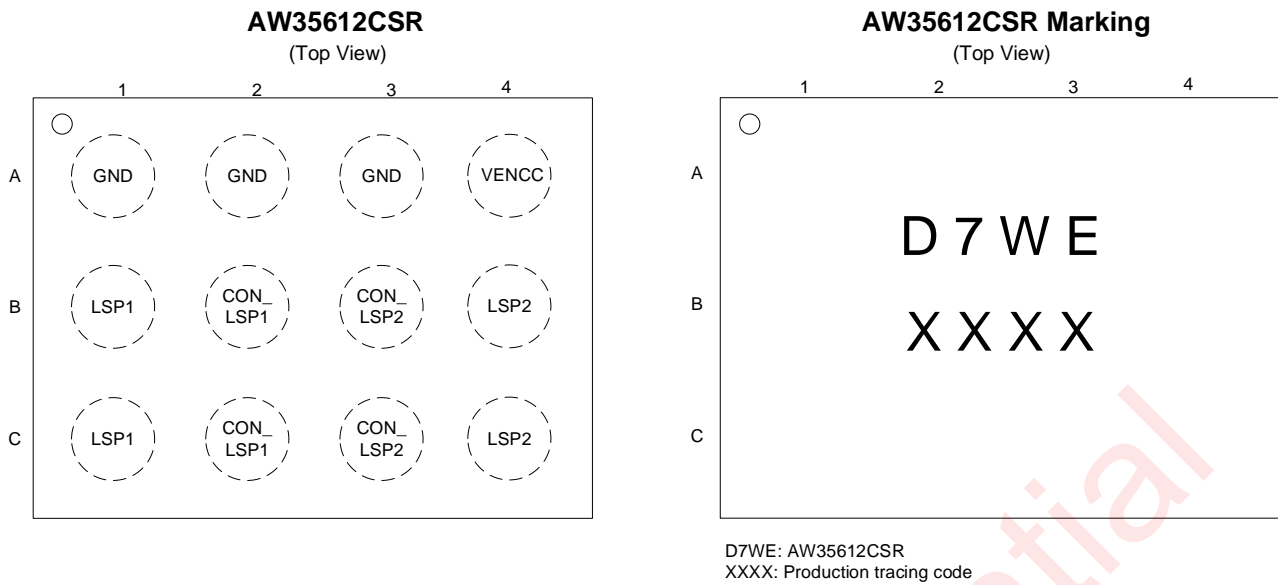


Figure 2 Pin Configuration

PIN DEFINITION

Pin	Name	Description
A1,A2,A3	GND	Ground.
A4	VENCC	2.7V to 5.5V power supply.
B1,C1	LSP1	System side of the LSP1 OVP FET.
B2,C2	CON_LSP1	Connector side of the LSP1 OVP FET.
B3,C3	CON_LSP2	Connector side of the LSP2 OVP FET.
B4,C4	LSP2	System side of the LSP2 OVP FET.

FUNCTIONAL BLOCK DIAGRAM

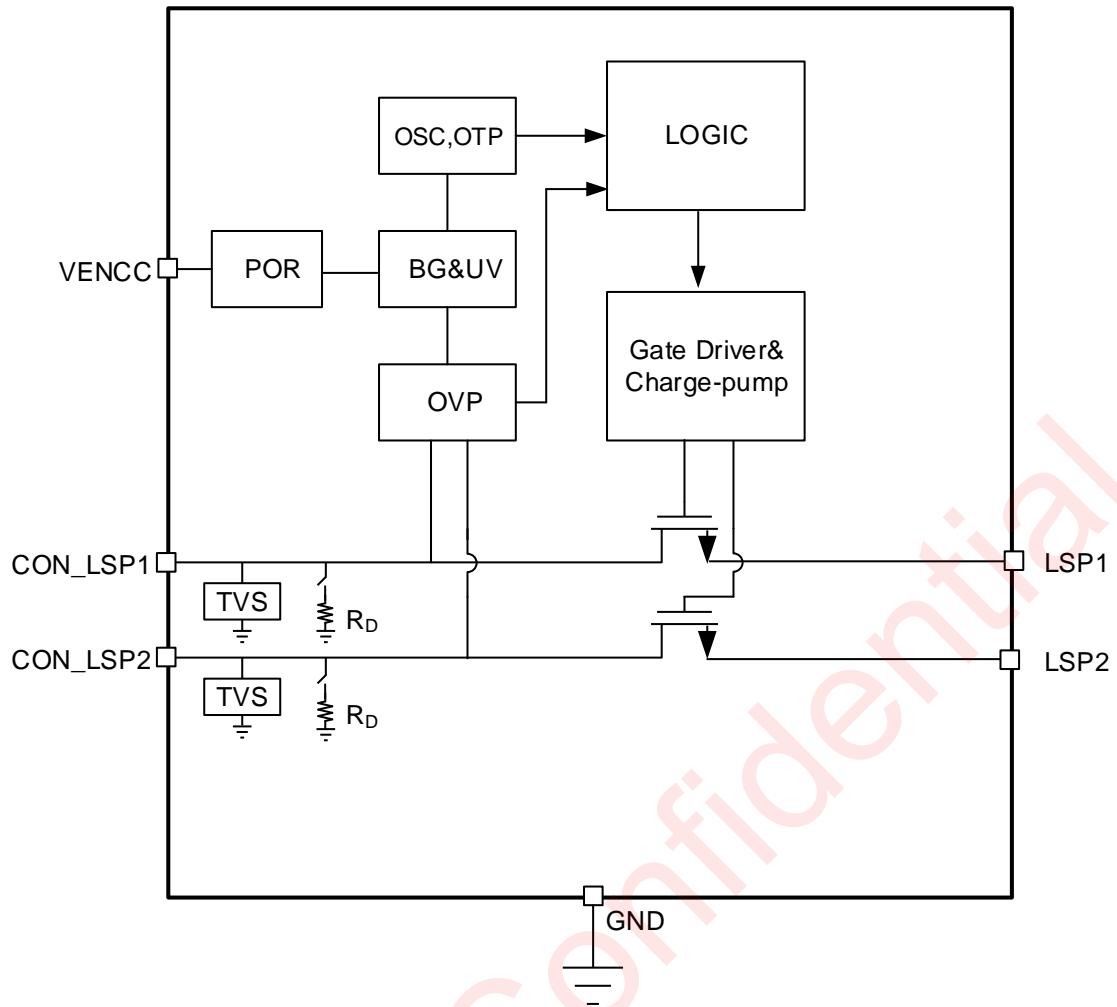


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

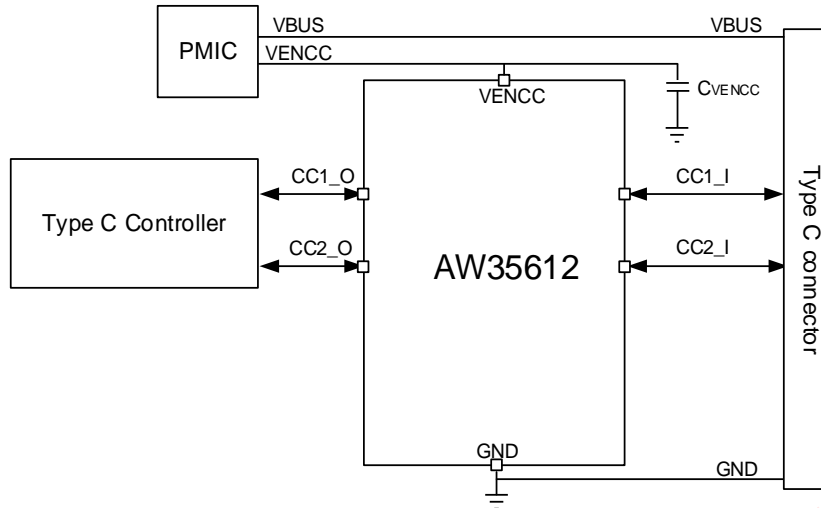


Figure 4 AW35612 application circuit (LSP switch used for CC switch)

Notice for Typical Application Circuits:

1. Place C_{VENCC} as close to the chip as possible.
2. CC1, CC2 channels support $\pm 1A$ current, route the lines according to application current value.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35612CSR	-40°C ~ 85°C	WLCSP 1.82mm×1.27mm-12B	D7WE	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Symbol	Parameter	Condition	Min.	Max.	Unit
V _{VENCC}	Power voltage		-0.3	6	V
V _{CON_LSPX}	CON_LSP1, CON_LSP2 input voltage		-0.3	24	V
V _{LSPX}	LSP1, LSP2 output voltage		-0.3	6	V
I _{CON_LSPX}	CON_LSP1, CON_LSP2 DC current		-1	1	A
T _{JMAX}	Maximum operating junction temperature			150	°C
T _{STG}	Storage temperature		-65	150	°C
T _{LEAD}	Soldering temperature	At leads, 10 seconds		260	°C
CON_LSPX Surge	CON_LSP1, CON_LSP2 surge immunity	IEC61000-4-5 test with 2Ω equivalent series resistance	-80	80	V

NOTE1: Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
R _{θJA}	Thermal resistance from junction to ambient (NOTE 1)	In free air	88.8	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
V _{ESD}	IEC61000-4-2 system ESD on CON_LSP1,CON_LSP2	Contact discharge	±8	kV
		Air gap discharge	±12	kV
	Human body model	ESDA/JEDEC JS-001-2017	±2	kV
	Charged device model	ESDA/JEDEC JS-002-2018	±1.5	kV
I _{Latch-up}	Latch up	JESD78E	±200	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{VENCC}	Input DC voltage	2.7		5.5	V
V _{CON_LSPX} , V _{LSPX}	CON_LSP1,CON_LSP2,LSP1,LSP2 voltage	0		5.5	V
T _A	Ambient temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{VENCC} = 3.3\text{V}$, $C_{VENCC} = 1\mu\text{F}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Power supply and leakage current						
V_{UVLO}	Power under voltage lockout	V_{ENCC} rising	1.60	2.50	2.70	V
V_{UVLO_HYS}	Power under voltage lockout hysteresis			100		mV
I_{VENCC}	V_{ENCC} supply current	$V_{VENCC}=3.3\text{V}$		20	60	μA
I_{LSP_Leak}	Leakage current for LSP pins	$V_{VENCC}=3.3\text{V}$, $V_{LSPX}=3.3\text{V}$, CON_LSPX floating		0.5	3	μA
LSP switches						
R_{ON}	Switch on resistance	$V_{VENCC}=3.3\text{V}$, $V_{LSPX}=3.3\text{V}$, $I_{OUT}=100\text{mA}$, $T_A = 25^{\circ}\text{C}$		340	600	m Ω
R_{ON_Flat}	On resistance flatness	CON_LSPX input 100mA, sweep LSPX voltage between 0V and 3.3V, $T_A = 25^{\circ}\text{C}$			20	m Ω
R_D	Dead battery pull-down resistance	$V_{CON_LSPX}=3.3\text{V}$	4.1	5.1	6.1	k Ω
V_{CLAMPH}	CON_LSPX clamp voltage	External current 330 μA in CON_LSPX	1.35	1.75	2.00	V
V_{CLAMPM}	CON_LSPX clamp voltage	External current 180 μA in CON_LSPX	0.75	1.00	1.20	V
V_{CLAMPL}	CON_LSPX clamp voltage	External current 80 μA in CON_LSPX	0.55	0.87	1.10	V
V_{OVPLSP}	OVP threshold on CON_LSPX	CON_LSPX rising	5.5	5.8	6.0	V
V_{OVPLSP_HYS}	OVP threshold hysteresis			100		mV
CON_LSP	Equivalent on capacitance	Capacitance from CON_LSPX or LSPX to GND when device is powered. V_C_LSPX/V_{LSPX} = 0V to 1.2V, $f = 240\text{kHz}$		200		pF
BW_{LSP}	Single ended on bandwidth (-3dB)	$R_L=50\Omega$		20		MHz
$V_{CLAMPLSP}$	Maximum clamp voltage on system side	8/20 μs surge, $V_{surge}=+80\text{V}$		7		V
Thermal shutdown						
T_{SDN}	Shutdown temperature	Temperature rising		135		$^{\circ}\text{C}$
T_{SDN_HYS}	Shutdown temperature hysteresis			10		$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (CONTINUED)

$T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise noted. Typical values are guaranteed for $V_{\text{VENCC}} = 3.3\text{V}$, $C_{\text{VENCC}} = 1\mu\text{F}$, $T_A = 25^{\circ}\text{C}$.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Timings requirements						
$t_{\text{ON_FET}}$	Power on delay time	Time from VENCC valid to LSP OVP FETs are on		2.4		ms
$t_{\text{ON_FET_DB}}$	Dead battery resistors valid time	Time from VENCC valid to the internal dead battery resistors are turned off		4.5		ms
$t_{\text{ovp_res}}$	OVP response time	Time from crossing rising CON_LSPX at OVP voltage until LSPX stop rising. Rising rate is $70\text{V}/\mu\text{s}$		70		ns
$t_{\text{ovp_deb_LSP}}$	LSP switch recovery time after OVP removed			50		μs
$t_{\text{off_thermal}}$	Time to shut down from over-temperature			20		μs
$t_{\text{OTP_deb}}$	OTP recovery time			20		ms

TIMING DIAGRAM

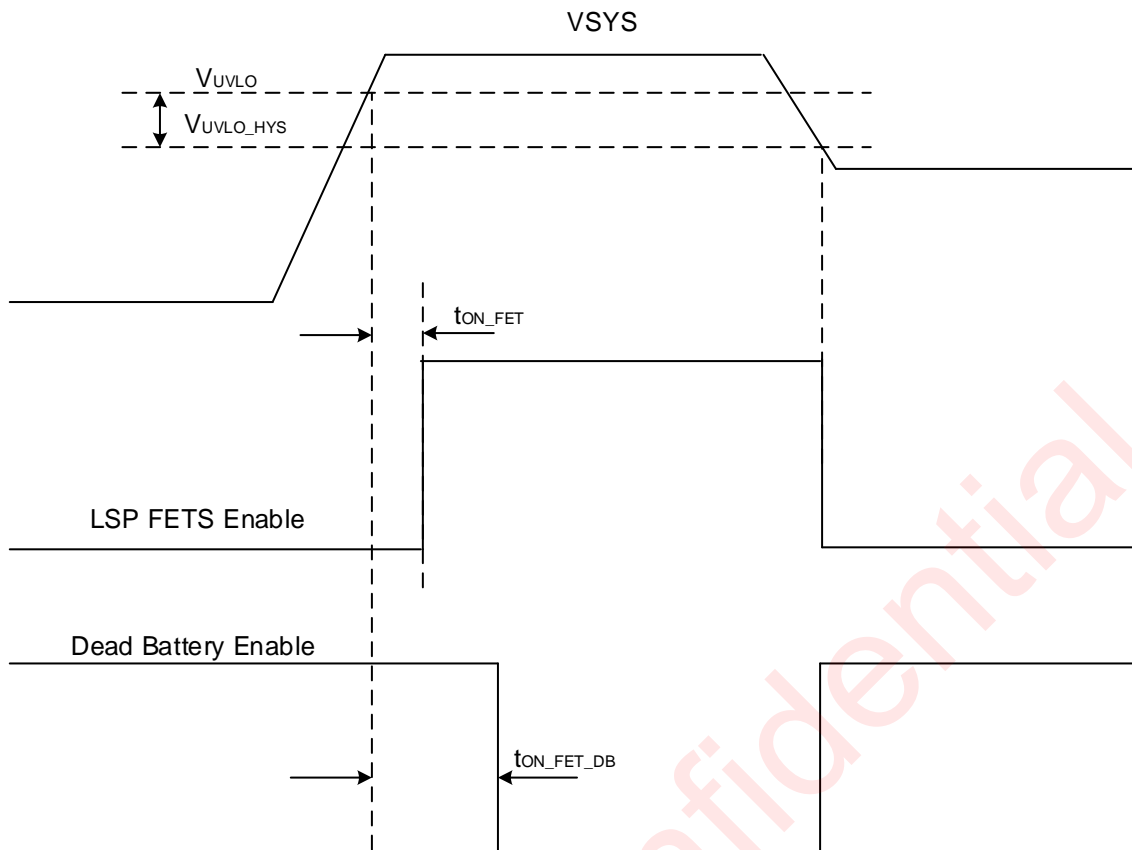


Figure 5 Power on and off Timing diagram

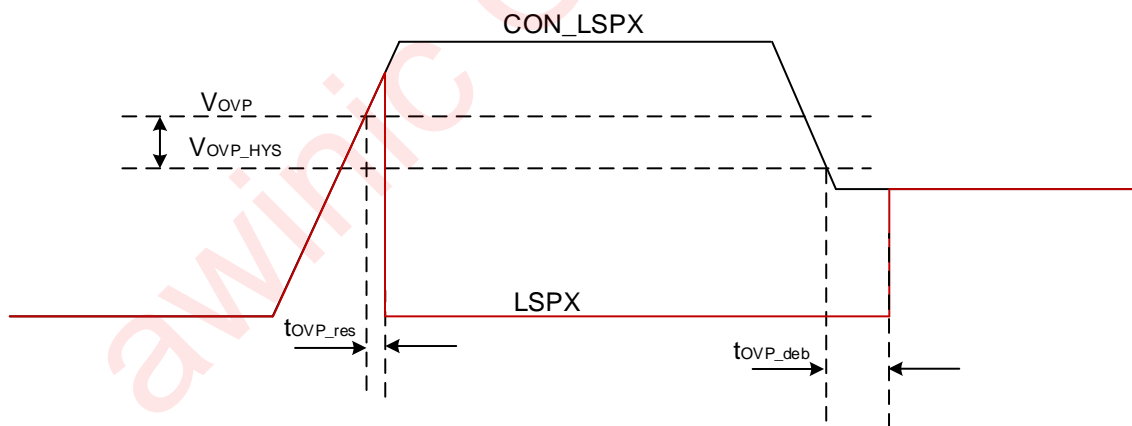
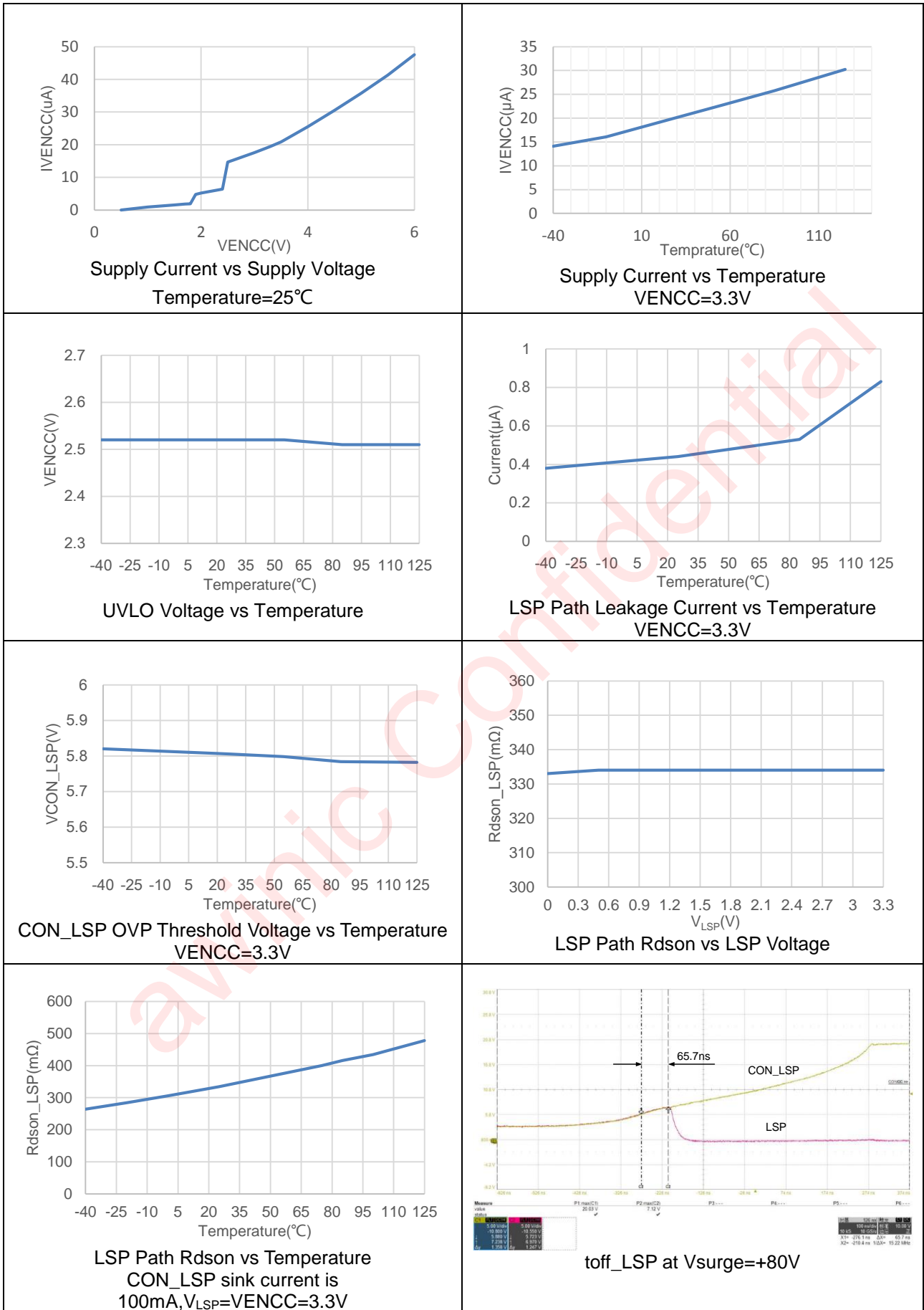


Figure 6 Over Voltage Protection Timing diagram

TYPICAL CHARACTERISTICS



DETAILED FUNCTIONAL DESCRIPTION

The AW35612 is a single chip USB Type-C port protection solution, it integrates two channels of switches with over-voltage protection function that protect LSP1 and LSP2. The CON_LSP1 and CON_LSP2 pins of AW35612 are 24V DC tolerant, so they can be well protected if they are shorted to USB VBUS by accident or moisture.

Surge and ESD Protection

AW35612 integrates $\pm 80\text{V}$ IEC61000-4-5 surge protection on CON_LSP1 and CON_LSP2, and also provides $\pm 8\text{kV}$ contact discharge and $\pm 12\text{kV}$ air discharge IEC61000-4-2 ESD protection on CON_LSP1 and CON_LSP2, so no external TVS are needed on these two pins, which helps to reduce external BOM cost.

LSP Switch Power Delivery

The typical on-resistance of the integrated switches of LSP1 and LSP2 is $340\text{m}\Omega$, the two switches are both able to deliver 1A DC current, which is compliant with the USB Type-C specification.

LSP Dead Battery Resistors

AW35612 integrates dead battery pull-down resistors on CON_LSP1 and CON_LSP2 pins to allow dead battery charging. In dead battery condition, the AW35612 is unpowered, the pull-up resistor from a power adaptor will activate the pull-down resistor inside the AW35612. Once power delivery is established from power adaptor to the system and AW35612 has power supply on its VENCC pin, after about 2.4ms the AW35612 turns on its LSP switches and after about another 2.1ms it removes its R_D pull-down resistors.

Over-Voltage Protection

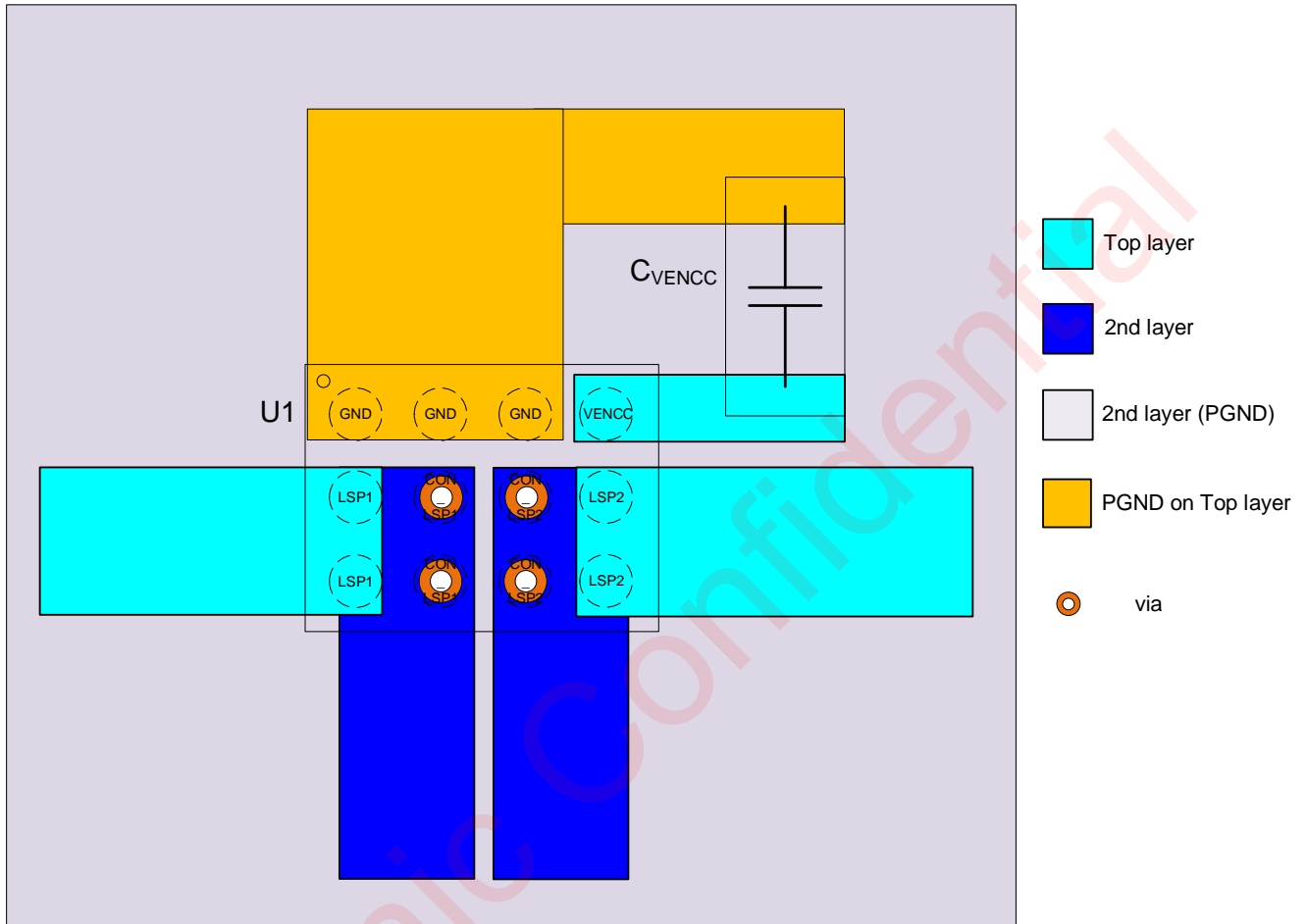
The two channels of integrated switches both have over-voltage protection function, when over-voltage event is detected on any pin of CON_LSP1, CON_LSP2, device will shut off both the switches within 70ns (typical). The typical OVP threshold voltage of CON_LSP1 and CON_LSP2 is 5.8V.

PCB LAYOUT CONSIDERATION

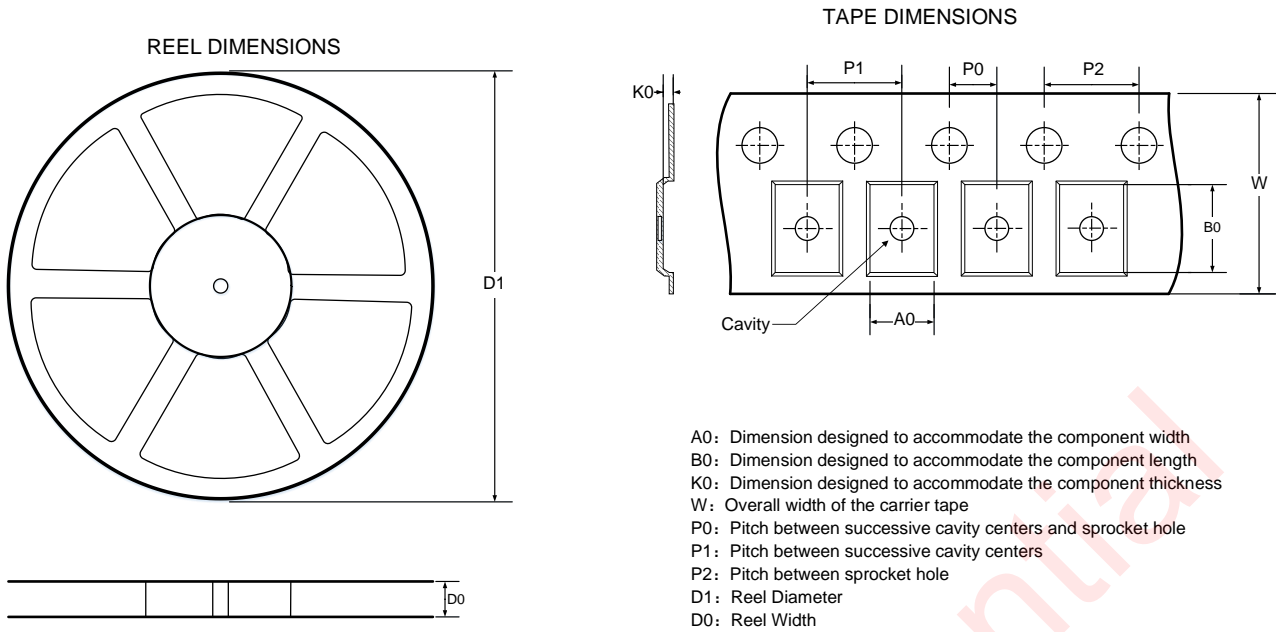
To obtain the optimal performance of AW35612, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to VENCC pin as possible.
2. LSP1, LSP2 channels support $\pm 1A$ current, route the lines according to application current value.

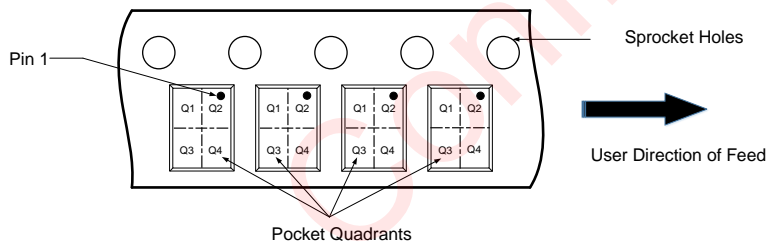
The following picture is an example of LAYOUT:



TAPE AND REEL INFORMATION



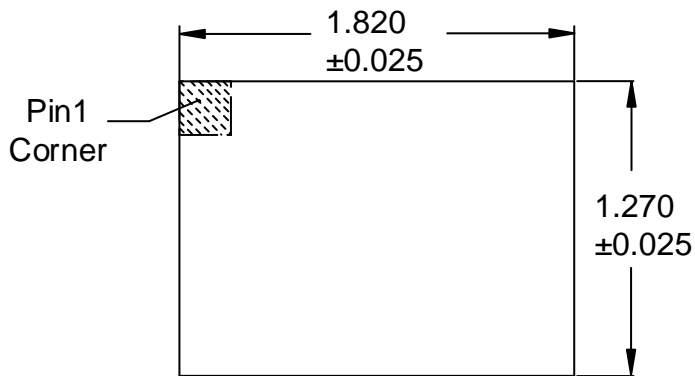
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



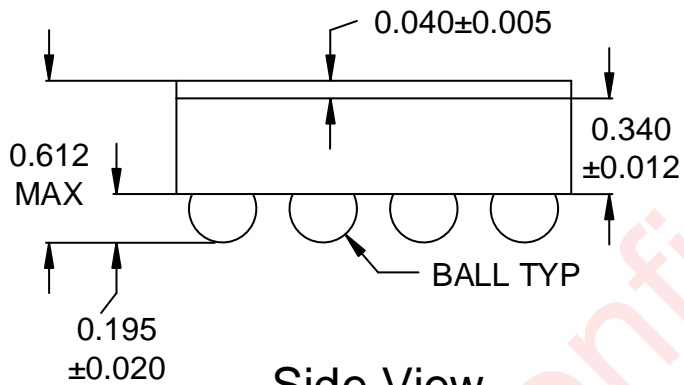
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.37	1.94	0.69	2.00	4.00	4.00	8.00	Q2

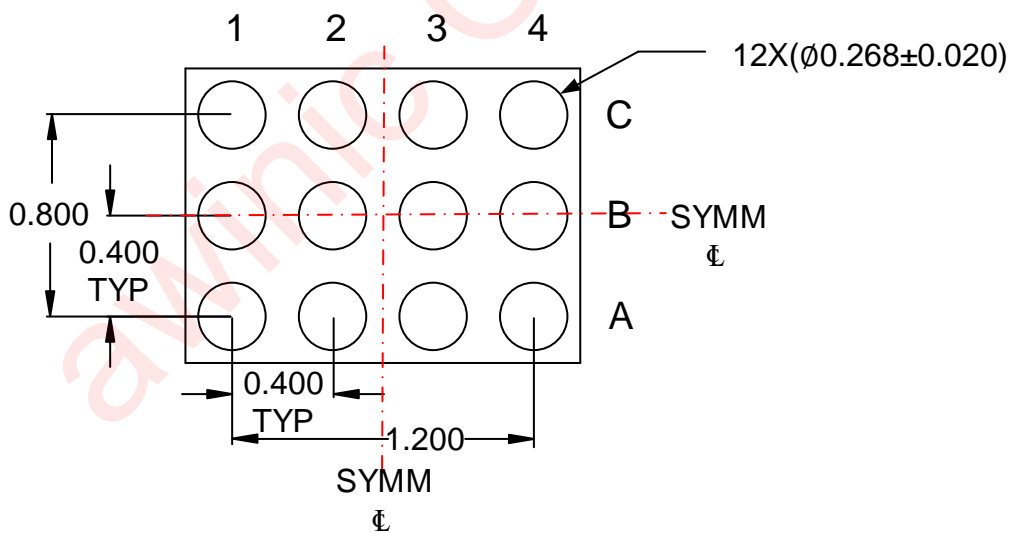
PACKAGE DESCRIPTION



Top View



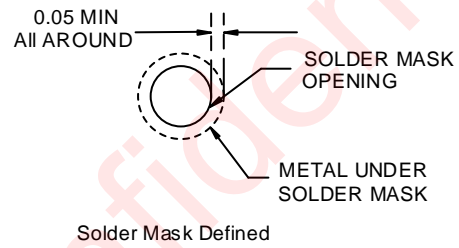
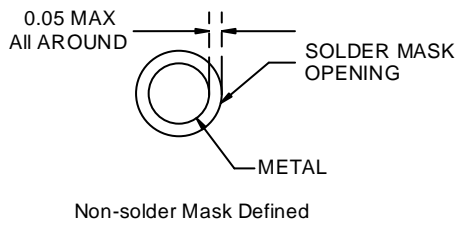
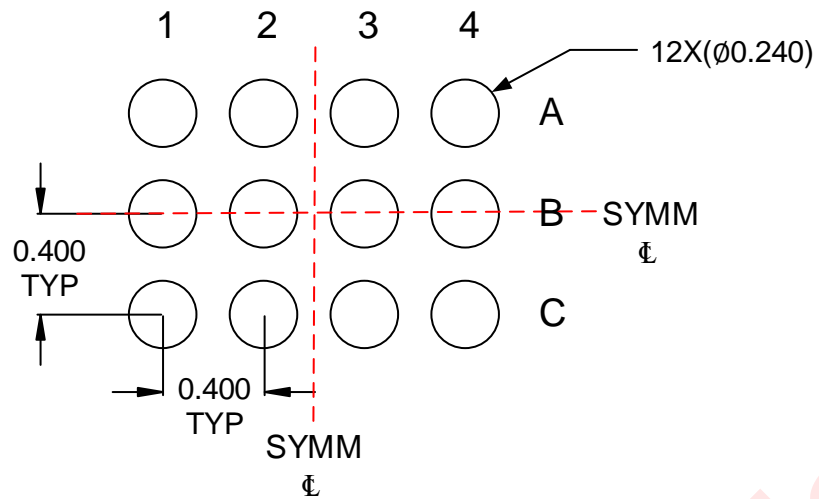
Side View



Bottom View

Unit: mm

LAND PATTERN DATA



Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	April.2019	First version
V1.1	Sep.2020	Update UVLO_H low limit

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