

High Efficiency Low Noise Large Volume Handsets Stereo TLTR-AGC 3rd Smart K Audio Amplifier

FEATURES

- ◆ Triple-Level Triple-Rate AGC algorithm:
 - Enhance bass, improve the dynamic range
 - Increase volume, eliminate noise, timely and effectively protect the speaker
- ◆ Output Power: 3.1W@8Ω, 3.5W@6Ω
- ◆ Low Noise: 11μV
- ◆ Low THD+N: 0.02%
- ◆ Overall efficiency up to 80%
- ◆ Support high power receiver stereo application
- ◆ Support AB/D speaker, AB/D receiver 2-in-1 application
 - AB receiver: 0dB, Vn=11μV, THD+N=0.2%
 - D receiver: 4.5dB, Vn=16μV, THD+N=0.02%
- ◆ Support 1.8V I2C Control
- ◆ Over current protection, over-temperature protection and short-circuit protection
- ◆ Super TDD-Noise suppression
- ◆ Excellent pop-click suppression
- ◆ High PSRR: 90dB (217Hz)
- ◆ FCQFN 2.5mmX2.0mmX0.55mm-16L package

APPLICATIONS

- ◆ Smart phone、Tablet PC、Tactile feedback

DESCRIPTION

AW87359 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 3rd Smart K audio amplifier. AW87359 integrates awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87359 integrated efficiency up to 90% of high voltage DO-Chargepump technology, significantly improving the dynamic range of the music output. AW87359 noise floor is as low as to 38μV at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87359 support speaker and high power receiver stereo applications; supports speaker and receiver 2-in-1 applications, class AB/D receiver optional, ultra-low noise is 11μV.

AW87359 controls internal registers through the I²C interface. Register parameters include output voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters etc.

AW87359 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87359 features small FCQFN 2.5mmX2.0mmX0.55mm-16L package.

TYPICAL APPLICATION CIRCUIT

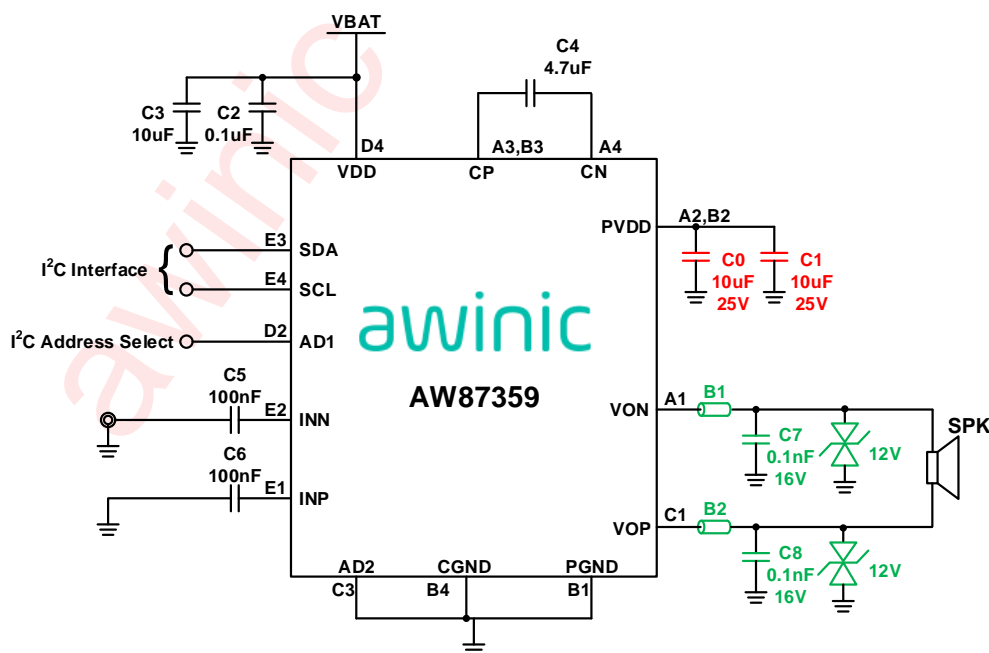


Figure 1 AW87359 Single-ended input mode Application Diagram

PIN CONFIGURATION AND TOP MARK

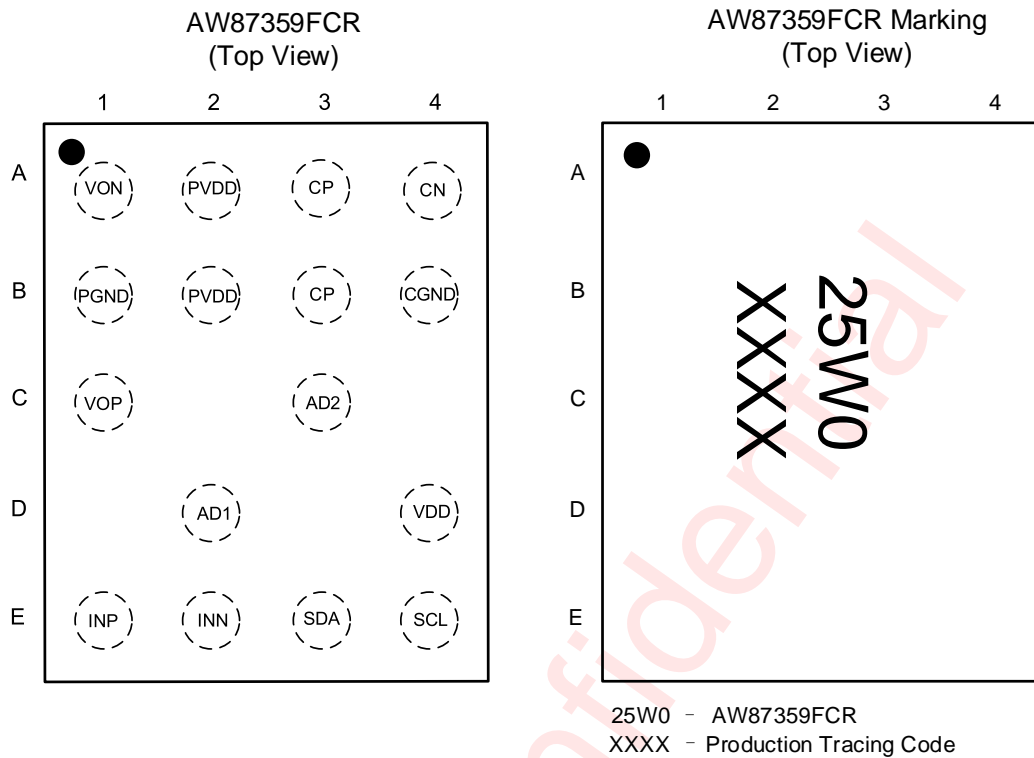


Figure 2 AW87359 Pin configuration and Top Mark

PIN DESCRIPTION

Number	Symbol	Description
A1	VON	Negative audio output terminal
A2,B2	PVDD	Charge Pump output voltage
A3,B3	CP	Positive input Charge Pump Flying Capacitance
A4	CN	Negative input Charge Pump Flying Capacitance
B1	PGND	Amplifier power ground
B4	CGND	Charge Pump power ground
C1	VOP	Positive audio output terminal
C3	AD2	I ² C address pin2
D2	AD1	I ² C address pin1
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I ² C-bus data input/output
E4	SCL	I ² C-bus clock input

FUNCTIONAL DIAGRAM

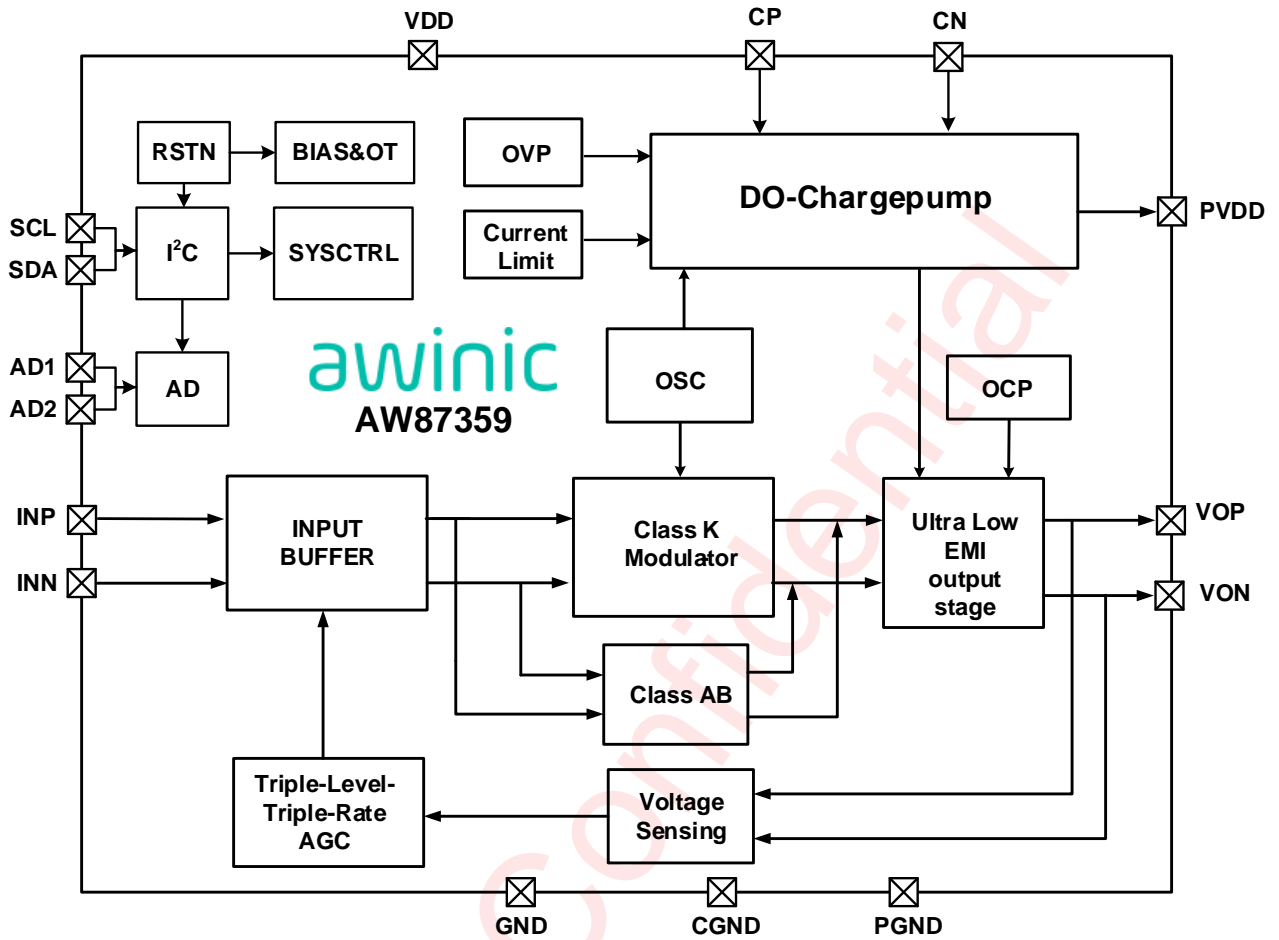
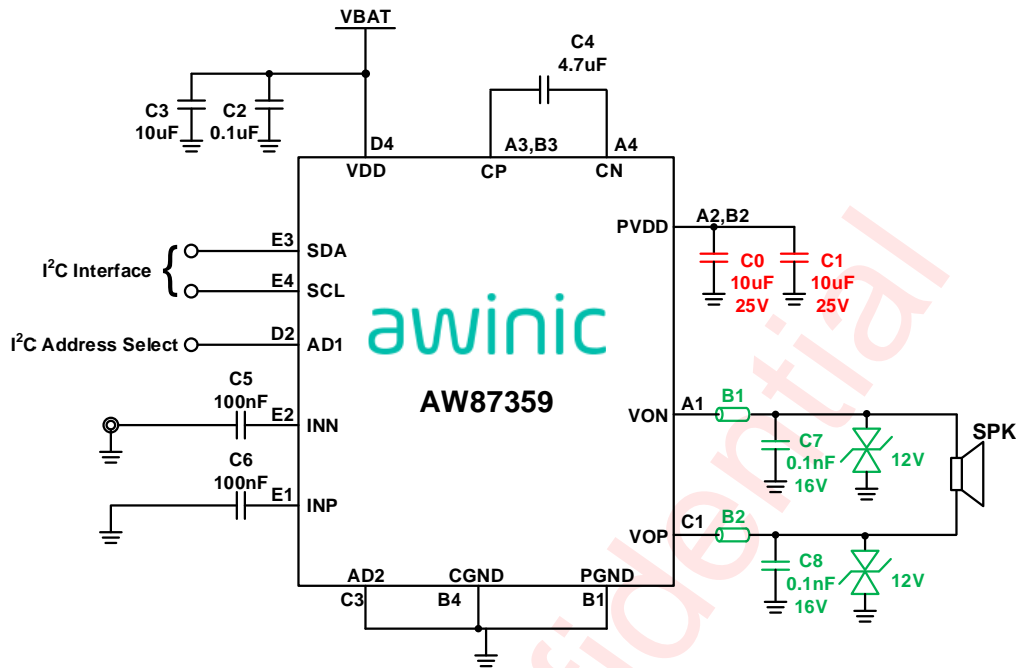


Figure 3 AW87359 Functional Diagram

TYPICAL APPLICATION CIRCUIT

Figure 4 AW87359 Single-ended input mode Application Diagram^(Note 1)

Note1: When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor.

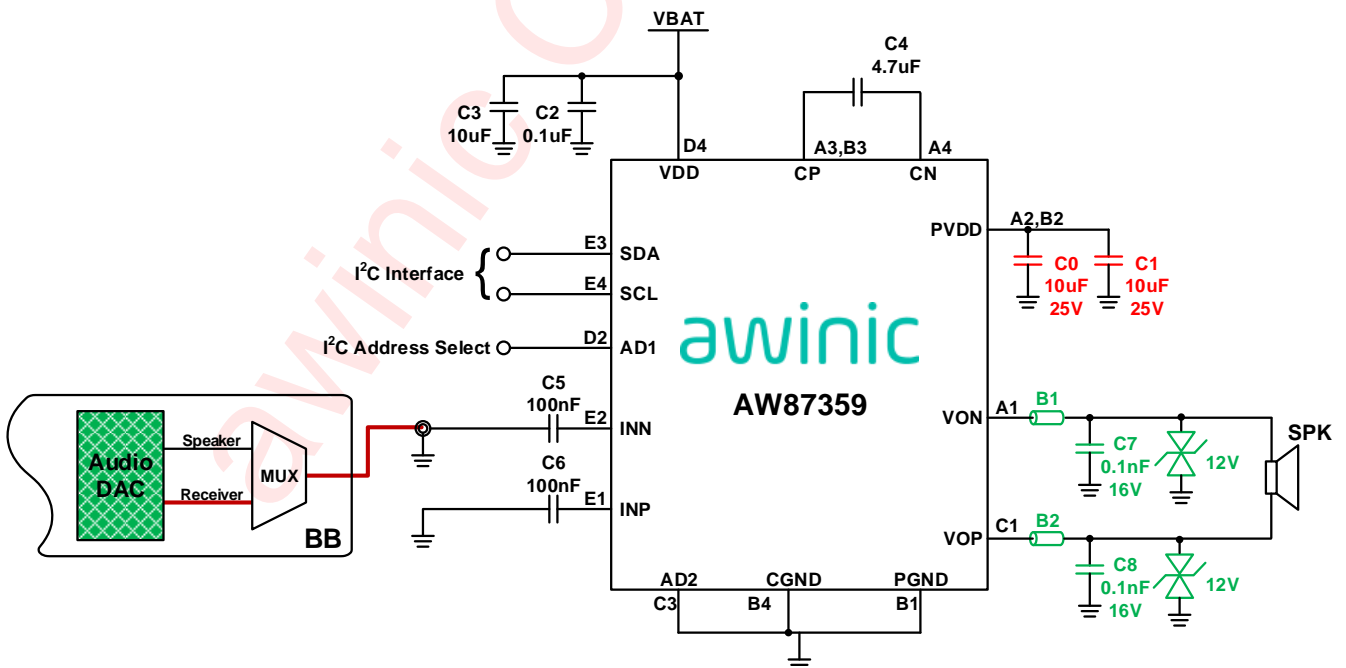


Figure 5 AW87359 Speaker & Receiver 2-in-1 Mode Application Diagram

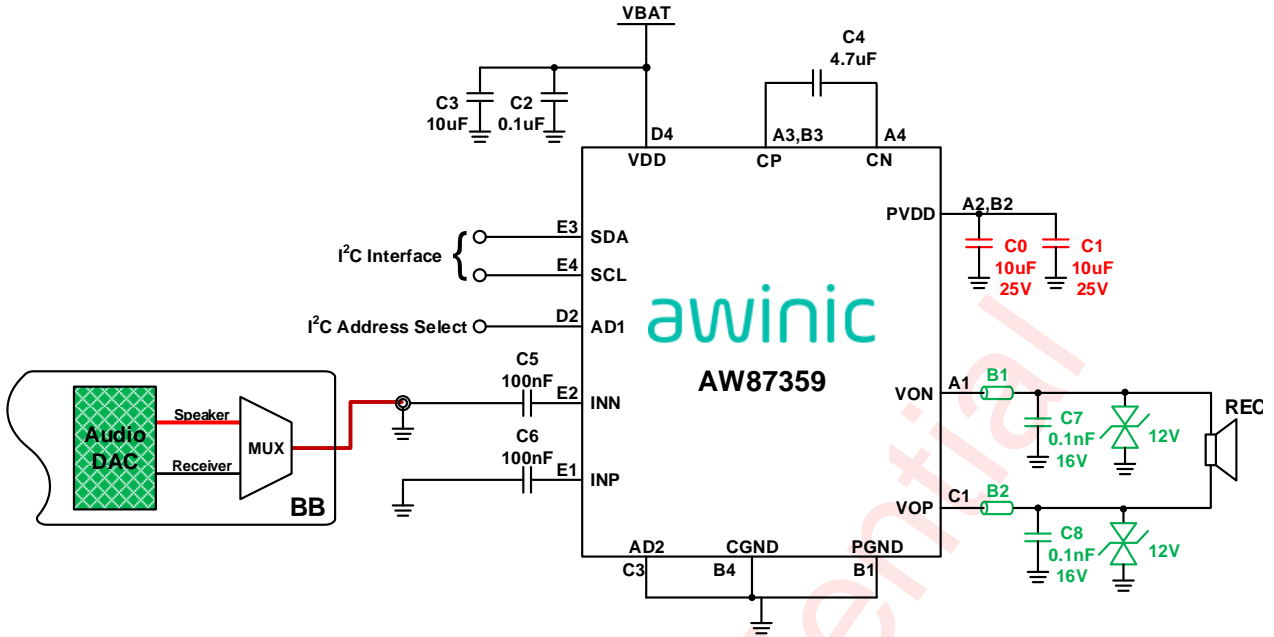


Figure 6 AW87359 High Power Receiver Stereo Mode Application

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87359FCR	-40°C ~85°C	FCQFN 2.5mmX2.0mmX0.55mm-16L	25W0	MSL1	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING (Note2)

Parameter	Range
Supply Voltage V_{DD}	-0.3V to 6V
INN,INP	-0.3V to $V_{DD}+0.3V$
Charge pump output voltage PV_{DD}	-0.3V to 9.5V
VOP,VON	-0.6V to $PV_{DD}+0.6V$
CP	-0.3V to $PV_{DD}+0.3V$
CN	-0.3V to $V_{DD}+0.3V$
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	65.2°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 3)	
HBM (human body model)	±2kV
MM (machine model)	±400V
CDM (charged-device model)	±1.5kV
Latch-up	
Test Condition: JEDEC STANDARD NO.78E	+IT: 450mA -IT: -450mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

Test method of the charge device model: ESDA/JEDEC JS-002-2014

ELECTRICAL CHARACTERISTICS

Test condition: $T_A=25^{\circ}\text{C}$, $V_{DD}=3.6\text{V}$, $PVDD\text{ OVP}=8\text{V}$, $R_L=8\Omega+33\mu\text{H}$, $f=1\text{kHz}$ (unless otherwise noted)

Parameter		Test conditions	Min	Typ	Max	Units
V_{DD}	Power supply voltage		2.8		5.5	V
UVLO	Under-voltage protection voltage			2.5		V
	Under-voltage protection hysteresis voltage			100		mV
V_{IH}	SCL, SDA, AD1, AD2 high-level input voltage		1.3		V_{DD}	V
V_{IL}	SCL, SDA, AD1, AD2 low-level input voltage		0		0.45	V
I_{SB}	Standby current	$V_{DD}=3.6\text{V}$		5		μA
T_{SD}	Over temperature protection threshold			160		$^{\circ}\text{C}$
T_{SDR}	Over temperature protection recovery threshold			130		$^{\circ}\text{C}$
T_{ON}	Turn-On time			45		ms
DO-Chargepump						
PVDD	The maximum Output voltage	$V_{DD}=2.8\text{V to }4\text{V}$, $PVDD\text{ OVP}=8\text{V}$		$2*V_{DD}$		V
		$V_{DD} >4\text{V}$		8 (Note4)		V
OVP	OVP voltage	$V_{DD} >4\text{V}$		8 (Note4)		V
	OVP hysteresis voltage	$V_{DD} >4\text{V}$		50		mV
F_{CP}	Chargepump operating frequency	$V_{DD}=2.8\text{V to }5.5\text{V}$	1.08	1.45	1.8	MHz
η_{CP}	Chargepump efficiency	$V_{DD}=4.2\text{V}$, $I_{load}=200\text{mA}$		90		%
T_{ST}	Softstart Time	No load, $CO_{UT}=20\mu\text{F}$		2.1		ms
Class K MODE						
V_{OS}	Output offset voltage	No input	-30	0	30	mV
I_q	Speaker Quiescent current	$V_{DD}=3.6\text{V}$, input ac grounded, $R_L=8\Omega+33\mu\text{H}$		14.2		mA
η	total efficiency (CP+Class D)	$V_{DD}=4.2\text{V}$, $P_o=2.5\text{W}$, $R_L=8\Omega+33\mu\text{H}$, $PVDD\text{ OVP}=8\text{V}$		80		%
V_{inp}	Recommended input signal amplitude	$V_{DD}=2.8\text{V to }5.5\text{V}$			1	Vp
F_{osc}	Modulation frequency	$V_{DD}=2.8\text{V to }5.5\text{V}$	540	720	900	kHz
P _{agc}	TLTR AGC power	$R_L=8\Omega+33\mu\text{H}$	0.72	0.8 (Note4)	0.88	W
		$R_L=6\Omega+33\mu\text{H}$	0.96	1.067 (Note4)	1.17	W
PSRR	Power supply rejection ratio	$V_{DD}=4.2\text{V}$, $V_{pp_sin}=200\text{mV}$	217Hz		82	dB
			1kHz		75	dB
SNR	Signal-to-noise ratio	$V_{DD}=4.2\text{V}$, $PVDD\text{ OVP}=8\text{V}$, $P_o=3.2\text{W}$, $A_v=18\text{dB}$, $\text{THD+N}=1\%$, $R_L=8\Omega+33\mu\text{H}$		102		dB
SNR	Signal-to-noise ratio	$V_{DD}=4.2\text{V}$, $PVDD\text{ OVP}=8\text{V}$, $P_o=0.8\text{W}$, $A_v=18\text{dB}$, $R_L=8\Omega+33\mu\text{H}$		94		dB
E_N	Speaker Output noise	$A_v=24\text{dB}$	20Hz to 20kHz, input ac grounded, A-weighting	48		μV
E_N	Speaker Output noise	$A_v=18\text{dB}$		38		μV

Parameter		Test conditions	Min	Typ	Max	Units
Av	Speaker gain	V _{DD} =2.8V to 5.5V		24 (Note4)		dB
Rini	Speaker Inner input resistance	Av=24dB		9		kΩ
	Speaker Inner input resistance	Av=18dB		18		
Fin	Speaker input Cut-off frequency	Cin=68nF, Av=24dB		260		Hz
	Speaker input Cut-off frequency	Cin=68nF, Av=18dB		130		
	Speaker input Cut-off frequency	Cin=100nF, Av=24dB		177		
	Speaker input Cut-off frequency	Cin=100nF, Av=18dB		89		
THD+N	Total harmonic distortion + noise	V _{DD} =4.2V, P _O =0.6W, R _L =8Ω+33μH, f=1kHz, PVDD OVP=8V		0.03		%
Po	Speaker Output Power	THD+N=1%, R _L =8Ω+33μH, V _{DD} =4.2V, PVDD OVP=8V		3.1		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =4.2V, PVDD OVP=8V		3.7		W
		THD+N=1%, R _L =6Ω+33μH, V _{DD} =4.2V, PVDD OVP=8V		3.5		W
		THD+N=10%, R _L =6Ω+33μH, V _{DD} =4.2V, PVDD OVP=8V		4.2		W
		THD+N=1%, R _L =8Ω+33μH, V _{DD} =3.6V, PVDD OVP=8V		2.3		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =3.6V, PVDD OVP=8V		2.9		W
		THD+N=1%, R _L =6Ω+33μH, V _{DD} =3.6V, PVDD OVP=8V		2.7		W
		THD+N=10%, R _L =6Ω+33μH, V _{DD} =3.6V, PVDD OVP=8V		3.4		W
KAB Speaker MODE (PVDD OVP=6V)						
I _q	Speaker Quiescent current	V _{DD} =3.6V, input ac grounded, R _L =8Ω+33μH		12.3		mA
η	total efficiency (CP+Class D)	V _{DD} =4.2V, P _O =1.2W, R _L =8Ω+33μH		40		%
E _N	Speaker Output noise	Av=24dB	20Hz to 20kHz, input ac grounded, A-weighting	46		μV
		Av=18dB		36		
Av	Speaker gain	V _{DD} =2.8V to 5.5V		24 (Note4)		dB
Rini	Speaker Inner input resistance	Av=24dB		9		kΩ
	Speaker Inner input resistance	Av=18dB		18		kΩ
Fin	Speaker input Cut-off frequency	Cin=68nF, Av=24dB		260		Hz
	Speaker input Cut-off frequency	Cin=68nF, Av=18dB		130		
	Speaker input Cut-off frequency	Cin=100nF, Av=24dB		177		
	Speaker input Cut-off frequency	Cin=100nF, Av=18dB		89		
PSRR	AB Speaker Power supply rejection ratio	V _{DD} =4.2V, V _{p-p_sin} =200mV	217Hz	80		dB
			1kHz	82		dB
THD+N	Total harmonic distortion + noise	V _{DD} =4.2V, P _O =1.2W, R _L =8Ω+33μH, f=1kHz		0.1		%
Po	AB Speaker Output Power	THD+N=1%, R _L =8Ω+33μH, V _{DD} =4.2V		2.1		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =4.2V		2.6		W
		THD+N=1%, R _L =8Ω+33μH, V _{DD} =3.6V		2.0		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =3.6V		2.5		W

Parameter		Test conditions		Min	Typ	Max	Units
2-in-1 Receiver MODE (1X Chargepump)							
I _q	D Receiver quiescent current (overall)	V _{DD} =3.6V, input ac grounded, R _L =8Ω+33μH			5.0		mA
	AB Receiver quiescent current (overall)	V _{DD} =3.6V, input ac grounded, R _L =8Ω+33μH			6.3		mA
η	D Receiver efficiency	V _{DD} =4.2V, P _o =0.8W, R _L =8Ω+33μH			88		%
	AB Receiver efficiency	V _{DD} =4.2V, P _o =0.4W, R _L =8Ω+33μH			47		%
A _v	D Receiver gain	V _{DD} =2.8V to 5.5V			4.5 (Note4)		dB
	AB Receiver gain	V _{DD} =2.8V to 5.5V			0 (Note4)		dB
R _{ini}	D Receiver Inner input resistance	A _v =4.5dB			48		kΩ
	AB Receiver Inner input resistance	A _v =0dB			72		kΩ
F _{in}	D Receiver input cut-off frequency	C _{in} =68nF, A _v =4.5dB			49		Hz
		C _{in} =100nF, A _v =4.5dB			33		
	AB Receiver input cut-off frequency	C _{in} =68nF, A _v =0dB			33		Hz
		C _{in} =100nF, A _v =0dB			22		
E _N	D Receiver output noise	A _v =4.5dB	20Hz to 20kHz, input ac grounded, A-weighting		16		μV
	AB Receiver output noise	A _v =0dB			11		μV
THD+N	Total harmonic distortion + noise	V _{DD} =4.2V, P _o =0.1W, R _L =8Ω+33μH, f=1kHz, D Receiver			0.01		%
		V _{DD} =4.2V, P _o =0.1W, R _L =8Ω+33μH, f=1kHz, AB Receiver			0.15		%
PSRR	D Receiver Power supply rejection ratio	V _{DD} =4.2V, V _{p-p_sin} =200mV	217Hz		78		dB
			1kHz		76		dB
	AB Receiver Power supply rejection ratio	V _{DD} =4.2V, V _{p-p_sin} =200mV	217Hz		93		dB
			1kHz		88		dB
P _o	D Receiver Output Power	THD+N=1%, R _L =8Ω+33μH, V _{DD} =4.2V			0.98		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =4.2V			1.21		W
		THD+N=1%, R _L =8Ω+33μH, V _{DD} =3.6V			0.73		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =3.6V			0.90		W
	AB Receiver Output Power	THD+N=1%, R _L =8Ω+33μH, V _{DD} =4.2V			0.46		W
		THD+N=10%, R _L =8Ω+33μH, V _{DD} =4.2V			0.63		W
Triple-Level Triple-Rate AGC							
T _{AT1}	AGC1 Attack Time				0.08 (Note4)		ms/dB
T _{AT2}	AGC2 Attack Time				0.64 (Note4)		ms/dB
T _{AT3}	AGC3 Attack Time				41 (Note4)		ms/dB
T _{RLT}	Release time				21 (Note4)		ms/dB
A _{MAX}	The maximum attenuation gain	V _{DD} =2.8V to 5.5V			-13.5		dB

Note 4: Registers are adjustable; Refer to the list of registers.

MEASUREMENT SETUP

AW87359 features switching digital output, as shown in Figure 7. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

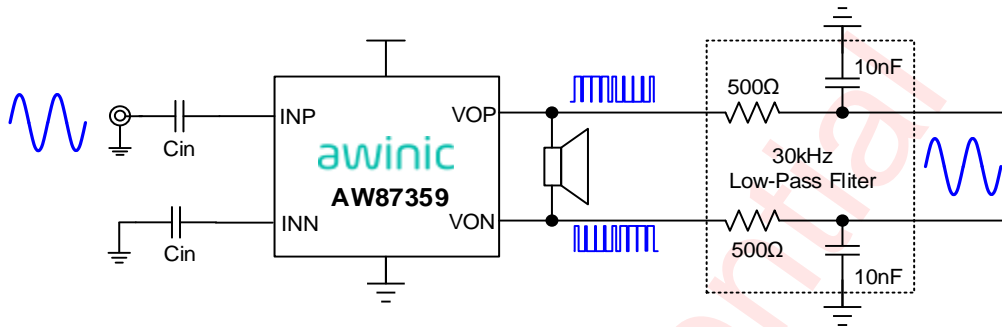


Figure 7 AW87359 Test Setup

Low pass filter uses resistance and capacitor values listed in Table 1.

R _{filter}	C _{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 1 AW87359 Recommended Values for Low Pass Filter

Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal, as shown in Figure 8:

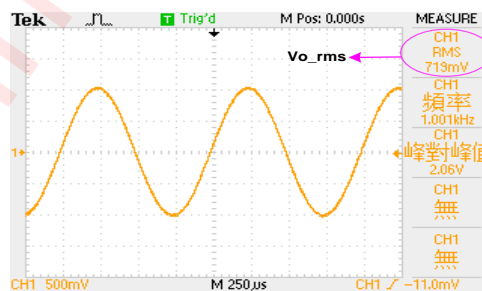
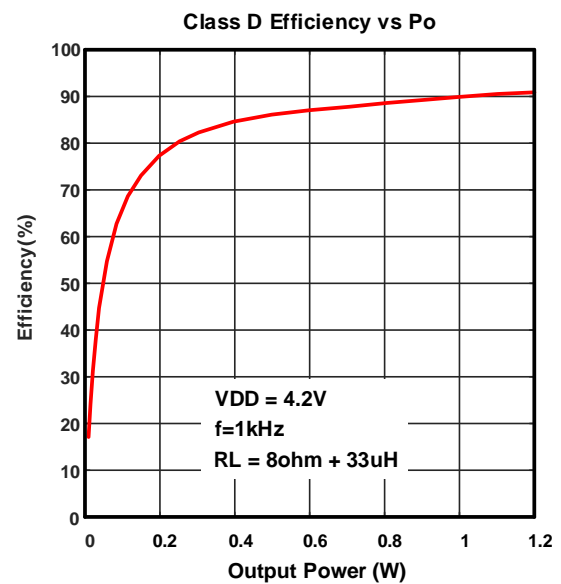
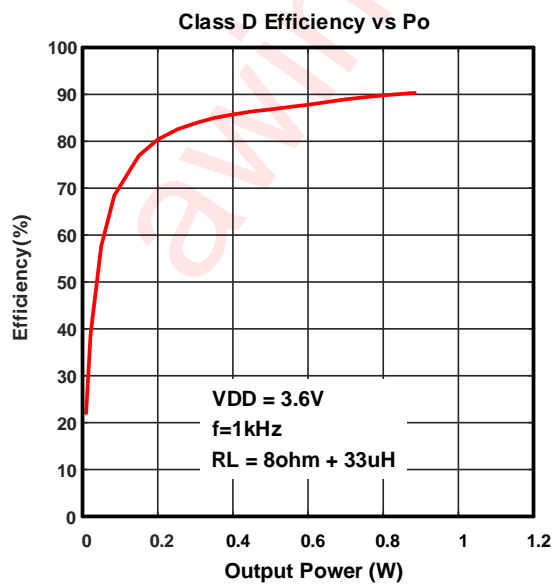
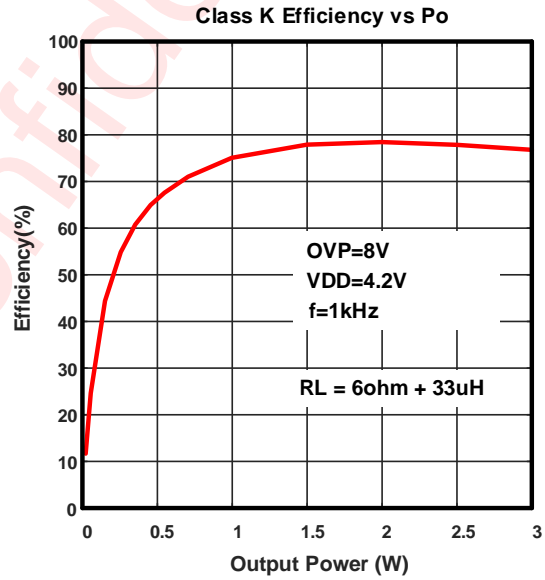
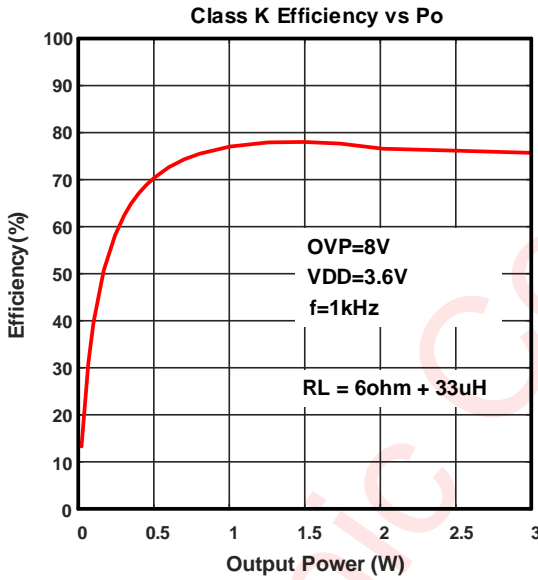
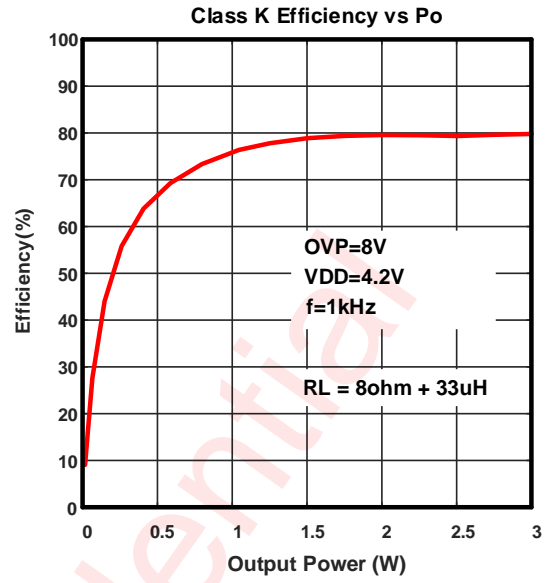
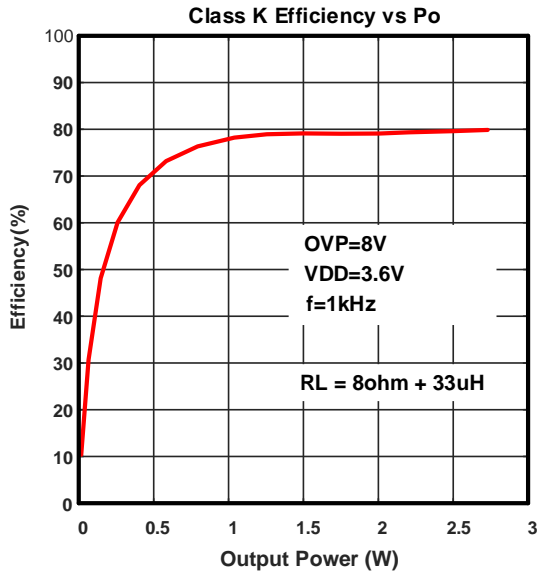


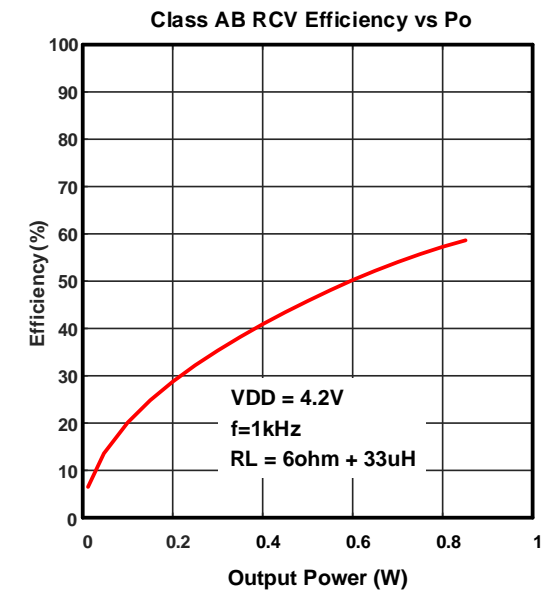
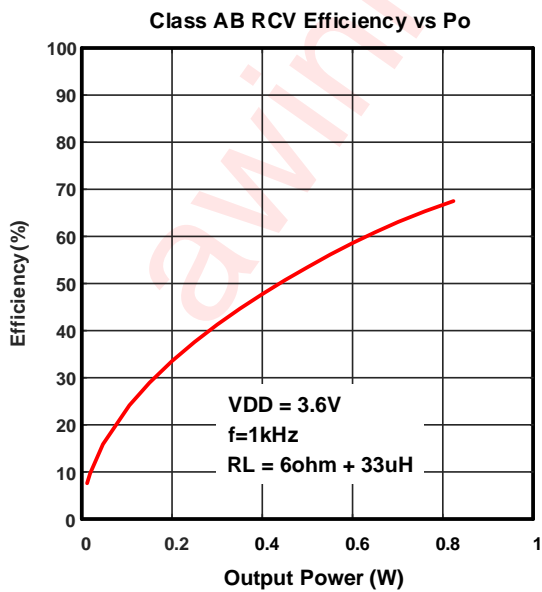
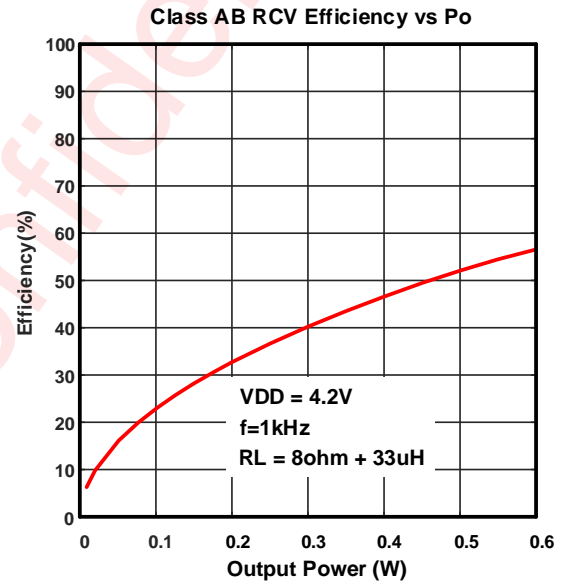
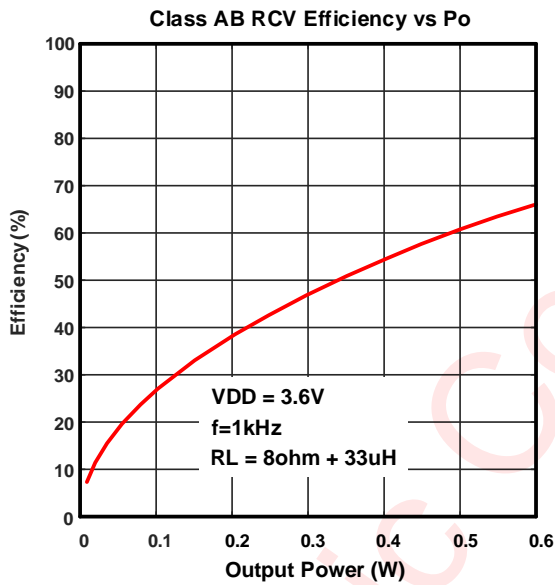
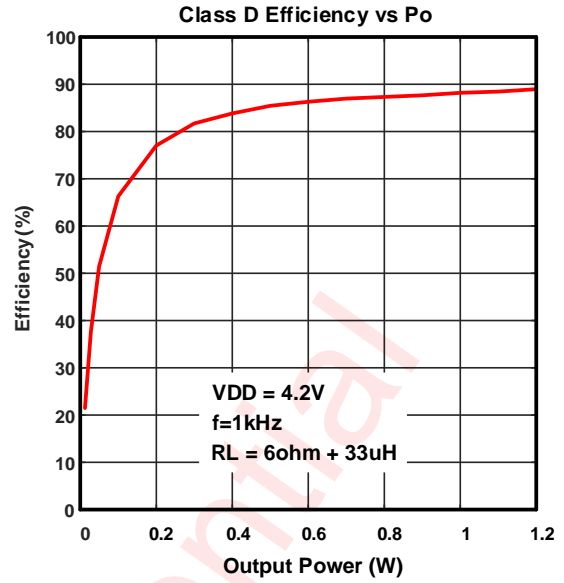
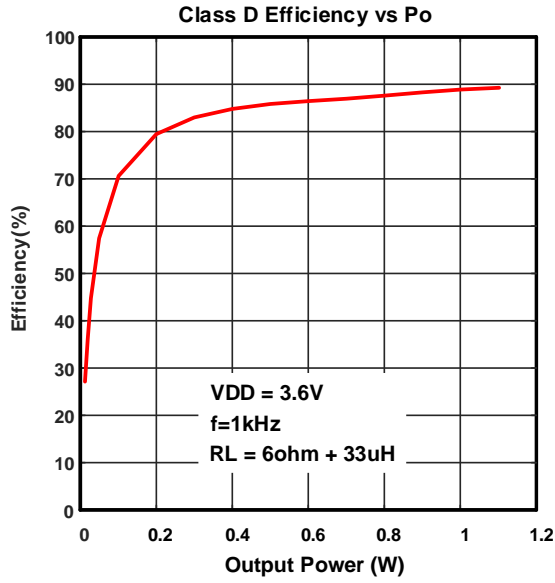
Figure 8 Output RMS Value

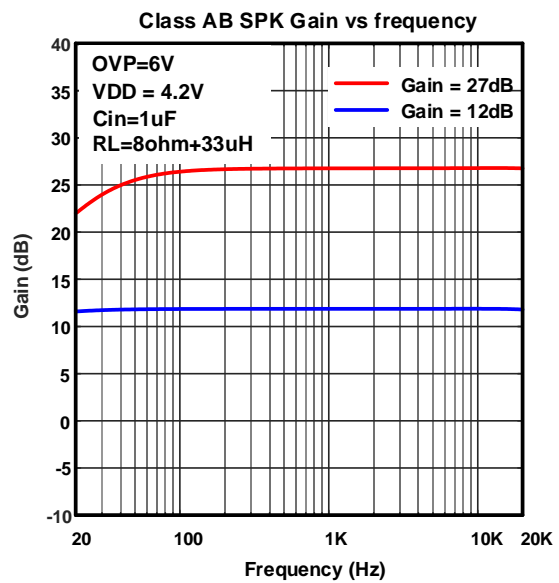
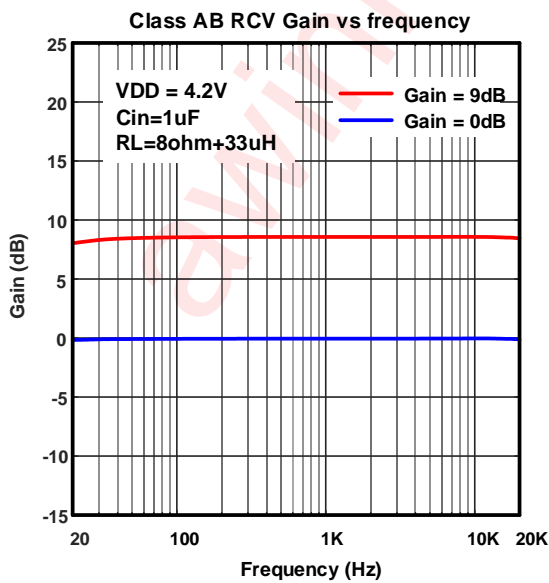
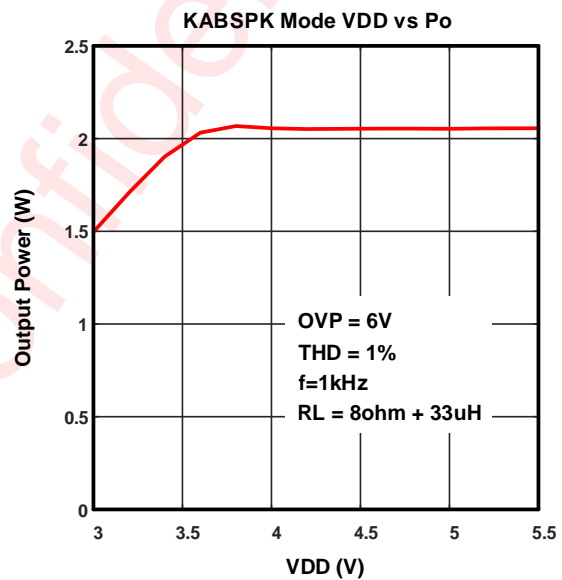
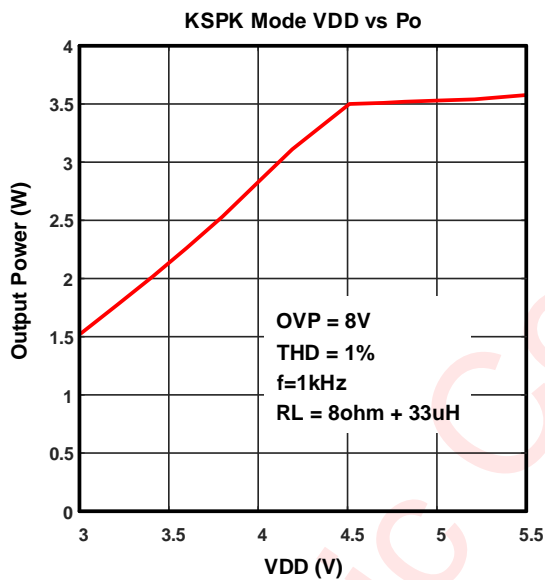
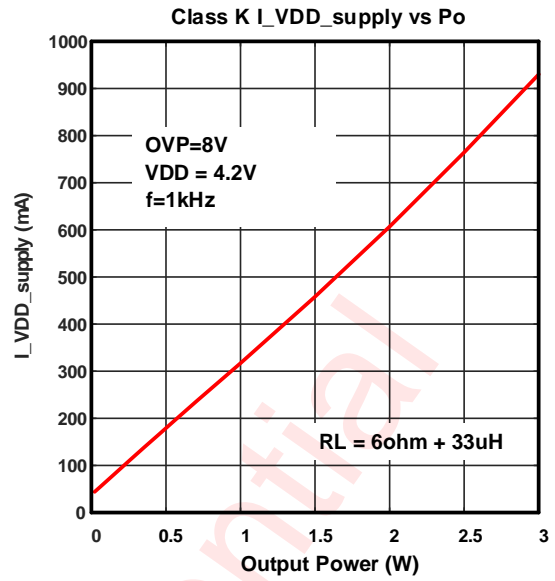
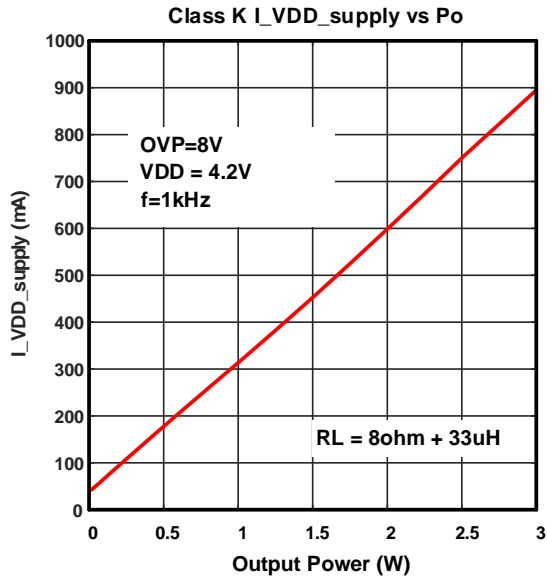
The power calculation of Speaker is as follows:

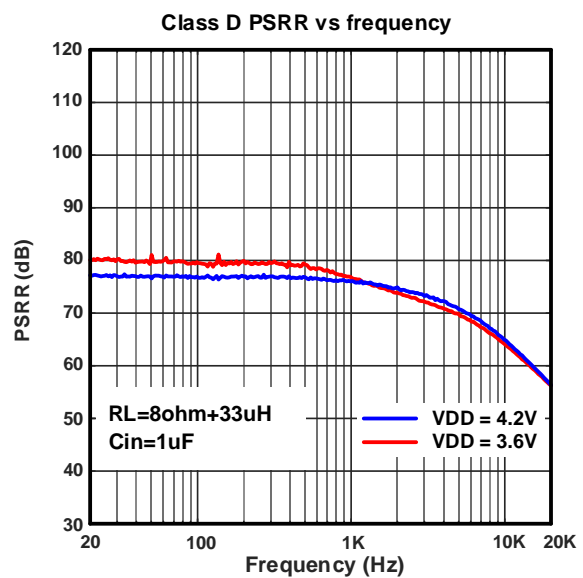
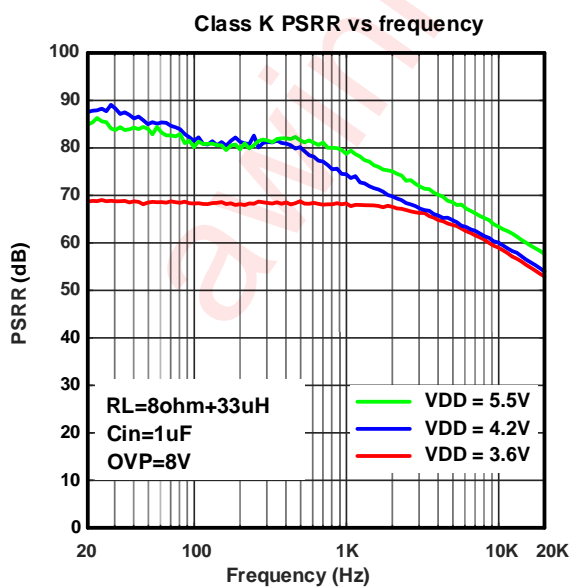
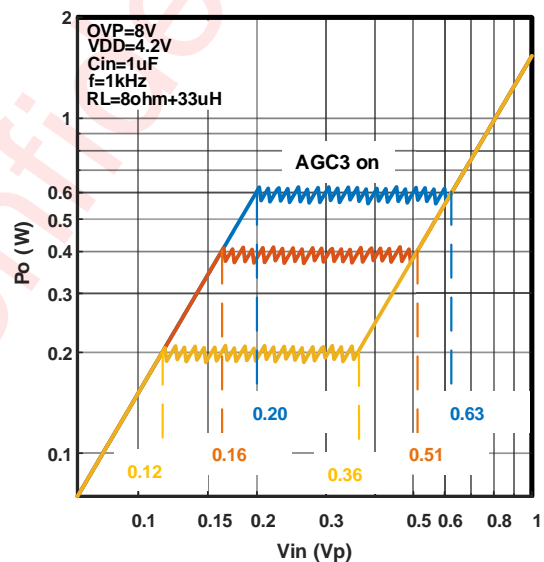
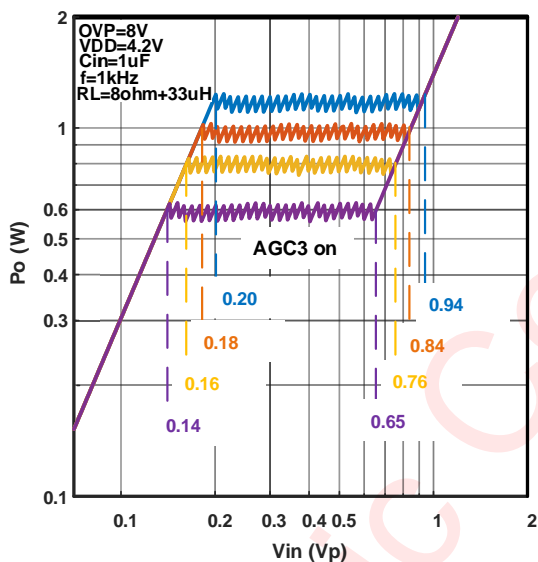
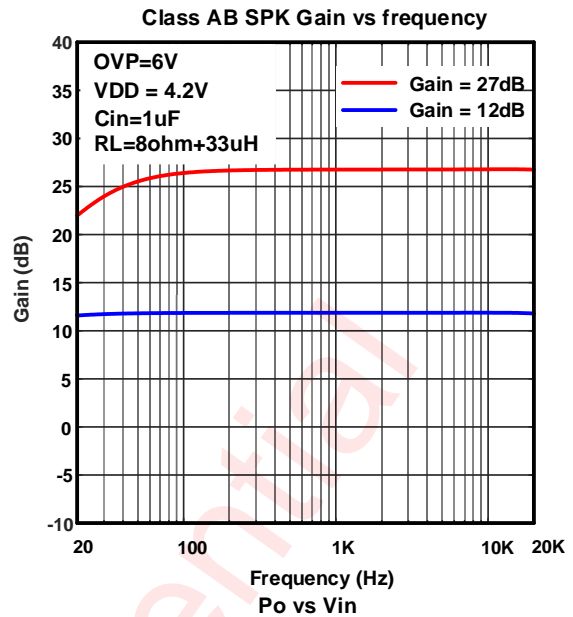
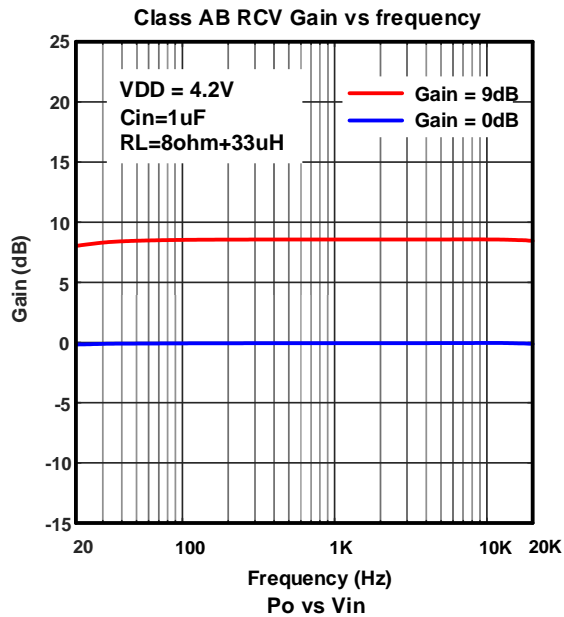
$$P_L = \frac{(V_{0_rms})^2}{R_L} \quad R_L: \text{load impedance of the speaker}$$

TYPICAL CHARATERISTICS

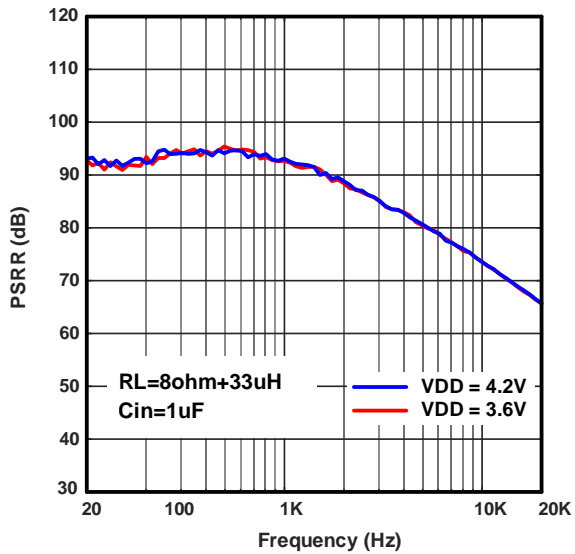




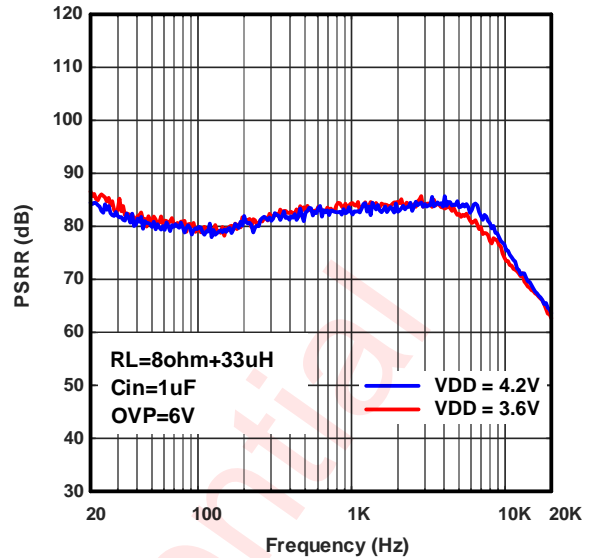




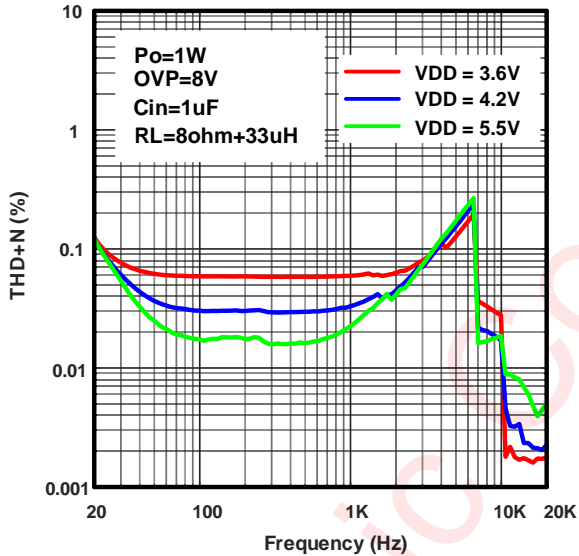
Class AB RCV PSRR vs frequency



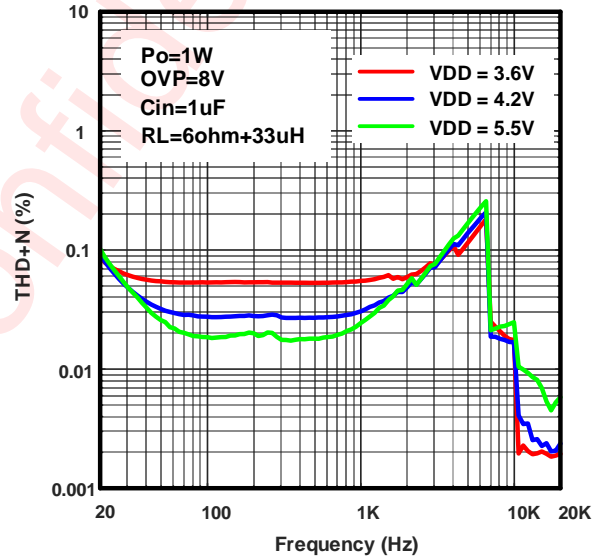
Class AB SPK PSRR vs frequency



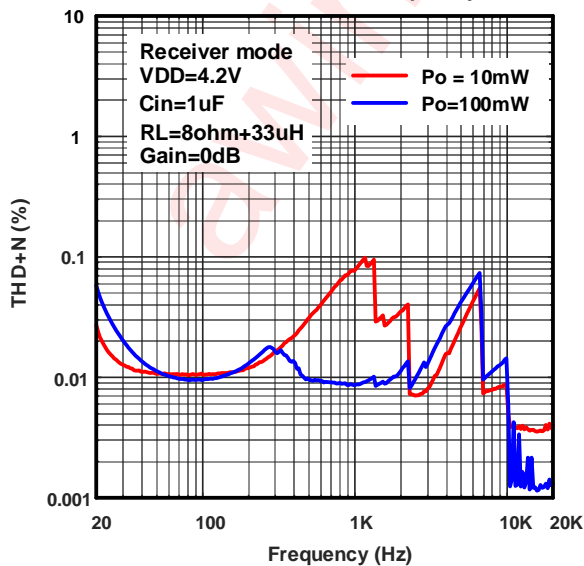
Class K THD+N vs frequency



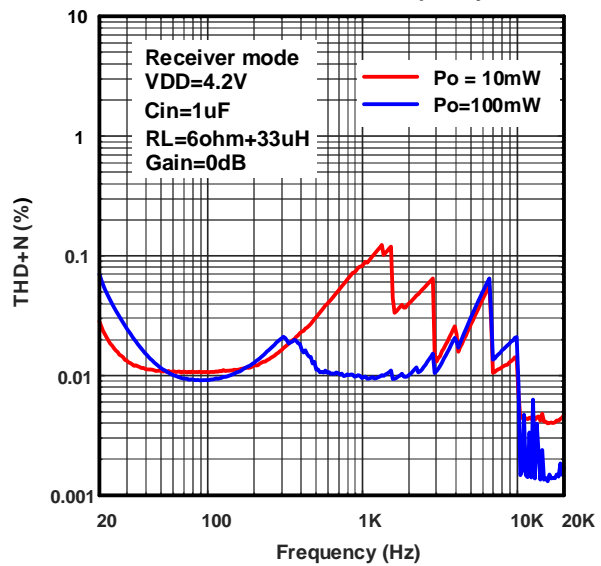
Class K THD+N vs frequency

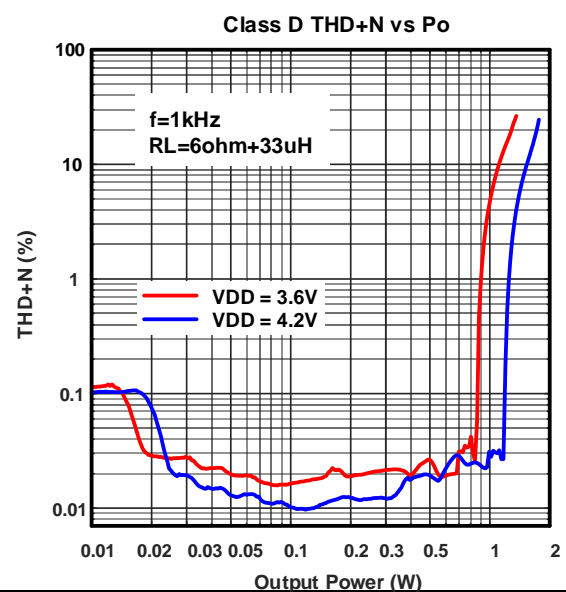
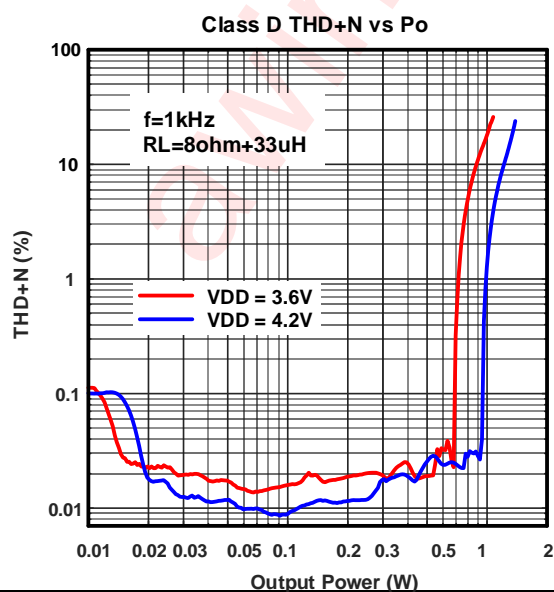
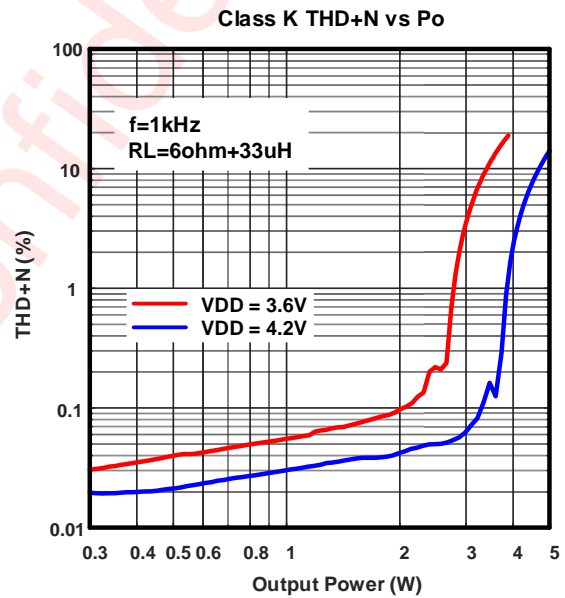
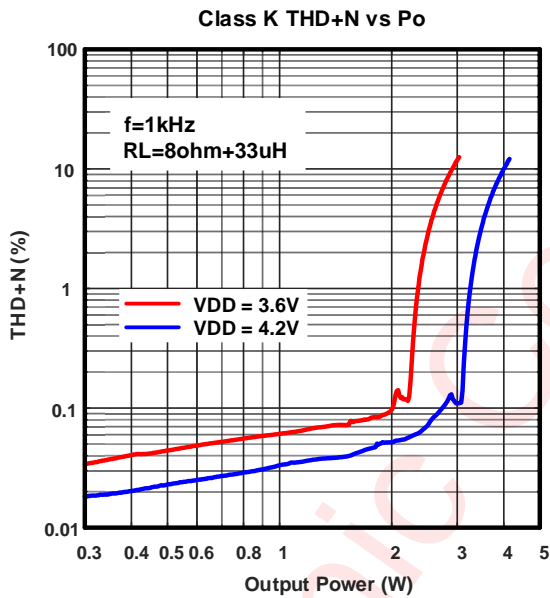
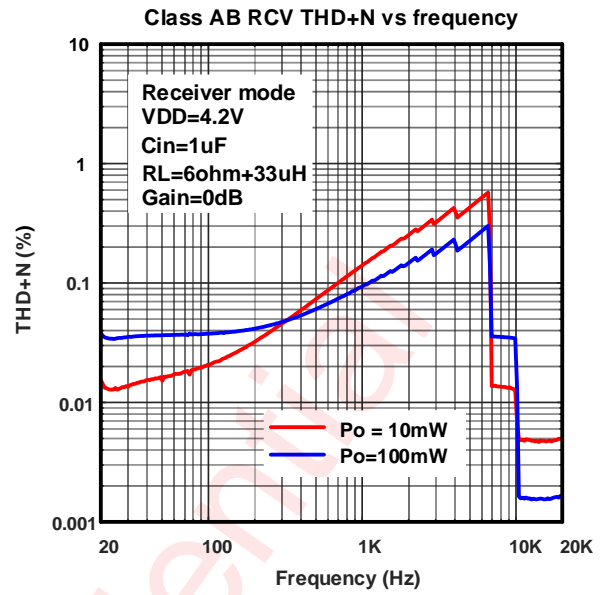
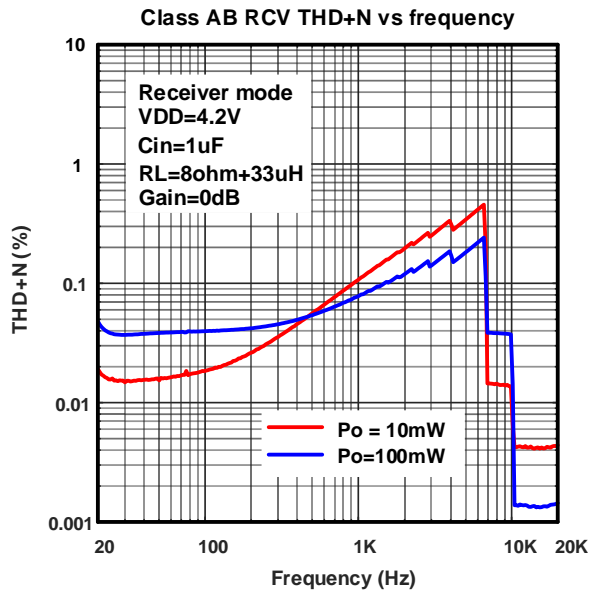


Class D THD+N vs frequency

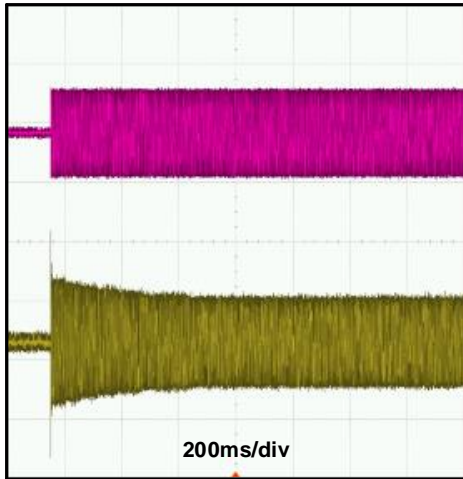


Class D THD+N vs frequency

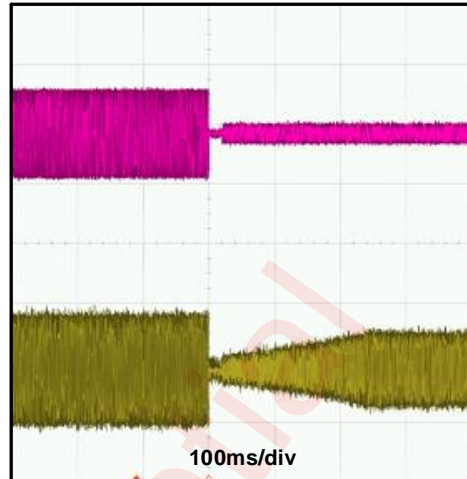




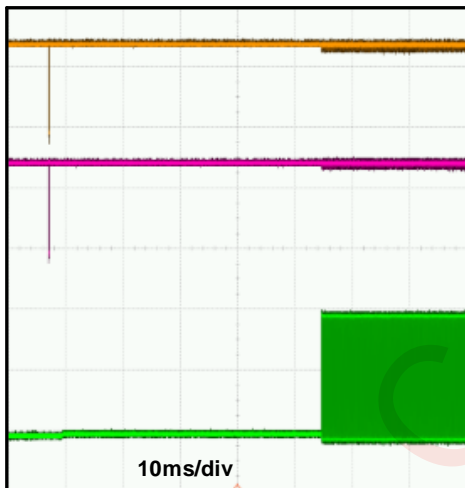
Triple-Level Triple Rate AGC Attack Timing



Triple-Level Triple Rate AGC Release Timing



Start-up sequence



Shutdown sequence



WORKING PRINCIPLE

AW87359 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, 3rd Smart K audio amplifier. AW87359 integrates awinic's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87359 integrated efficiency up to 90% of High voltage DO-Chargepump boost technology, significantly improving the dynamic range of the music output. AW87359 noise floor is as low as to 38 μ V at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87359 support Speaker and High power Receiver stereo applications; supports speaker and receiver 2-in-1 applications, class AB/D Receiver optional, ultra-low noise is 11 μ V.

AW87359 controls internal registers through the I2C interface. Register parameters include chargepump output Voltage, power amplifier gain, Triple-Level Triple-Rate AGC parameters etc.

AW87359 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87359 features small FCQFN 2.5mmX2.0mmX0.55mm-16L package.

CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87359 uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. In the process of using the phone, even if the battery voltage drops, AW87359 can still provide high quality large volume music enjoyment. The output power of AW87359 can be configured from 0.1W to 2W via I²C, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

Triple-Level Triple-Rate AGC technology

AWINIC proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the powder of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87359 Triple-Level Triple-Rate AGC technology can fit the speaker better and perform better overall performance. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

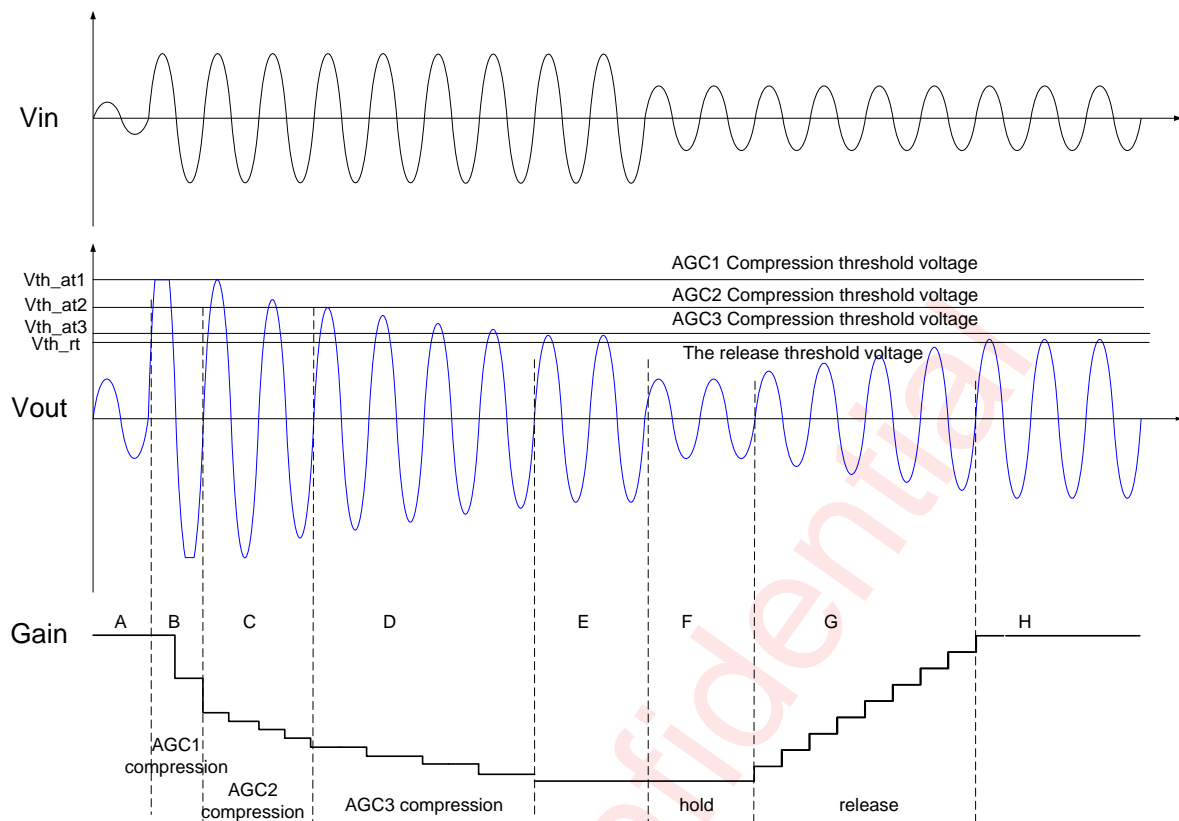


Figure 9 Triple-Level Triple-Rate AGC Operation Principle

A: Small input signal, the output voltage is lower than threshold voltage V_{th} of AGC, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts fast compression, the attack time is set through the I²C register 0x0Ah [2:1], when the output voltage is higher than V_{th_at1} , and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage V_{th_at2} , AGC2 starts work, the attack time is set through the I²C register 0x09h [4:2], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage V_{th_at2} , which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage V_{th_at2} and higher than the AGC3 attack threshold voltage V_{th_at3} , AGC3 starts work, the attack time is set through the I²C register 0x07h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below of the AGC3 attack threshold voltage V_{th_at3} , matching the speaker to achieve greater volume and better sound quality.

E: Triple-Level Triple-Rate AGC attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage V_{th_rt} , at this point, gain remains the same in the maintain time (10ms~20ms).

G: Gain increases when the time of output voltage lower than the release threshold voltage V_{th_rt} is longer than the holding time. The release time can be set through I²C register 0x07h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements.

Such as close AGC1 and AGC2, retain only AGC3, this is the single-AGC mode, similar to AW8736 (AGC3 attack time is set to 1.28ms/dB; release time is set to 41ms/dB); Close AGC2, open AGC1 and AGC3, this is Multi_level AGC. It can be set similar to AW8738 (AGC1 attack time is set to 80us/dB; AGC3 attack time is set to 0.64ms/dB; release time is set to 10.24ms/dB).

Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

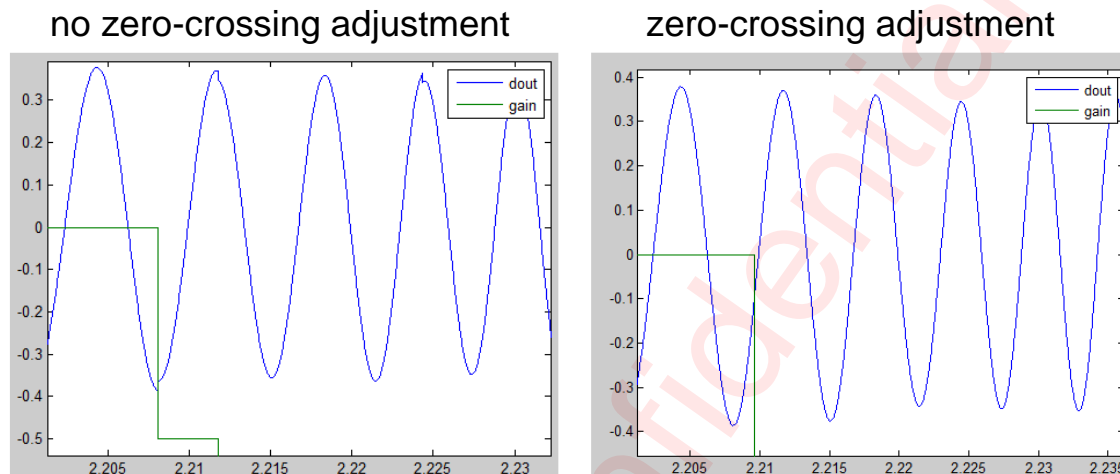


Figure 10 Zero-adjust Comparison

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

DO-Chargepump

AW87359 features DO-chargepump technology, with high efficiency and high drive capability, operating frequency 1.45MHz, built-in soft start circuit, current limiting control loop and over-voltage control loop to ensure circuit stable and reliable work.

High efficiency

AW87359 features DO-chargepump architecture, the output voltage PVDD is twice of the input voltage VDD, ideal efficiency up to 100%. The efficiency of the DO-chargepump is the ratio of the output power to input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times the DO-chargepump, the input current I_{IN} is M times of I_{OUT} , the efficiency formula is:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

Where M is the operating mode variable of the chargepump, V_{OUT} is the output voltage of chargepump, I_{OUT} is the load current. For the DO-chargepump, the output voltage is twice of the input voltage, can greatly

improve the power efficiency, taking into account the chargepump internal switching losses and IC quiescent current loss, the actual efficiency is as high as 90%.

AW87359 DO-chargepump can be set to pass-through mode and 2X chargepump mode via the register 0x02h [3] to supply power to the Class D output stage.

Chargepump structure

The basic diagram of the chargepump shows in Figure 11, the chargepump in AW87359 has four switches, the output voltage PVDD can reach twice of the input voltage through the four switches of the timing control.

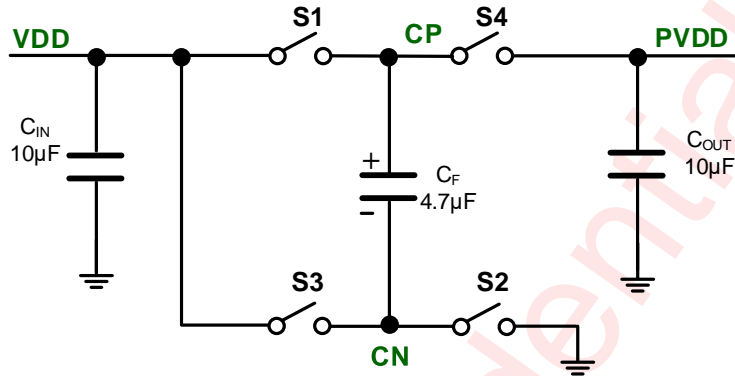


Figure 11 Chargepump Schematic Diagram

The chargepump works with two phases, in Φ_1 , as shown in the Figure 12: S1, S2 on, VDD charges the capacitor C_F .

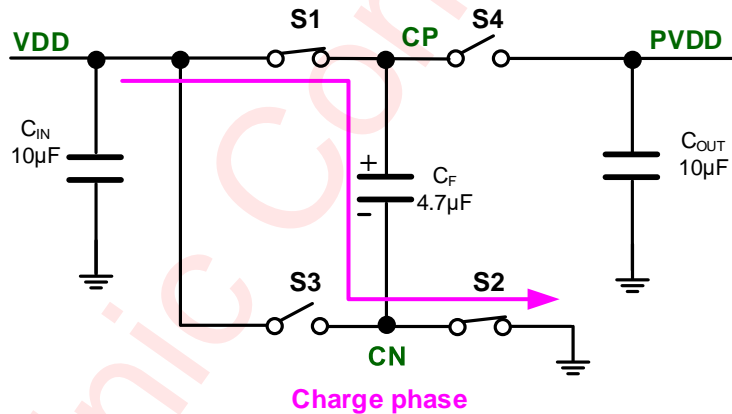


Figure 12 Φ_1 : Flying Capacitor Charging

In Φ_2 , as shown in the Figure 13: S1 and S2 off, S3 and S4 on, since the voltage across the capacitor cannot be changed abruptly, the capacitors C_F are superimposed on VDD, causing the PVDD to rise to a higher voltage.

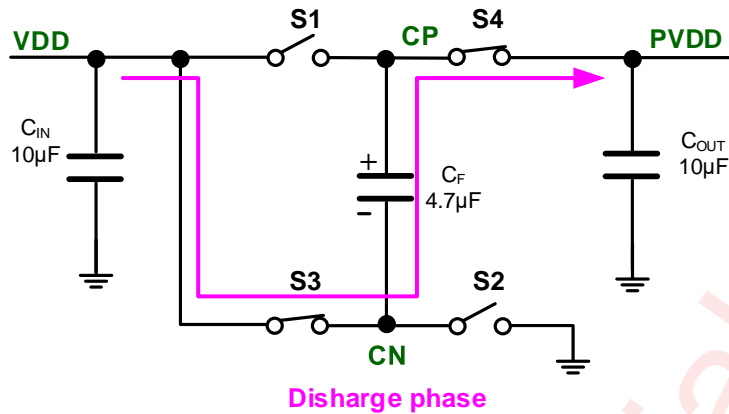


Figure 13 Φ2: Flying Capacitor Charge is Transferred to C_{OUT}

Soft start

In order to limit the inrush current of the power supply during the start of the chargepump, the chargepump has a soft start function. The current limit is 300mA during start-up.

Current limiting control

DO-chargepump architecture integrates the current limiting control loop, in normal operation, the current limiting control loop controls the maximum output current capability of the chargepump when the load is too heavy or the chargepump flows through a large current.

Over-voltage protection(OVP) control

The output voltage PVDD is twice of the input voltage VDD in DO-chargepump structure, providing high voltage rail for internal power amplifier circuits, allowing the amplifier in the lithium battery voltage range to provide greater output dynamic range, in order to achieve high volume, high-quality class K audio amplifier playback sound quality. DO-chargepump integrated over-voltage protection control loop, when the input voltage VDD is greater than 4V, the output voltage PVDD is not twice of VDD, it is determined by the over-voltage control loop. And PVDD is stable at 8.0V.

Speaker & Receiver 2-in-1 application

AW87359 built-in speaker and receiver 2-in-1 application mode, through the register settings, there are class AB-type 2-in-1 receiver mode and class D-type 2-in-1 receiver mode can be selected, the gain can be adjusted through the I²C register 0x05, adjustable range of 0~9dB, the application is very flexible. The 2-in-1 receiver mode uses the signal path of the speaker, with ultra-low distortion and strong drive capability, and eliminates the need for additional peripheral components, saving system cost and PCB layout space.

In the typical application case of Figure 5, the input capacitance C_{in}=68nF, the gain is 24dB in the speaker application mode, the input high-pass cutoff frequency is 260Hz; In 4.5dB gain class D-type 2-in-1 receiver application mode, The output noise is 16µV, the input high-pass cut-off frequency is 34Hz; In 0dB gain class AB-type 2-in-1 receiver application mode, the output noise is as low as 11µV, the input high-pass cut-off frequency is 22Hz, which is very suitable for high-definition voice applications. AW87359 can achieve speaker and receiver's 2-in-1 application without changing any hardware in the case.

High Power Receiver Stereo Applications

AW87359 built-in high-power receiver stereo application mode, makes full use of the receiver, not only takes the voice calls into account and uses the receiver as speaker, but also combines the AWINIC's proprietary TLTR-AGC technology, significantly enhancing the stereo sound quality and volume, enhancing the

dynamic music, therefore, high power receiver stereo application has gradually become a mainstream application in smart phone.

AW87359 is in the high-power receiver stereo application mode, when the register 0x02h [2] is set to 1. Gain adjustable range is 0~ 27dB by adjusting the I²C register 0x05h [4: 0], AGC3 power adjustable range is 0.1W~1.5W@8ohm receiver, 0.025W~0.375W@32ohm receiver through adjusting the I²C register 0x06h [3:0]. AW87359 can flexibly match a variety of high-power Receiver, combined with TLTR AGC technology, significantly enhance the stereo sound quality and volume, and enhance music dynamic listening.

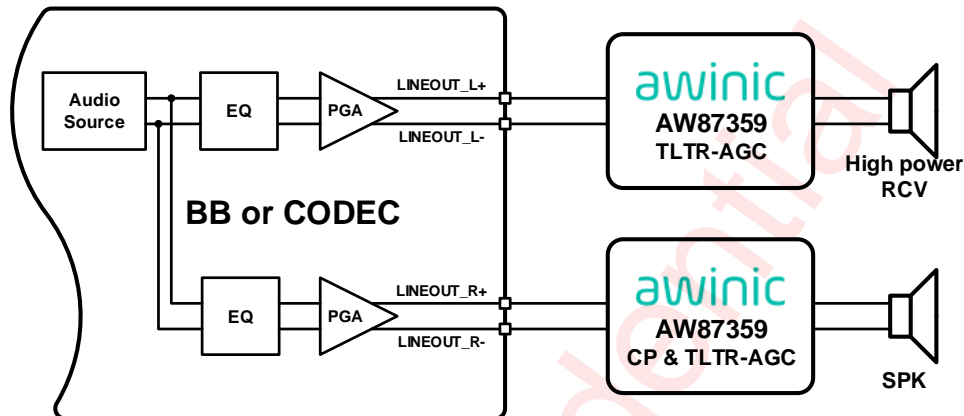


Figure 14 AW87359 High Power Receiver Stereo Mode Application

RNS(RF TDD Noise Suppression)

TDD Noise Causes

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.

With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

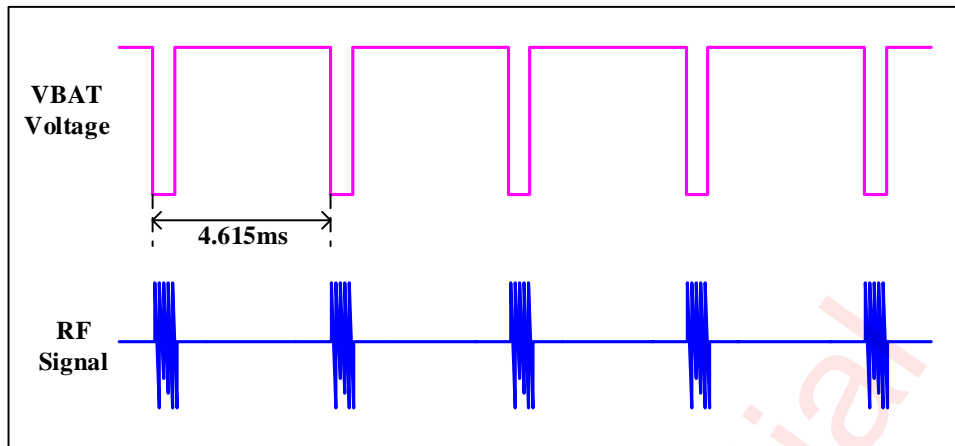


Figure 15 Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

Conduction noise suppression

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log\left(\frac{v_{dd_{ac}}}{v_{out_{ac}}}\right)$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than 60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 mV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is 60dB or 80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers

For conventional audio power amplifiers, when the input resistor R_{in} and the input capacitor C_{in} mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24V/V gain, PSRR will be weakened to 46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to 28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW87359 features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Radiation noise suppression

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW87359 features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

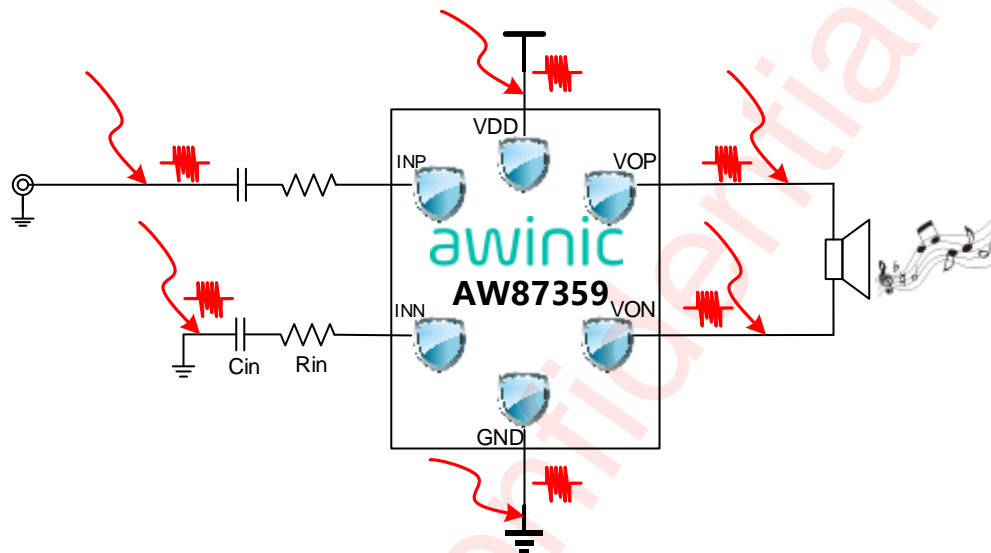


Figure 16 RF Radiation Coupling Graph

Class D amplifier without filter

When the traditional class D amplifier is in idle state of no input signal, the output will have the inverse square wave, it will directly above the load of the speaker, will form a large current power switch on the speaker, therefore we need to increase the LC filter to restore the analog audio signal at the amplifier output. The LC filter increase the cost and PCB layout area, while increase the power consumption, reduce the performance of THD+N.

The AW87359 features a Class D amplifier without a filter, eliminating the need for an output LC filter. In the idle state of no input signal, the two outputs (VOP, VON) of the amplifier are in-phase square waves and not generate idle switching currents on the speaker load. When the input signal is added to the input terminal, the duty ratio of the output is changed. The duty cycle of the VOP becomes larger and the duty cycle of the VON becomes smaller, and the difference value of the output forms the differential amplified signal on the speaker.

EEE

The AW87359 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth, fully meet FCC CLASS B specification requirements.

Pop-Click Suppression

The AW87359 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

over temperature protection

When the AW87359 operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C).

Automatic recovery of overcurrent protection

AW87359 with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, AW87359 internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting.

awinic Confidential

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f _{SCL}	SCL Clock frequency			400	kHz
2	t _{LOW}	SCL Low level Duration	1.3			μs
3	t _{HIGH}	SCL High level Duration	0.6			μs
4	t _{RISE}	SCL, SDA rise time			0.3	μs
5	t _{FALL}	SCL, SDA fall time			0.3	μs
6	t _{SU:STA}	Setup time SCL to START state	0.6			μs
7	t _{HD:STA}	(Repeat-start) Start condition hold time	0.6			μs
8	t _{SU:STO}	Stop condition setup time	0.6			μs
9	t _{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	t _{SU:DAT}	SDA setup time	0.1			μs
11	t _{HD:DAT}	SDA hold time	10			ns

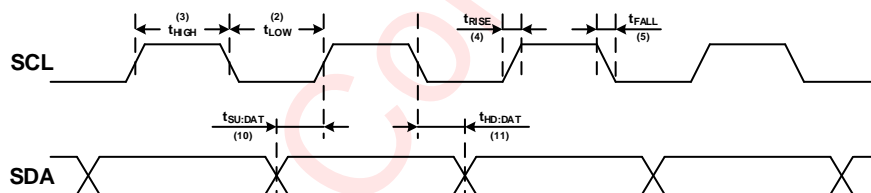


Figure 17 SCL and SDA timing relationships in the data transmission process

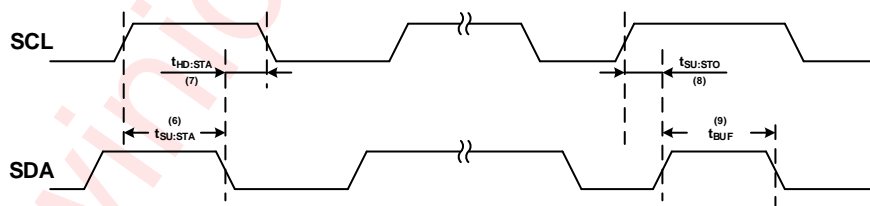


Figure 18 the Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL

default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state: The SCL maintain a high level, SDA from high to low level

STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 19.

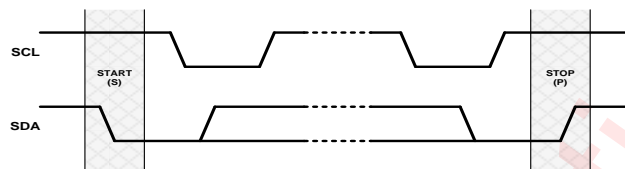


Figure 19 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 20. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an acknowledgment bit (Acknowledge, ACK or A), as shown in Figure 21. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

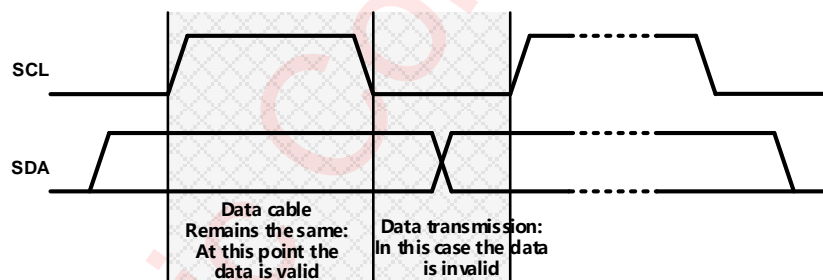


Figure 20 The Data Transfer Rules on the I²C Bus

The whole process of actual data transmission is shown in Figure 21. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag (R/\overline{W}). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

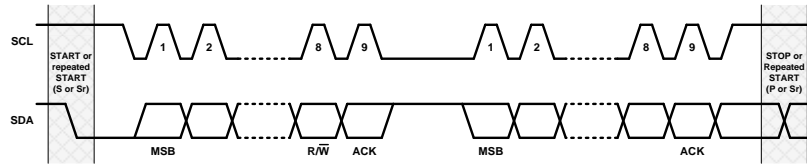


Figure 21 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87359 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 22:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\bar{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87359 register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87359, within AW87359 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

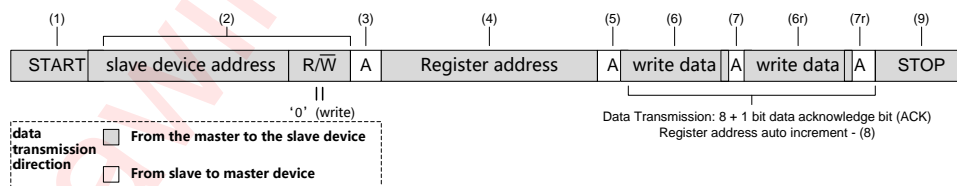


Figure 22 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87359 as the

slave device, the transmission process carried out by following steps listed in Figure 23:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW87359, and followed by a "read / write" flag ($R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW87359 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W} = 1$) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

AW87359 automatically increment register address once after the slave sent each acknowledge bit (ACK).

The master device generates the STOP state to end the data transmission.

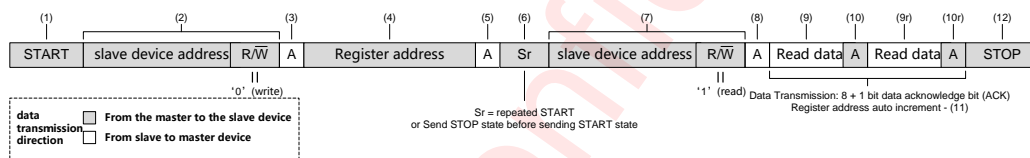


Figure 23 Reading Process (Data Transmission Direction Remains the Same)

Register List

name	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Chip ID	0x00	0	1	0	1	1	0	0	1
SYCTRL	0x01	0	0	0	0	EN_PA	EN_CP	0	EN_SW
MODECTRL	0x02	0	0	0	0	EN_2X	EN_SPK ⁽¹⁾	EN_LG	EN_AB ⁽²⁾
CPOVP	0x03	0	0	0	0	CP_OVP ⁽³⁾ [3]	CP_OVP ⁽³⁾ [2]	CP_OVP ⁽³⁾ [1]	CP_OVP ⁽³⁾ [0]
CPP	0x04	0	0	0	0	0	1	0	1
Gain	0x05	0	0	0	Gain [4]	Gain [3]	Gain [2]	Gain [1]	Gain [0]
AGC3_Po	0x06	0	0	0	0	AGC3_Po[3]	AGC3_Po[2]	AGC3_Po[1]	AGC3_Po[0]
AGC3	0x07	AGC3_RT[2]	AGC3_RT[1]	AGC3_RT[0]	AGC3_AT[2]	AGC3_AT[1]	AGC3_AT[0]	AGC3FAST[1]	AGC3FAST[0]
AGC2_Po	0x08	0	0	0	0	AGC2_Po[3]	AGC2_Po[2]	AGC2_Po[1]	AGC2_Po[0]
AGC2	0x09	0	0	0	AGC2_AT[2]	AGC2_AT[1]	AGC2_AT[0]	AGC2FAST[1]	AGC2FAST[0]
AGC1	0x0A	0	1	0	0	1	AGC1_AT[1]	AGC1_AT[0]	PD_AGC1

(1) EN_SPK: enable speaker application

(2) EN_AB: enable class AB application

(3) CP_OVP: chargepump OVP voltage

register	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A
Default	0x59	0x0C	0x0C	0x08	0x05	0x00 (EN_SPK=1 && EN_LG=1) (EN_SPK=0)	0x00 (EN_SPK=1 && EN_LG=1)	0x4 E	0x06 (EN_SPK =1)	0x08	0x4A
						0x10 (EN_SPK=1 && EN_LG=0)	0x07 (EN_SPK=1 && EN_LG=0)		0x09 (EN_SPK =0)		
							0x0F (EN_SPK=0)				

Table 2 AW87359 Register Default Value

Any register address which is more than 0x0A and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87359's I2C address is 10110A2A1, as shown in Table 3, in order to avoid conflict with other I2C devices address, you can pull up or pull-down AW87359 of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	1	1	0	A2	A1	R/W

Table 3 AW87359 Address Byte

CHIP ID Register (address: 0x00)

I ² C Bit	Name	R/W	Default	Description
7:0	IDCODE	R	0x59	Chip ID will be returned after reading. All configuration registers will be reset to default values after 0xAA is written.

SYSTEM CONTROL (SYCTRL) Register (address: 0x01)

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3	EN_PA	R/W	1	Power Amplifier enable
				0: Power Amplifier disable 1: Power Amplifier enable, the PA working mode depends on EN_AB
2	EN_CP	R/W	1	Chargepump Enable

				0: Charge Pump disable, PVDD=0 1: Charge Pump enable, the CP working mode depends on EN_2X
1	--	--	0	Reserved and Unused
0	EN_SW	R/W	0	CP and PA software power-up 0: CP and PA software power-down 1: CP and PA software power-up

MODE CONTROL (MODECTRL) Register (address: 0x02)

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	000	Reserved and Unused
3	EN_2X	R/W	1	2X Charge Pump Mode enable 0: 1X Direct Through Mode enable 1: 2X Charge Pump Mode enable
2	EN_SPK	R/W	1	SPK Mode or RCV Mode enable 0: SPK Mode disable 1: SPK Mode enable
1	EN_LG	R/W	0	Low Gain enable 0: Low Gain disable 1: Low Gain enable
0	EN_AB	R/W	0	Class AB enable, Class D disable 0: Class AB disable, Class D enable 1: Class AB enable, Class D disable

CHARGE PUMP OUTPUT VOLTAGE (CPOVP) Register (address: 0x03)

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	CP_OVP	R/W	1000	Setting Chargepump OVP Voltage 1011~1111: reserved. If set, turns to default. 0000: 6.0V 0001: 6.25V 0010: 6.5V 0011: 6.75V 0100: 7V 0101: 7.25V 0110: 7.5V 0111: 7.75V 1000: 8V 1001: 8.25V 1010: 8.5V
3:0	CP_OVP	R/W	0000	Charge Pump OVP voltage setting. When EN_AB=1 && EN_2X=1 0011~1111: reserved. If set, turns to default. 0000: 6.0V 0001: 6.25V 0010: 6.5V

CHAREPUMP PARAMETER (CPP) Register (address: 0x04)

I ² C Bit	Name	R/W	Default	Description
7:0	--	--	00000101	Reserved and Unused

GAIN CONTROL (Gain) Register (address: 0x05)

For EN_SPK=1 && EN_LG=1:

I ² C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused

4:0	Gain	R/W	00000	Power Amplifier Gain setting
				10011~11111: reserved. If set, turns to default.
				00000: 0dB
				00001: 1.5dB
				00010: 3dB
				00011: 4.5dB
				00100: 6dB
				00101: 7.5dB
				00110: 9dB
				00111: 10.5dB
				01000: 12dB
				01001: 13.5dB
				01010: 15dB
				01011: 16.5dB
				01100: 18dB
				01101: 19.5dB
				01110: 21dB
01111: 22.5dB				
10000: 24dB				
10001: 25.5dB				
10010: 27dB				

For EN_SPK=1 && EN_LG=0:

I ² C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:0	Gain	R/W	10000	Power Amplifier Gain setting
				00000~00111, 10011~11111: reserved. If set, turns to default.
				01000: 12dB
				01001: 13.5dB
				01010: 15dB
				01011: 16.5dB
				01100: 18dB
				01101: 19.5dB
				01110: 21dB
				01111: 22.5dB
				10000: 24dB
				10001: 25.5dB
10010: 27dB				

For EN_SPK=0:

I ² C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:0	Gain	R/W	00000	Power Amplifier Gain setting
				00111~11111: reserved. If set, turns to default.
				00000: 0dB
				00001: 1.5dB
				00010: 3dB
				00011: 4.5dB
				00100: 6dB
				00101: 7.5dB
				00110: 9dB

AGC3 OUTPUT POWER (AGC3_Po) Register (address: 0x06)

For EN_SPK=1 && EN_LG=1:

I ² C Bit	Name	R/W	Default	Description
----------------------	------	-----	---------	-------------

7:4	--	--	000	Reserved and Unused
3:0	AGC3_PO	R/W	0000	AGC3 Output Power setting
				0000: 0.1W@8Ω
				0001: 0.2W@8Ω
				0010: 0.3W@8Ω
				0011: 0.4W@8Ω
				0100: 0.5W@8Ω
				0101: 0.6W@8Ω
				0110: 0.7W@8Ω
				0111: 0.8W@8Ω
				1000: 0.9W@8Ω
				1001: 1.0W@8Ω
				1010: 1.1W@8Ω
				1011: 1.2W@8Ω
				1100: 1.3W@8Ω
1101: 1.4W@8Ω				
1110: 1.5W@8Ω				
1111: AGC3 OFF				

For EN_SPK=1 && EN_LG=0:

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	000	Reserved and Unused
3:0	AGC3_PO	R/W	0111	AGC3 Output Power setting
				0000~0011: reserved. If set, turns to default.
				0100: 0.5W@8Ω
				0101: 0.6W@8Ω
				0110: 0.7W@8Ω
				0111: 0.8W@8Ω
				1000: 0.9W@8Ω
				1001: 1.0W@8Ω
				1010: 1.1W@8Ω
				1011: 1.2W@8Ω
				1100: 1.3W@8Ω
				1101: 1.4W@8Ω
				1110: 1.5W@8Ω
				1111: AGC3 OFF

For EN_SPK=0:

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	000	Reserved and Unused
3:0	AGC3_PO	R/W	1111	AGC3 Output Power setting
				0000~1110: reserved. If set, turns to default.
				1111: AGC3 OFF

AGC3 PARAMETER (AGC3) Register (address: 0x07)

I ² C Bit	Name	R/W	Default	Description
7:5	AGC3_RT	R/W	010	AGC3 Release Time setting
				000: 5.12ms/dB
				001: 10.24ms/dB
				010: 20.48ms/dB
				011: 41ms/dB
				100: 82ms/dB
				101: 164ms/dB
				110: 328ms/dB
111: 656ms/dB				
4:2	AGC3_AT	R/W	011	AGC3 Attack Time setting

				000: 1.28ms/dB
				001: 2.56ms/dB
				010: 10.24ms/dB
				011: 41ms/dB
				100: 82ms/dB
				101: 164ms/dB
				110: 328ms/dB
				111: 656ms/dB
1:0	AGC3FSAT	R/W	10	AGC3 First Attack Time setting
				00: 10.24ms/dB
				01: 20.48ms/dB
				10: 41ms/dB
				11: 82ms/dB

AGC2 OUTPUT POWER(AGC2_Po) Register (address: 0x08)

For EN_SPK=1:

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC2_PO	R/W	0110	AGC2 Output Power setting
				1010~1111: reserved. If set, turns to default.
				0000: 0.4W@8Ω
				0001: 0.6W@8Ω
				0010: 0.8W@8Ω
				0011: 1.0W@8Ω
				0100: 1.2W@8Ω
				0101: 1.4W@8Ω
				0110: 1.6W@8Ω
				0111: 1.8W@8Ω
				1000: 2.0W@8Ω
				1001: AGC2 OFF

For EN_SPK=0:

I ² C Bit	Name	R/W	Default	Description
7:4	--	--	0000	Reserved and Unused
3:0	AGC2_PO	R/W	1001	AGC2 Output Power setting
				0000~1000, 1010~1111: reserved. If set, turns to default.
				1001: AGC2 OFF

AGC2 PARAMETER (AGC2) Register (address: 0x09)

I ² C Bit	Name	R/W	Default	Description
7:5	--	--	000	Reserved and Unused
4:2	AGC2_AT	R/W	010	AGC2 Attack Time setting
				000: 0.16ms/dB
				001: 0.32ms/dB
				010: 0.64ms/dB
				011: 2.56ms/dB
				100: 10.24ms/dB
				101: 41ms/dB
				110: 82ms/dB
				111: 164ms/dB
1:0	AGC2FAST	R/W	00	AGC2 First Attack Time setting
				00: 0.16ms/dB
				01: 0.64ms/dB
				10: 2.56ms/dB

				11: 10.24ms/dB
--	--	--	--	----------------

AGC1 PARAMETER (AGC1) Register (address: 0x0A)

I ² C Bit	Name	R/W	Default	Description
7:3	--	--	01001	Reserved and Unused
2:1	AGC1_AT	R/W	01	AGC1 Attack Time
				00: 0.04ms/dB
				01: 0.08ms/dB
				10: 0.16ms/dB
				11: 0.32ms/dB
0	PD_AGC1	R/W	0	AGC1 function power-down
				0: AGC1 function power-up
				1: AGC1 function power-down

APPLICATION INFORMATION

Capacitor Selection

The output capacitor of chargepump is usually within the range $0.1\mu\text{F}\sim 47\mu\text{F}$, It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO_3), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

a) temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive. X5R capacitance change within $\pm 15\%$ in temperature range of 55°C to 85°C , X7R capacitance change within $\pm 15\%$ in temperature range of $-55^\circ\text{C}\sim 125^\circ\text{C}$. The output capacitance of the AW87359's chargepump recommends X5R ceramic capacitors.

b) Voltage Stability

Class II type capacitor has poor voltage stability — Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V, the package size is 0805, 1206 or 0603, the capacitance value is $10\mu\text{F}$. The capacitor's voltage stability of different types of capacitor is as shown below:

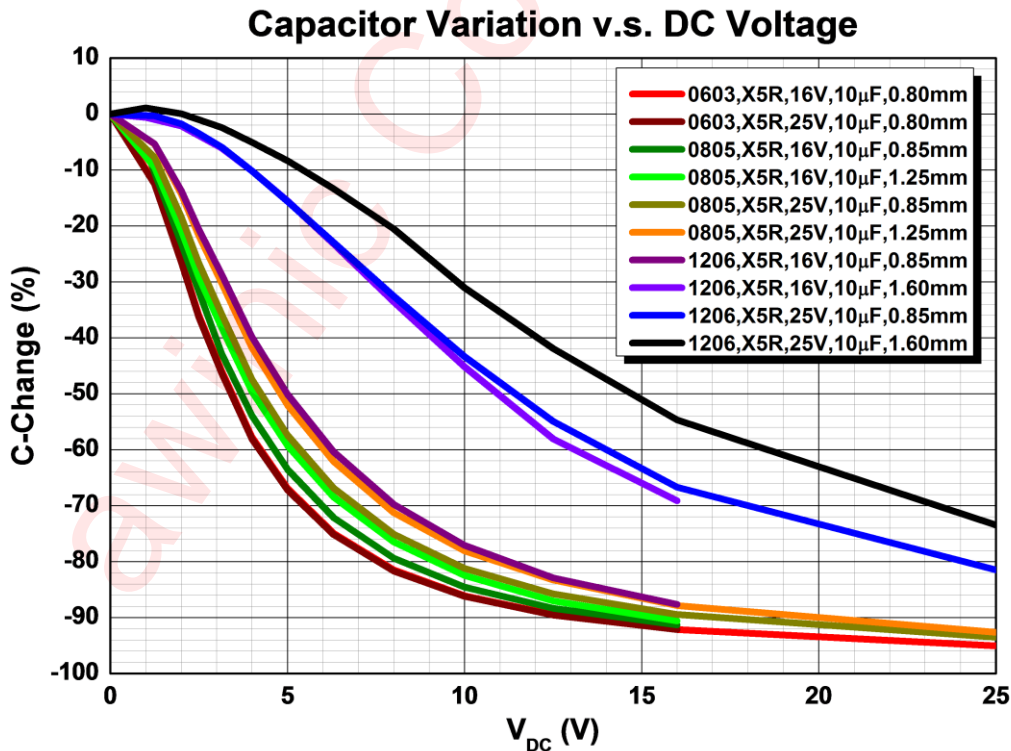


Figure 24 Different Types of Capacitive Voltage Stability

Among them, the space remaining value of different types of capacitors at $V_{DC} = 8.5V$ as shown below:

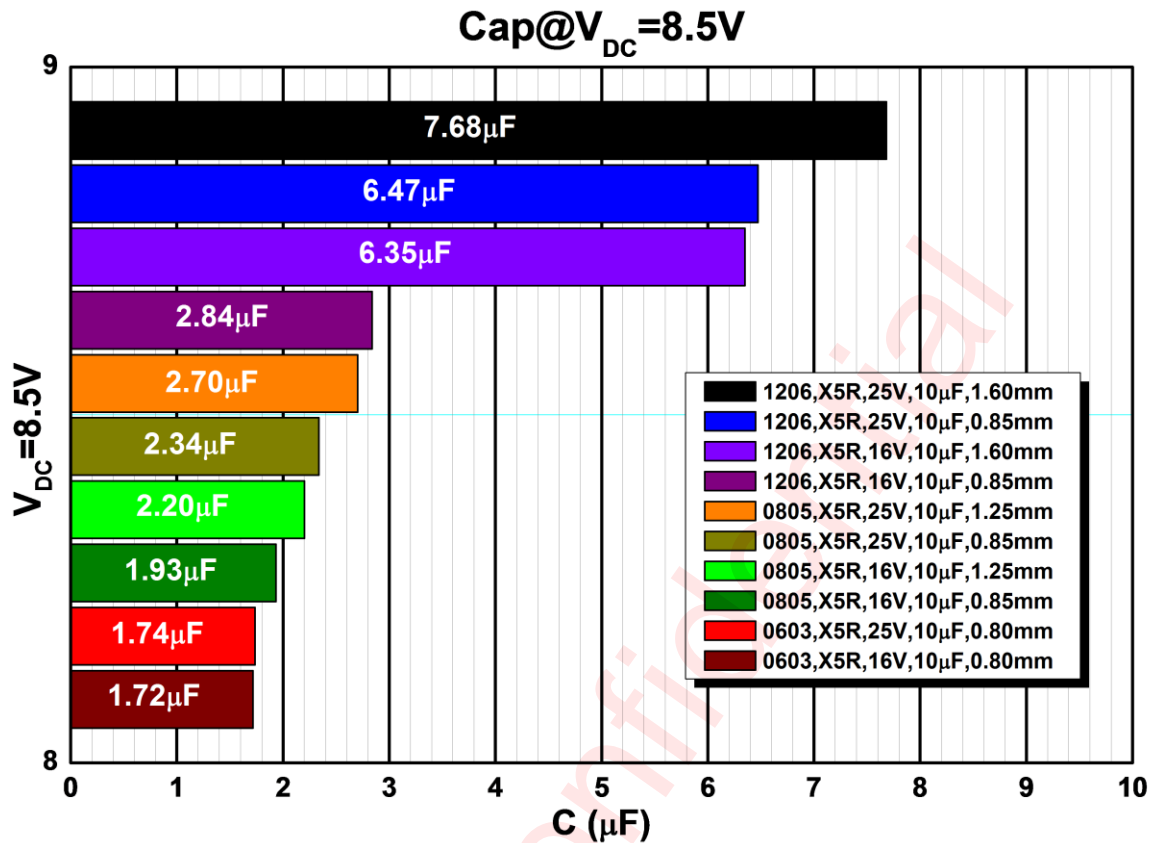


Figure 25 The Space Remaining Value of Different Types of Capacitors at $V_{DC} = 8.5V$

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. the higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW87359 typical applications, it is necessary to ensure the output value of the PVDD capacitor $\geq 3\mu F$ when $PVDD=8.5V$.

Input Capacitor- C_{in} (input high-pass cutoff frequency)

The input capacitors and input resistors form a high-pass filter to filter out the DC component of the input signal. The -3dB frequency points of the high pass filter is shown below:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} \text{ (Hz)}$$

The selection of a smaller C_{in} capacitor in the application helps to filter out 217Hz noise, which comes from the input coupling, and the smaller capacitor is advantageous to reduce the pop-click noise when the power amplifier turn on. Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. A capacitor value deviation of 10% or better capacitance is recommended.

Take typical application as an example, the input high-pass cutoff frequency is calculated as below:

$$f_{\text{H}}(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}} = \frac{1}{2 * \pi * 9\text{k}\Omega * 68\text{nF}} \text{ (Hz)} = 260\text{Hz}$$

Class D-type speaker & receiver 2-in-1 application (Gain=1), the input high pass frequency is as follows:

$$f_{\text{H}}(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}} = \frac{1}{2 * \pi * 48\text{k}\Omega * 100\text{nF}} \text{ (Hz)} = 34\text{Hz}$$

Class AB-type speaker & receiver 2-in-1 (Gain=1), the input high pass frequency is as follows:

$$f_{\text{H}}(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}} = \frac{1}{2 * \pi * 72\text{k}\Omega * 100\text{nF}} \text{ (Hz)} = 22\text{Hz}$$

Supply Decoupling Capacitor (C_S)

A good decoupling capacitor can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance, the ESR value of the capacitor should be as small as possible. In AW87359 applications, low ESR (equivalent-series-resistance) X7R or X5R ceramic capacitors are recommended. Generally, 10μF ceramic capacitors are used to bypass the VDD to the ground, and the decoupling capacitor should be placed as close to the VDD chip as possible in the layout. If you want to filter out low-frequency noise better, you need to add a 10μF or greater decoupling capacitor depending on your application. Meanwhile, a 33pF~0.1μF ceramic capacitor is placed on the pin of the power supply to filter the high frequency interference on the power supply. The capacitor should be placed as close as possible to the D4 pin and inductor.

Chargepump Flying capacitor (C_F)

The Flying capacitor is used to transfer energy between the power supply and the chargepump load, the value of the Flying capacitor directly affects the load regulation rate and the output drive capability of the chargepump. If flying capacitor is too small, it will affect the chargepump load adjustment rate and output drive capability, thereby affecting the power output of the amplifier, and the larger the Flying capacitor, the better the load regulation ability, driving ability is also stronger. Recommended use of 4.7μF, low ESR X7R, X5R ceramic capacitors, it is recommended to use more than 10V pressure capacitor.

Output capacitance of chargepump (C_{OUT})

The output capacitance of the chargepump and the ESR directly affect the ripple of the output, thus affecting the performance of the power amplifier. Recommended use of 10μF, low ESR X7R or X5R ceramic capacitors, you need to select the 25V voltage resistance capacitor.

Output beads, capacitors, TVS

Using EEE technology, in the class K mode, the AW87359 can also meet the FCC CLASS B specification requirements. It is recommended to Use ferrite chip beads and capacitors if device near the EMI sensitive circuits, there are long leads from amplifier to speaker, placed as close as possible to the output pin.

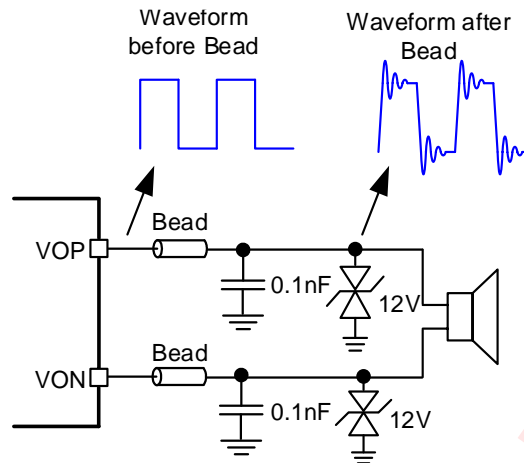


Figure 26 Ferrite Chip Bead and Capacitor

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

Power amplifier output PWM signals of high voltage to PVDD voltage, voltage to 8.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 12V TVS.

PCB AND DEVICE LAYOUT CONSIDERATION

EXTERNAL COMPONENTS PLACEMENT

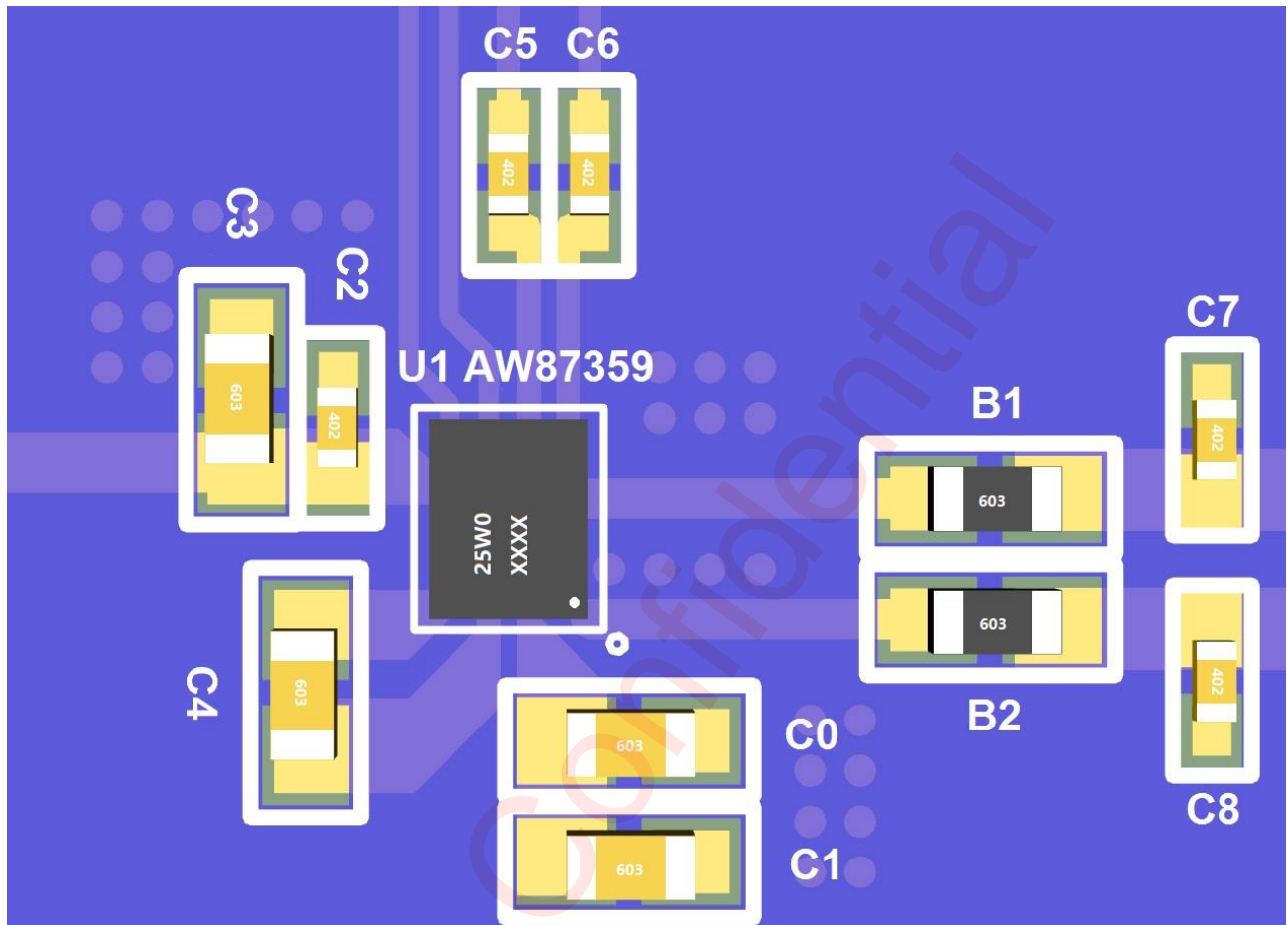


Figure 27 AW87359 External Components Placement

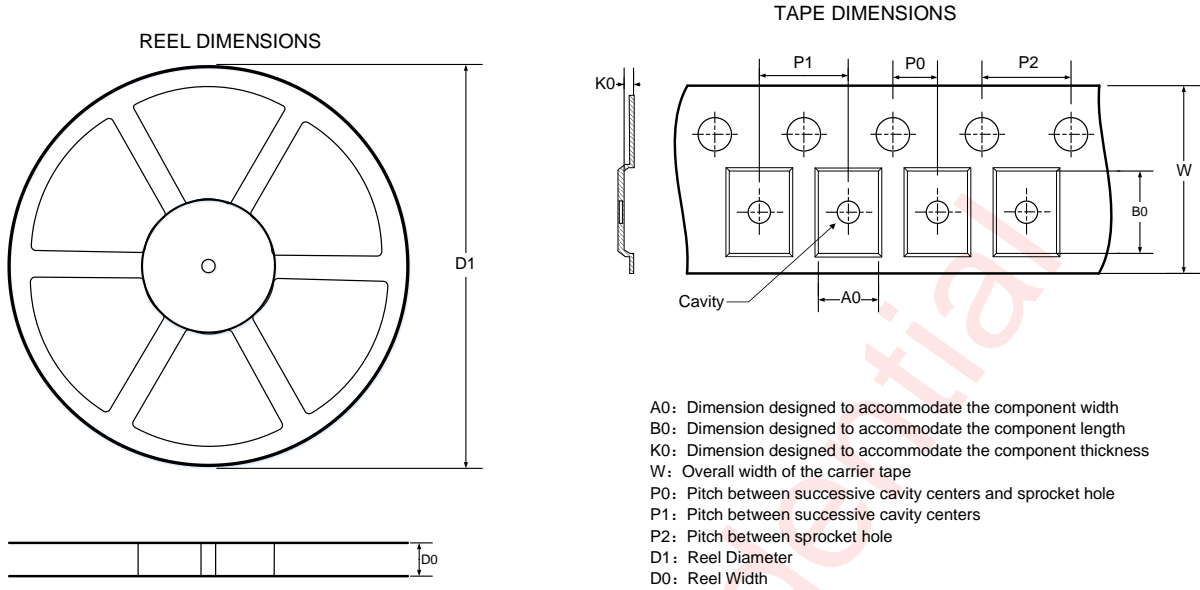
LAYOUT CONSIDERATIONS

This device is a power amplifier chip. To obtain the optimal performance, PCB layout should be considered carefully.

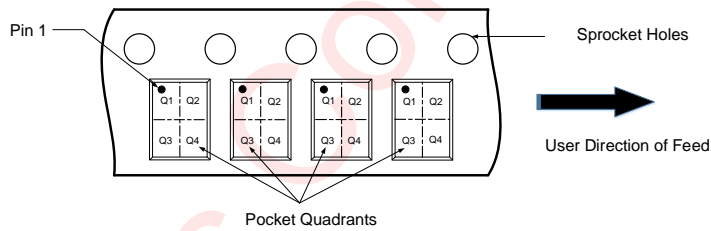
In order to obtain excellent performance of AW87359, PCB layout must be carefully considered. The design consideration should follow the following principles:

1. In AW87359 peripheral device layout, you first need to guarantee the chargepump output capacitance close to PVDD pin.
2. Try to provide a separate short and thick power line to AW87359, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin.
3. The input capacitors should be close to AW87359 INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87359 VON and VOP pin. The output line from AW87359 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

TAPE & REEL DESCRIPTION



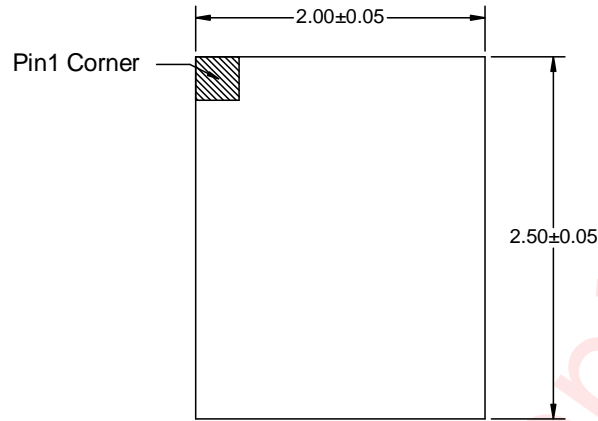
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	2.20	2.67	0.83	2.00	8.00	4.00	12.00	Q1

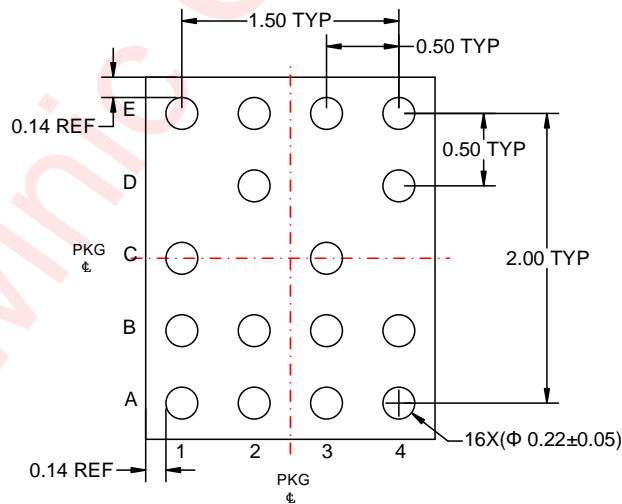
PACKAGE DESCRIPTION



Top View



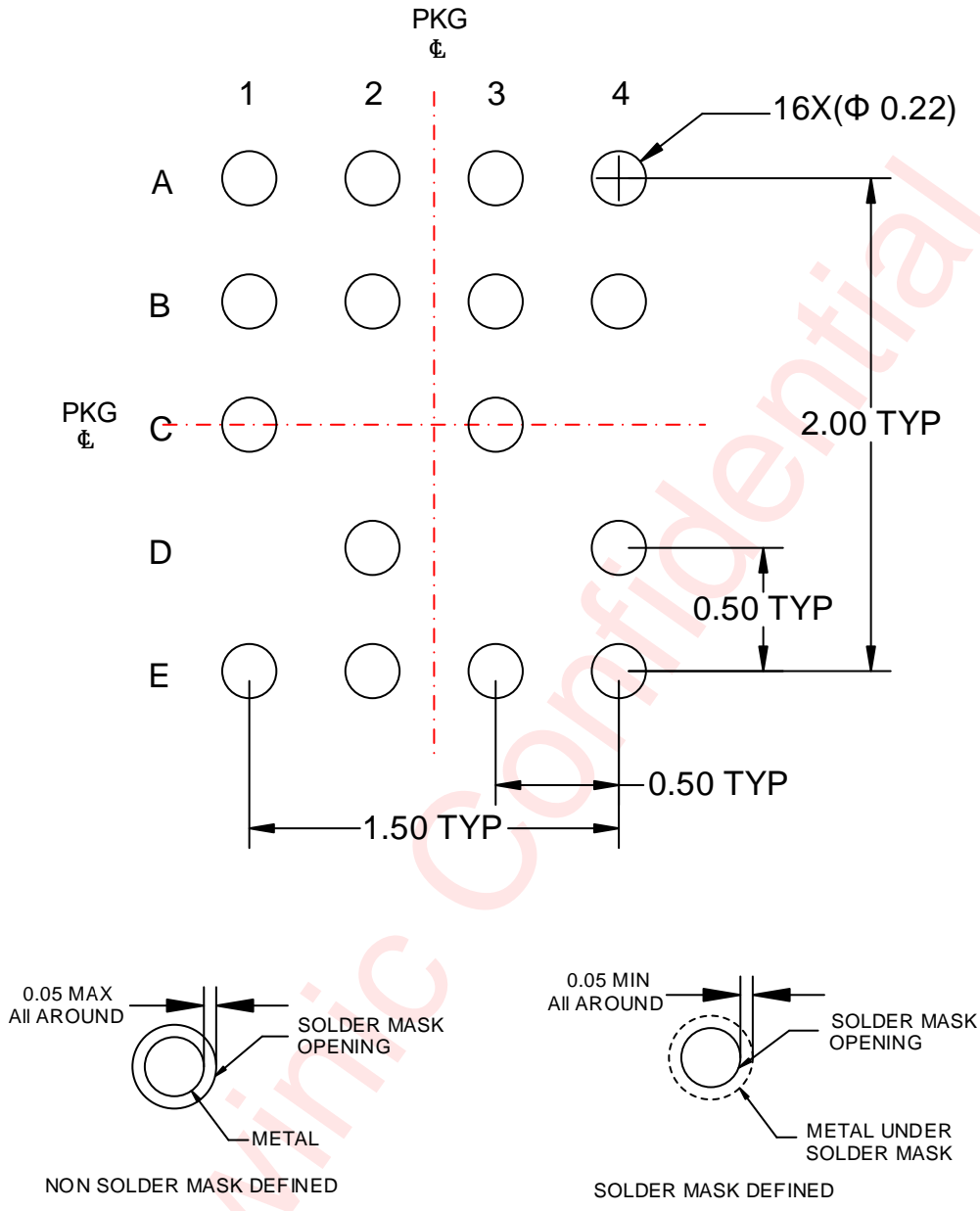
Side View



Bottom View

Unit: mm

LAND PATTERN



Unit: mm

VERSION INFORMATION

Version	Date	Description
V1.0	2019-05-01	AW87359FCR datasheet V1.0
V1.1	2019-12-15	Add test curve
V1.2	2020-05-27	Change test curve, Pin name
V1.3	2020-09-23	Change the name of the PCB device layout Modify package tolerance values Add description of register 0x08 at 00001001 when EN_SPK=1
V1.4	2020-12-10	Add test data of VDD vs Po
V1.5	2022-04-28	Update PIN CONFIGURATION AND TOP MARK

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