OZ3717 Data Sheet
Version 1.0

Revision History

Rev.	Date	Description
V1.0	11/20/2019	Initial Release

Contents

Digital Front End (DFE) IC for 10 to 17 Li-Ion Cells with High Side Drivers for N channel Power MOSFETs

FEATURES

- **Highly accurate Digital Front End (DFE) with High Side Driver**
  - Voltage, Current & Temperature + Control
- **14-bit Analog to Digital Converter (SAR ADC)**
  - High precision voltage measurement
  - Cell Voltage: 17 inputs, typical 5mV accuracy
  - Pack Current Sense
  - VPACK, VBAT, V5 and VMCU Voltage measurements
  - 3 External Temperature inputs with 2 selectable precision current sources
  - 1 Internal Temperature input
  - 1 Auxiliary; Direct ADC input
- **16-bit Analog to Digital Converter (ΣΔ ADC)**
  - High precision current measurement and Coulomb Counting (CC)
- **High Side MOSFET drivers (Chg/Dsg)**
  - Compatible with 15V to 75V battery packs
  - Hot-swap packs safely, soft start and charge management with Linear-Mode FET control
  - Strong drive ability
    - Rise time with 22nF capacitor load: 30µs
    - Fall time with 22nF capacitor load: 30µs
- **Protections**
  - **Over-Voltage Protection (optional)**
    - Over-Voltage (Vov) Threshold:
      - V_{OV} = 3.3 ~ 4.575 V, 5mV/step
    - Hysteresis voltage:
      - 0~630 mV, 10mV/step
  - **Discharge Current Protection (optional)**
    - Discharge-Over-Current 1 (DOC1):
      - V_{DOC1} = 5.0 ~ 163.75 mV, 0.625mV/step
    - Discharge-Over-Current 2 (DOC2):
      - V_{DOC2} = 10 ~ 160 mV, 10mV/step
    - Short-Circuit (SC):
      - $V_{SC} = N*V_{DOC2}$ (N = 2, 4, 6 or 8)
  - **Charge Current Protection**
    - Charge-Over-Current (COC):
      - V_{COC} = 2.8125 ~ 82 mV, 0.3125mV/step
  - **Internal Over-Temperature Protection:**
    - Die Temperature Measurement
- **Simultaneous Multi-Cell Balance**
- **Cell-Tap-Open (CTO) Detection**
- **SPI Serial Communications Bus Interface**
  - Interrupt output to external Host
- **Low Power Consumption**
  - Active mode: < 150uA (Without CC)
  - Standby mode: < 12uA
  - Shutdown mode: < 1uA
- **Green Package LQFP48**

APPLICATIONS

- ESS/UPS, Garden Tools, Power Tools
- e-Bikes, e-Scooters, Pedelec and Pedal-Assist Bicycles
- LEV(Light Electric Vechiles)

GENERAL DESCRIPTION

OZ3717 is a highly integrated, low cost, Digital Front End (DFE) IC for 10 to 17 serial cells in battery packs for high cell count and battery powered applications. OZ3717 integrates a 14-bit high precision Successive Approximation (SAR) Analog to Digital Converter (ADC) to detect cell voltages, temperature and charge/discharge current. For Coulomb-Counting measurements OZ3717 uses a 16-bit Sigma-Delta (ΣΔ) current ADC.

It integrates a simple, standalone safety engine that performs high accuracy and high reliability protections for safety events including OV, COC, DOC (DOC1 and DOC2), SC and optional UV; external Host (Microcontroller) could perform the release from those protection states.

OZ3717 integrates a charge-pump circuit to drive high-side N-channel charge and discharge MOSFETs with strong driving capability for fast response. It also provides a linear mode control for either charge FET or discharge FET to enable automatic balancing and hot swapping for multiple battery packs.

OZ3717 integrates internal Cell-Balance switches that can be controlled by a Microcontroller to perform Cell-Balancing. The maximum internal cell balance current is 10mA per cell. For higher cell balance current, an external cell balance circuit may be used.

OZ3717 uses measured ADC values compared with stored digital threshold values to detect DOC1 and COC. This enables high-accuracy current sense with the use of small current sense resistors (e.g. ≤1 mΩ) to reduce power dissipation and heat. OZ3717 uses one dedicated fast comparator for DOC2 detection and a second dedicated fast comparator for SC detection. Any DOC2/SC fault quickly activates the INT pin to alert the Microcontroller for safety event.

For maximum safety; OZ3717 has a Cell-Tap-Open (CTO) detection mode. The CTO operation is initiated by the Microcontroller and performed by OZ3717. The host can decide the CTO status based upon the cell voltage ADC data recorded during the CTO mode.

External host communicates with OZ3717 via SPI Bus w/Cyclic Redundancy Check for maximum safety.

OZ3717 integrates Internal Over-Temperature protection to prevent itself from over-heating during extreme conditions; for example, multi-cell balance.

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ3717TN-0	-40°C to 85°C	LQFP48L Lead-Free
OZ3717TN-1		

Note: *OZ3717TN-0 for 3.3V LDO, OZ3717TN-1 for 5V LDO.*

PIN DIAGRAM

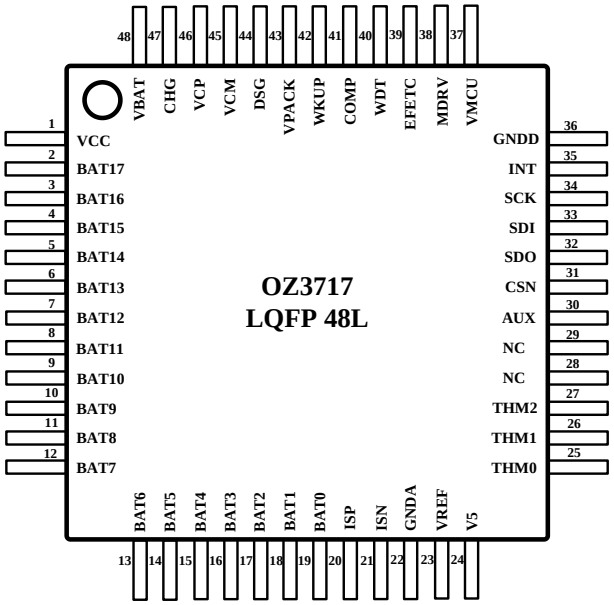


Figure 1: OZ3717 Pin diagram

SIMPLIFIED APPLICATION DIAGRAM

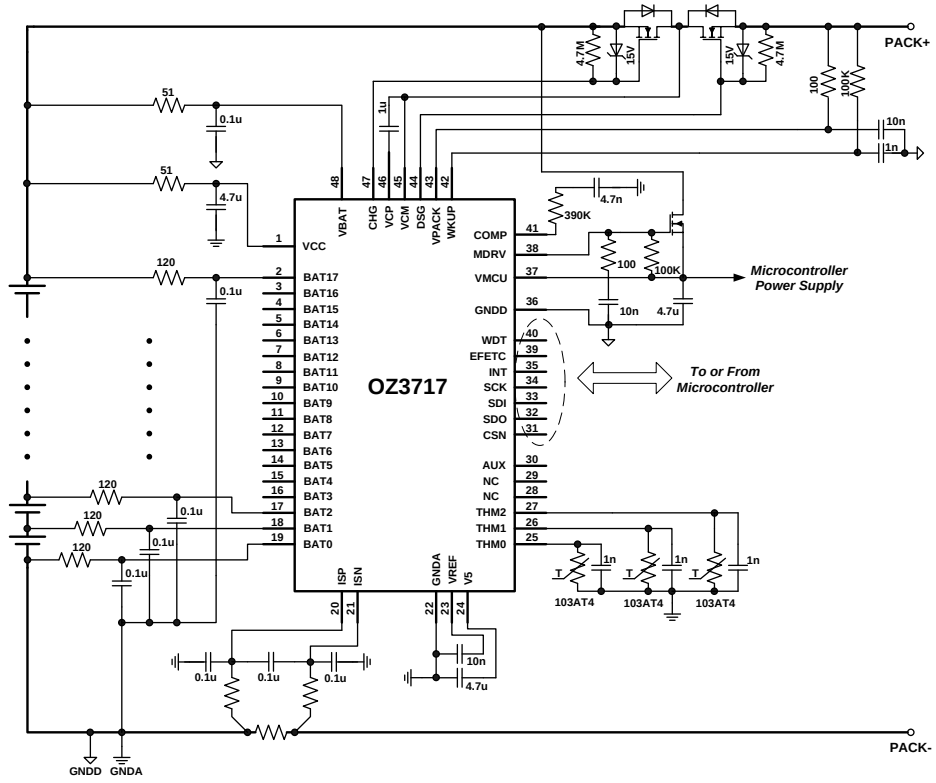


Figure 2: Simplified application diagram

SIMPLIFIED BLOCK DIAGRAM

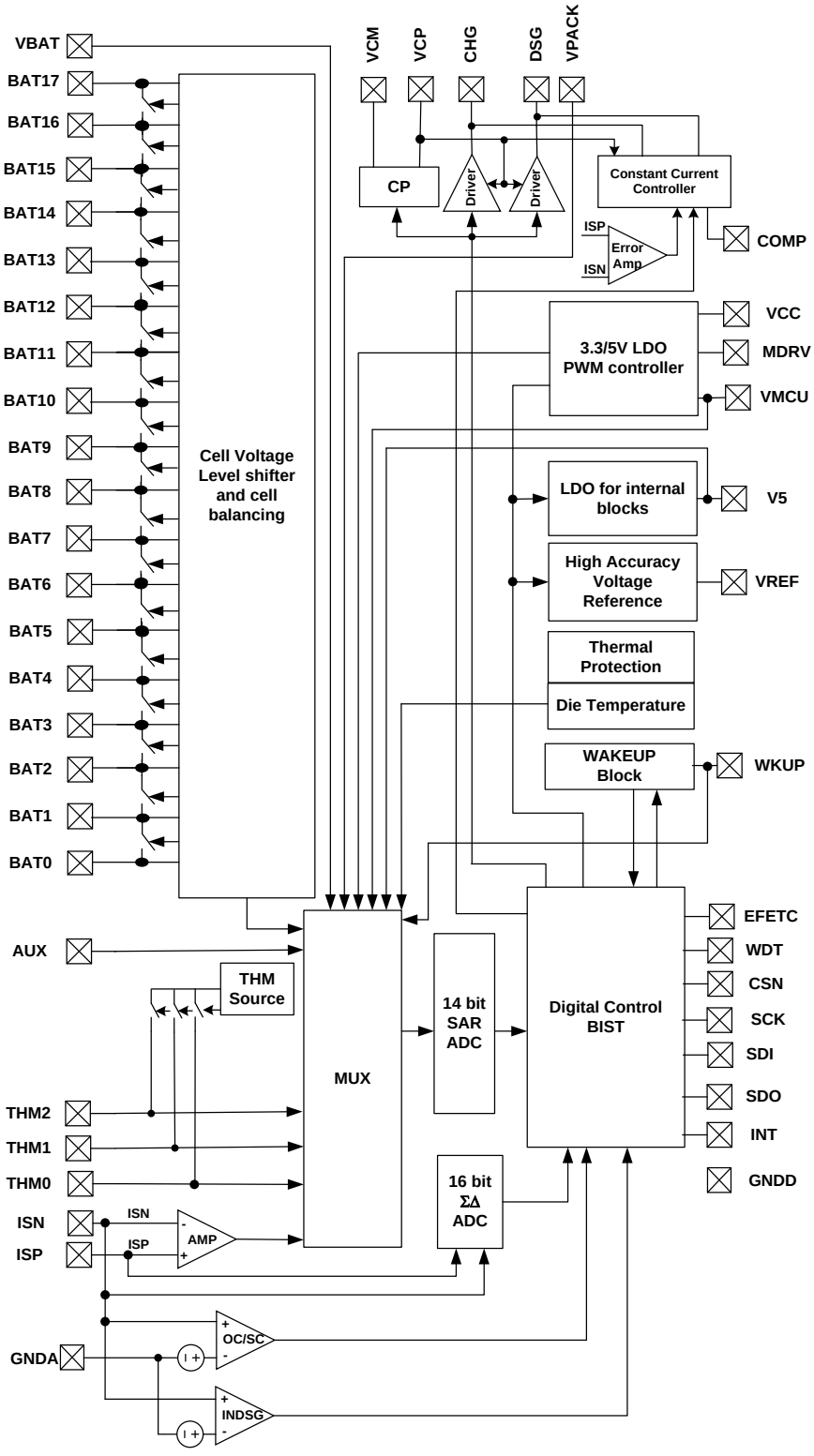


Figure 3: Block diagram

PIN DESCRIPTION

Table 1: Pin description

LQFP48 Pin No.	Pin Name	I/O	Type	Description
1	VCC	P	Power	Power supply of OZ3717
2	BAT17	I	Analog	Connect to Cell17 positive terminal
3	BAT16	I	Analog	Connect to Cell16 positive terminal and Cell17 negative terminal
4	BAT15	I	Analog	Connect to Cell15 positive terminal and Cell16 negative terminal
5	BAT14	I	Analog	Connect to Cell14 positive terminal and Cell15 negative terminal
6	BAT13	I	Analog	Connect to Cell13 positive terminal and Cell14 negative terminal
7	BAT12	I	Analog	Connect to Cell12 positive terminal and Cell13 negative terminal
8	BAT11	I	Analog	Connect to Cell11 positive terminal and Cell12 negative terminal
9	BAT10	I	Analog	Connect to Cell10 positive terminal and Cell11 negative terminal
10	BAT9	I	Analog	Connect to Cell9 positive terminal and Cell10 negative terminal
11	BAT8	I	Analog	Connect to Cell8 positive terminal and Cell9 negative terminal
12	BAT7	I	Analog	Connect to Cell7 positive terminal and Cell8 negative terminal
13	BAT6	I	Analog	Connect to Cell6 positive terminal and Cell7 negative terminal
14	BAT5	I	Analog	Connect to Cell5 positive terminal and Cell6 negative terminal
15	BAT4	I	Analog	Connect to Cell4 positive terminal and Cell5 negative terminal
16	BAT3	I	Analog	Connect to Cell3 positive terminal and Cell4 negative terminal
17	BAT2	I	Analog	Connect to Cell2 positive terminal and Cell3 negative terminal
18	BAT1	I	Analog	Connect to Cell1 positive terminal and Cell2 negative terminal
19	BAT0	I	Analog	Connect to Cell1 negative terminal
20	ISP	I	Analog	Current sense positive input
21	ISN	I	Analog	Current sense negative input
22	GNDA	P	Power	Analog ground
23	VREF	O	Analog	2.5V reference output. Connect external 10 nF capacitor to ensure stability and to reduce noise.
24	V5	P	P	5V LDO output. Only for OZ3717 internal use.
25	THM0	I	Analog	External temperature detection input 1
26	THM1	I	Analog	External temperature detection input 2
27	THM2	-	Analog	External temperature detection input 3
28	NC	-	Analog	Not connected
29	NC	-	Analog	Not connected
30	AUX	I	Analog	External general analog signal input (Direct ADC input)
31	CSN	I	Digital	SPI Bus Chip Select. Low active.
32	SDO	O	Digital	SPI Bus Serial data output
33	SDI	I	Digital	SPI Bus Serial data input
34	SCK	I	Digital	SPI Bus Serial data clock
35	INT	O	Digital	Interrupt signal to external host. Low-level trigger or falling edge trigger (100Hz)
36	GNDD	P	Power	Digital ground
37	VMCU	P	Power	5V or 3.3V (optional) LDO output and external power supply voltage sense. Only for external devices use.
38	MDRV	O	Analog	External MOSFET gate control signal for external low voltage power supply
39	EFETC	I	Digital	External MOSFET control input to enable Charge/Discharge MOSFET by Microcontroller
40	WDT	O	Digital	Microcontroller reset output (64ms) caused by OZ3717 internal Watch-Dog-Timer (WDT) overflow
41	COMP	O	Analog	Compensation terminal for Pre-discharge current control block

LQFN48 Pin No.	Pin Name	I/O	Type	Description
42	WKUP	I	Analog	Wakeup signal input —transition from Shutdown Mode to Active Mode
43	VPACK	I	Analog	PACK voltage sense
44	DSG	O	Analog	Discharge MOSFET control
45	VCM	I	Analog	Internal Charge Pump (CP); energy input for external CP storage capacitor
46	VCP	I	Analog	CP voltage feedback for internal charge pump
47	CHG	O	Analog	Charge MOSFET control
48	VBAT	I	Analog	Top of Cell Stack. Battery voltage sense

TYPICAL APPLICATION SCHEMATICS

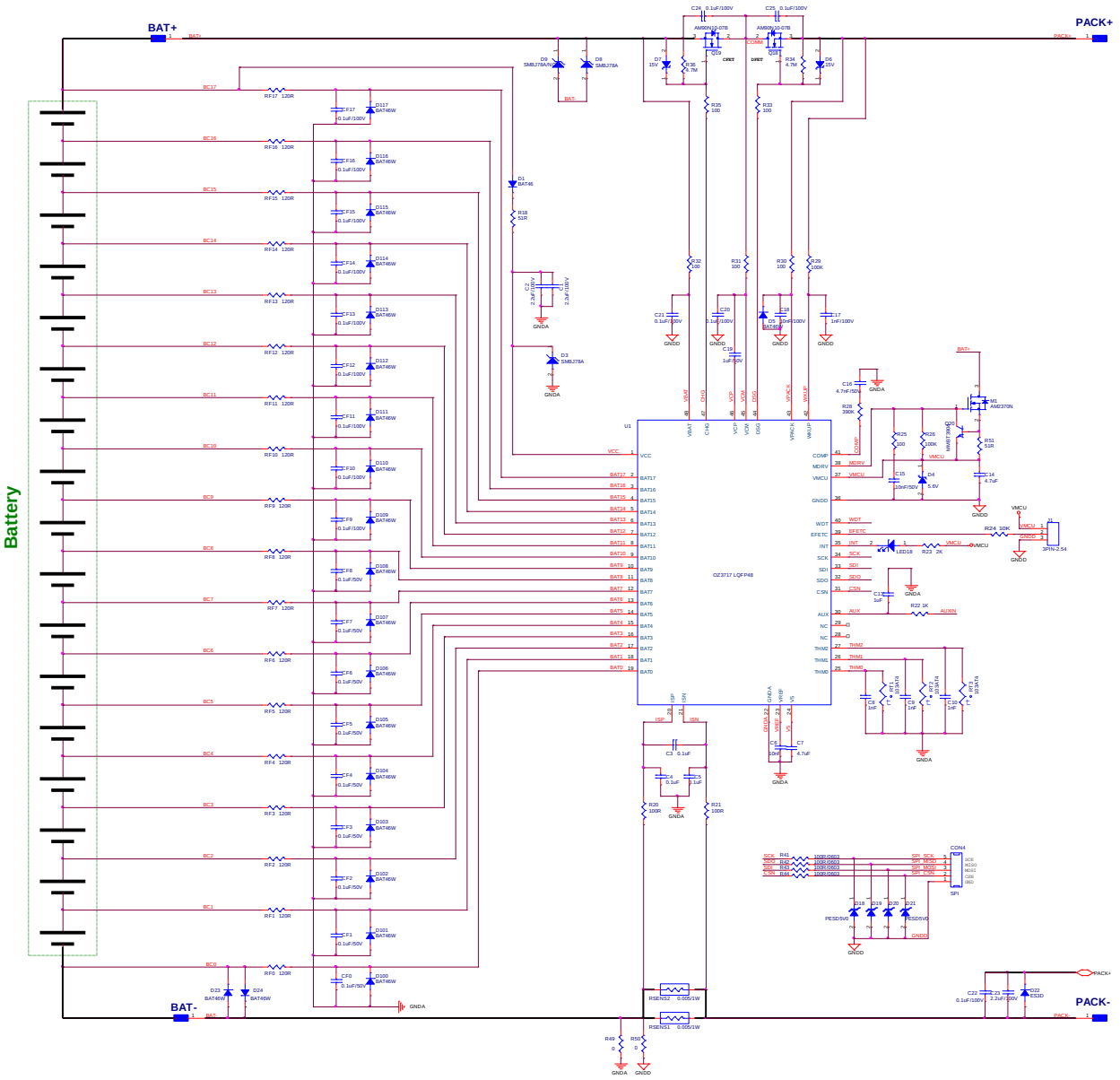


Figure 4: Typical application schematic for 2-terminal and 17 cells battery pack

***Note 1**: BAT46 type or other low forward diode are recommended for D100 – D117,howerver,If the negative terminal of the battery can be first connected to BAT- during power up (cells connecting to protection PCB), these diodes can be removed.*

***Note 2**: Please refer to APPENDIX A for the recommended value of each external component.*

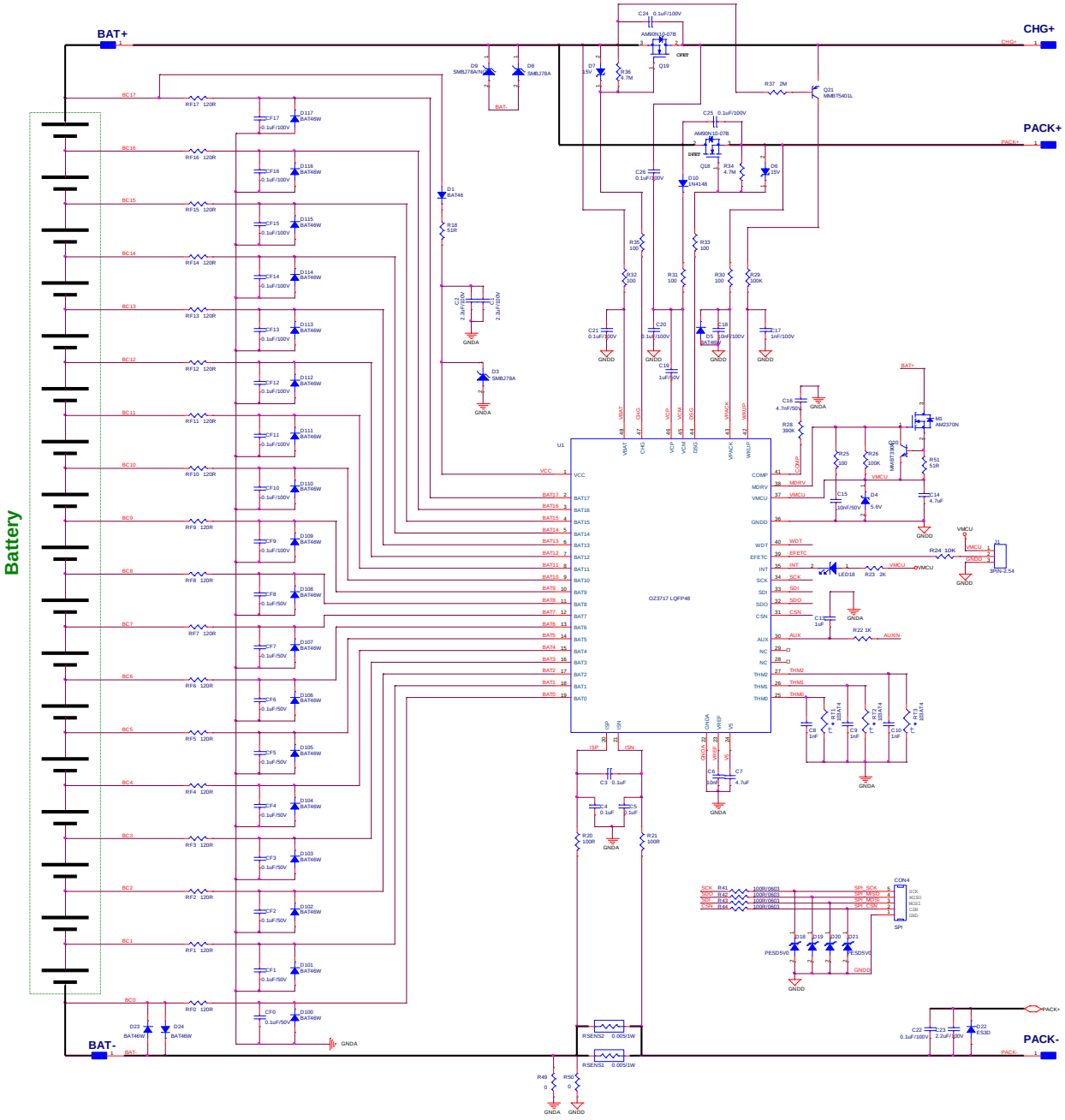


Figure 5: Typical application schematic for 3-terminal and 17 cells battery pack

Note 1*: BAT46 type or other low forward diode are recommended for D100 – D117,howerver,If the negative terminal of the battery can be first connected to BAT- during power up (cells connecting to protection PCB), these diodes can be removed.*

Note 2*: Please refer to APPENDIX A for the recommended value of each external component.*

ABSOLUTE MAXIMUM RATING

VCC, VBAT, VPACK, WKUP to GNDA, GNDD	-0.3 to +100 V
BATn to BATn-1 (where n is 2 to 17)	-100 to +100 V
BAT1 to BAT0	-0.3 to +100 V
BATn to GNDA (where n is 1 to 17)	-0.3 to +100 V
BAT0 to GNDA	-0.3 to +0.3 V
ISP, ISN, VREF, V5, THM0~THM2, AUX and COMP to GNDA	-0.3 to +6.5 V
CHG, DSG, VCP and VCM to GNDD	-0.3 to +110 V
MDRV	-0.3 to +12 V
VMCU, CSN, SDI, SDO, SCK, INT, EFETC and WDT to GNDD	-0.3 to +6.5 V
Maximum Operating Junction temperature	+125°C
Storage temperature range	-55°C to +150°C
ESD rating (HBM)	1.5 kV
ESD rating (CDM)	1.0 kV
ESD rating (MM)	250 V

NOTE: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

RECOMMENDED OPERATING RANGE

VCC, VBAT to GNDA, GNDD	8 to 80 V
VPACK to GNDA, GNDD	0 to 80 V
BATn to BATn-1 (where n is 2 to 17)	0.7 to 4.35 V
BAT1 to BAT0	0.7 to 4.35 V
BAT0 to GNDA	-0.3 to +0.3 V
THM0~THM2 and AUX to GNDA	0 to 2.5 V
ISN to ISP	-250 to 250 mV
WKUP to GNDD	0 to 80 V
MDRV	0 to 10 V
CSN, SDI, SDO, SCK, INT, EFETC and WDT to GNDD	0 to 5.5 V
Operating temperature range (ambient)	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

Table 2: Electrical Specifications. Unless otherwise specified: T_A = -40 to 85 ℃, VCC = 71.4 V, all cell voltages = 4.2 V

Symbol	Parameter	Test Conditions		Limits			Units
				Min.	Typ.	Max.	
Power Supply, LDO							
V_{P-ON}	Chip power-on voltage	VCC voltage goes up slowly		5.5	6.5	7.5	V
V_{P-DOWN}	Chip power-down voltage	VCC voltage goes down slowly		4.5	5.6	6.5	V
$I_{VCC-ACT}$	Supply current – Active	Auto-8 scan, ΣΔ ADC on, ***sw_vref_enable***="1"			240		µA
		Auto-8 scan, ΣΔ ADC off, ***sw_vref_enable***="1"			120		µA
		Auto-scan and ΣΔ ADC are both off, ***sw_vref_enable***="1"			85		µA
		Auto-scan and ΣΔ ADC are both off, ***sw_vref_enable***="0"		15	25	30	µA
$I_{VCC-STBY}$	Supply current – Standby	VCC = 10V to 75V		6	12	20	µA
I_{VCC-SD}	Supply current - Shutdown	VCC = 10V to 75V		0.5	1	2	µA
V_{5V}	V5 output voltage	I_{LOAD} < 200uA		4.95	5.0	5.05	V
V_{MCU}	VMCU output voltage	I_{LOAD} < 2mA, 3.3V output		3.35	3.4	3.45	V
		I_{LOAD} < 2mA, 5V output		5.1	5.2	5.3	V
Measurement (***Note 1***)							
V_{E-CELL}	Total measurement error of cell voltage channels	-40 to 85 °C	V_{CELL} = 1.50V	-20		20	mV
			V_{CELL} = 3.00V	-20		20	mV
			V_{CELL} = 4.50V	-25		25	mV
		-20 to 60 °C	V_{CELL} = 1.50V	-15		15	mV
			V_{CELL} = 3.00V	-15		15	mV
			V_{CELL} = 4.50V	-20		20	mV
$V_{E-CUR-SD}$	Total measurement error of current channel (ΣΔ ADC)	-40 to 85 °C	V_{ISN}-V_{ISP} = 0mV	-0.15		0.15	mV
		T_A = 23 °C		-0.075		0.075	mV
$V_{GE-CUR-SD}$	Gain error of current channels (ΣΔ ADC)	-250mV ≤ V_{ISN}-V_{ISP} ≤ 250mV		-1.00%		1.00%	
$V_{E-CUR-SAR}$	Total measurement error of current channel (SAR ADC)	-40 to 85 °C	V_{ISN}-V_{ISP} = 0mV	-0.3		0.3	mV
			-10mV ≤ V_{ISN}-V_{ISP} ≤ 10mV	-0.5		0.5	mV
			80mV ≤ V_{ISN}-V_{ISP} ≤ 160mV	-5		5	mV
		-20 to 60 °C	V_{ISN}-V_{ISP} = 0mV	-0.3		0.3	mV
			-10mV ≤ V_{ISN}-V_{ISP} ≤ 10mV	-0.5		0.5	mV
			80mV ≤ V_{ISN}-V_{ISP} ≤ 160mV	-3.5		3.5	mV
$V_{GE-CUR-SAR}$	Gain error of current channels (SAR ADC)	-40 to 85 °C 0 to 85 °C	-60mV ≤ V_{ISN}-V_{ISP} ≤ 80mV	-0.7%		0.7%	
$V_{E-TS-SAR}$	Total measurement error of temperature channel	V_{TS} = 250mV		-3		3	mV
		V_{TS} = 2500mV		-15		15	mV
V_{E-PACK}, V_{E-BAT}	Total measurement error of VPACK and VBAT channels	17V < V_{VPACK}, V_{VBAT} < 75V		-0.85		0.85	V
COC, DOC1, DOC2 and SC Protection (***Note 2***)							
V_{E-DOC2}	DOC2 protection threshold error	Set V_{DOC2} to 10mV		-3.5		3.5	mV
		Set V_{DOC2} to 150mV		-16		16	mV
T_{E-DOC2}	DOC2 protection delay time error	Set V_{DOC2} to 60mV and T_{DOC2} to 50ms (***Note 3***)		-5		5	ms
V_{E-SC}	SC protection threshold error	Set V_{DOC2} To 10mV, V_{SC} set to 2*V_{DOC2}		-12		12	mV
		Set V_{DOC2} To 150mV , V_{SC} set to 2*V_{DOC2}		-18		18	mV
T_{E-SC}	SC protection delay time error	Set V_{DOC2} to 10mV and T_{SC} to 62.5µs (***Note 3***)		-6.25		6.25	µs
V_{E-DOC1}	DOC1 protection threshold error			***Note 4***			mV
$T_{E-DOCR/SCR}$	DOC1, DOC2 and SC release time error	Set $T_{DOCR/SCR}$ to 30s (***Note 3***)		-10%* $T_{DOCR/SCR}$		10%* $T_{DOCR/SCR}$	-
V_{E-COC}	COC protection threshold error			***Note 4***			mV
T_{E-COCR}	COC release time error	Set T_{COCR} to 2s (***Note 3***)		-10%* T_{COCR}		10%* T_{COCR}	
OV Protection (***Note 2***)							
T_{DET}	Safety event check period (only for the events based on ADC data)	Work in Active mode, no trigger-scan			0.25		s
V_{E-OV}	OV protection threshold error			***Note 5***			mV
V_{E-OVR}	OV release threshold error			***Note 5***			mV
$V_{DSG-TH2}$	Discharge-state threshold 2			3	5	8	mV

ELECTRICAL SPECIFICATIONS (Continued)

Table 3: Electrical Characteristics. Unless otherwise specified: T_A = -40 to 85℃, VCC = 71.4 V, All cell voltages = 4.2 V

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Charge-state and Discharge-state determination						
$V_{E\text{-}CHG\text{-}TH}$	Charge-state threshold error			***Note 4***		mV
$V_{E\text{-}DSG\text{-}TH1}$	Discharge-state threshold 1 error			***Note 4***		mV
Wakeup detection, Load-on/off detection, Charger-in/out detection						
V_{WKUP}	Threshold for the WKUP pin HIGH/LOW determination	Add voltage lower than 0.6V to the WKUP pin and then increase it slowly	1.2	1.35	1.5	V
R_{WKUP}	Equivalent resistance on the WKUP pin in Shutdown mode	Add 0.8V on the WKUP pin		34		kΩ
V_{LO}	Threshold for the load-on or load-off determination, measure V_{VBAT}-V_{VPACK}	Discharge FET off, increase the load on battery pack gradually	0.8	1.25	1.6	V
V_{CHGIN}	Threshold for the charger-in or charger-out determination; measure V_{WKUP}-V_{VBAT}	Charge FET off, increase the charger voltage on battery pack gradually	0.20	0.75	1.3	V
FET driver						
V_{DSGH}	DSG output voltage when ON; measure V_{DSG}-V_{VCM}	DC load between DSG and VPACK ≥ 2M	11.4	12.1	12.8	V
V_{DSGL}	DSG output voltage when OFF; measure V_{DSG}-V_{VPACK}	No power source between DSG and VPACK	0	0.5	0.8	V
V_{CHGH}	CHG output voltage when ON; measure V_{CHG}-V_{VCM}	DC load between CHG and VBAT ≥ 2M	11.4	12.1	12.8	V
V_{CHGL}	CHG output voltage when OFF; measure V_{CHG}-V_{VBAT}	No power source between CHG and VBAT	0	0.5	0.8	V
$T_{DSG\text{-}R}$	DSG rise time when ON (***Note 6***)	22nF between DSG and PACK+, T_A = 25°C		30		µs
$T_{DSG\text{-}F}$	DSG fall time when OFF (***Note 6***)			30		µs
$T_{CHG\text{-}R}$	CHG rise time when ON (***Note 6***)	22nF between CHG and BAT+, T_A = 25°C		30		µs
$T_{CHG\text{-}F}$	CHG fall time when OFF (***Note 6***)			30		µs
$T_{CP\text{-}OK}$	Charge pump start-up time	470nF between VCM and VCP		10		ms
Digital Inputs and Outputs						
V_{IL}	Logic input LOW level		-	-	0.6V	V
V_{IH}	Logic input HIGH level		V_{VMCU} -0.6V	-	-	V
V_{OL}	Logic output LOW level	I_{LOAD} = 1mA			0.3V	V
V_{OH}	Logic output HIGH level	I_{LOAD} = -1mA	V_{VMCU} -0.3V			V
Cell Balance						
$R_{ON\text{-}B}$	Cell balance FET $R_{DS(ON)}$	V_{CELL} = 4.2 V, R_F = 51 Ω; Balance cell n (where n = 1 to 17)	-	400	-	Ω
T_{CB}	Cell balance timer		-	30	-	s
Internal Over Temperature Protection						
t_{CBOT}	Cell-Balance over temperature protection threshold	Balance cell n (where n = 1 to 17)		125*		
$t_{CBOT\text{-}H}$	Cell-Balance over temperature release hysteresis			25*		
t_{TSP}	Thermal Standby threshold			150*		
$t_{TSP\text{-}H}$	Thermal Standby release hysteresis			25*		
Miscellaneous						
I_{TS}	Current source for temperature measurement	Measure the current output from the TS pin during temperature measurement	19	20	21	µA
			115	120	125	µA
$I_{BAT\text{-}S}$	BATn sink current (where n = 3 to 17)	When trigger cell-n ADC, Vcell-n=4V (n=1,2,… 17)		25.6	30.8*	µA
	BATn sink current (where n = 2)			3.2	3.9*	µA
	BATn sink current (where n = 1)			9.8	11.8*	µA
$I_{BAT\text{-}L}$	BATn leakage current (where n = 1 to 17)	No ADC and cell balance on cell n	-0.2	0	0.2	µA
f_{OSC64K}	Internal 64kHz oscillator (for Coulomb Counting) frequency		57.5	64	70	kHz

** Guaranteed by design.*

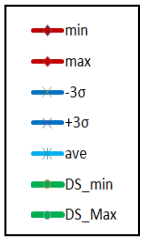
Note 1: *The specifications related to SAR ADC measurement values, above table, are based on the high accuracy mode (8 consecutive ADC conversions averaged for the final ADC value, please refer to the section FUNCTIONAL DESCRIPTION for detail).*

Note 2: *OV (T_{OV}), COC (T_{COC}), DOC1 (T_{DOC1}) protection delay setting's measurement unit is 'scan-cycle'; not second. The scan-cycle means one complete Auto-scan or Trigger-scan cycle. If the protection delay setting is set to N, only when a certain safety event is continuously detected for N scan-cycles, it is confirmed to have occurred.*
Note 3: *OZ3717 uses digital timer. The accuracy of all time values is determined by the internal oscillator's frequency error which could have about +/-10% variation of its standard value.*
Note 4: *OZ3717 compares the current channel ADC data with the threshold settings in Registers to determine whether the thresholds are reached. So these error ranges are determined by the current channel ADC accuracy (please refer to $V_{E-CUR-SAR}$).*
Note 5: *OZ3717 compares the cell voltage channel ADC data with the threshold settings in Registers to determine whether the thresholds are reached. So these ranges are determined by the cell voltage channel ADC accuracy (please refer to V_{E-CELL}).*
Note 6: *The time is measured between 2V – 8V of the rising or falling edge.*

TYPICAL OPERATING CHARACTERISTICS

Key:

- min = measured minimum
- max = measured maximum
- - 3σ = - 3 Sigma Statistical Limits
- +3σ = +3 Sigma Statistical Limits
- ave = arithmetic average (mean)
- DS_min = Data Sheet min limit
- DS_max = Data Sheet max limit



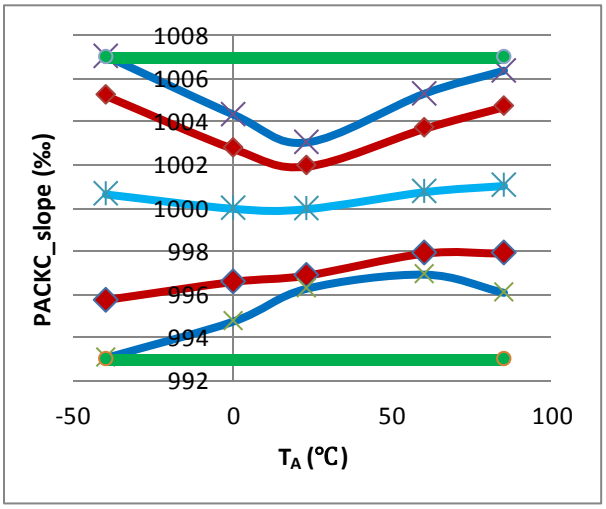


Figure 6: Current Channel - SAR ADC Slope (-60mV ≤ V_{ISN}-V_{ISP} ≤ 80mV) vs. Temperature (-40~85°C)

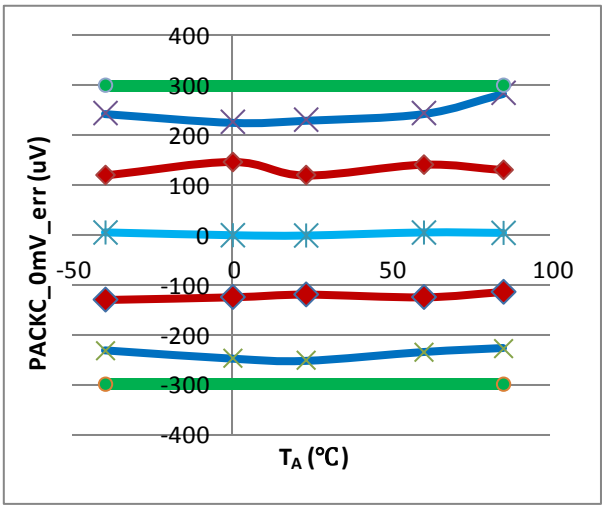


Figure 7: Current Channel - SAR ADC Error (V_{ISN}-V_{ISP} = 0mV) vs. Temperature (-40~85°C)

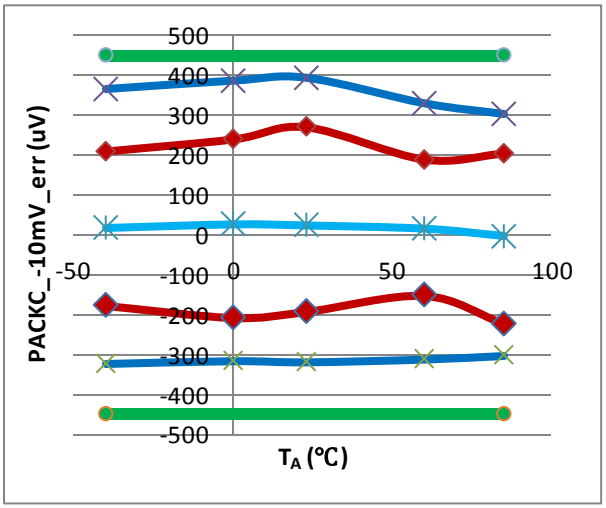


Figure 8: Current Channel - SAR ADC Error (V_{ISN}-V_{ISP} = -10mV) vs. Temperature (-40~85°C)

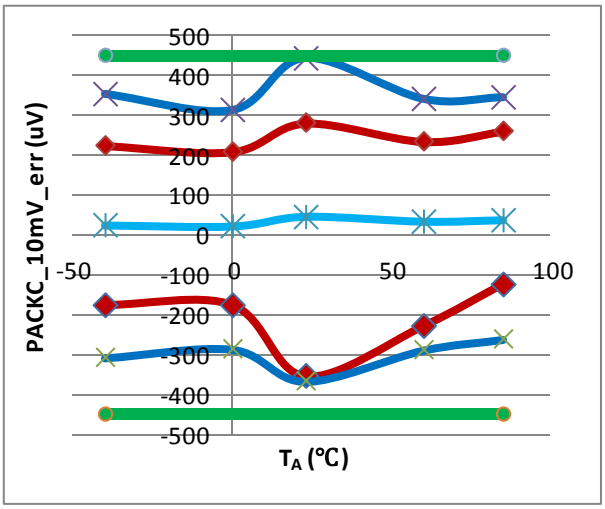


Figure 9: Current Channel - SAR ADC Error (V_{ISN}-V_{ISP} = 10mV) vs. Temperature (-40~85°C)

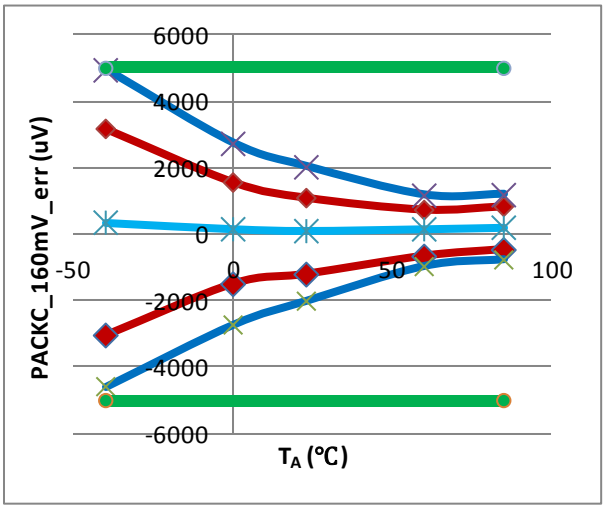


Figure 10: Current Channel - SAR ADC Error (V_{ISN}-V_{ISP} = 160mV) vs. Temperature (-40~85°C)

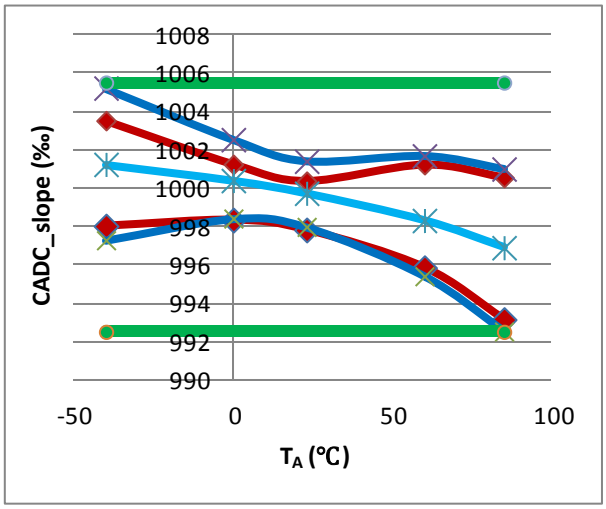


Figure 11: Current Channel - ΣΔ ADC Slope (-250mV ≤ V_{ISN}-V_{ISP} ≤ 250mV) vs. Temperature (-40~85°C)

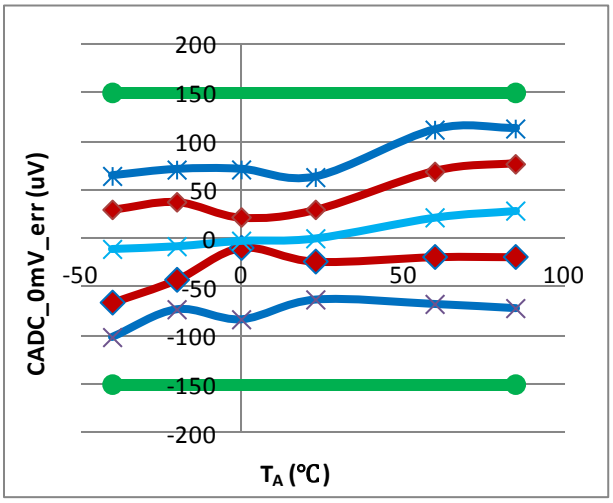


Figure 12: Current Channel - ΣΔ ADC Error (V_{ISN}-V_{ISP} = 0mV) vs. Temperature (-40~85°C)

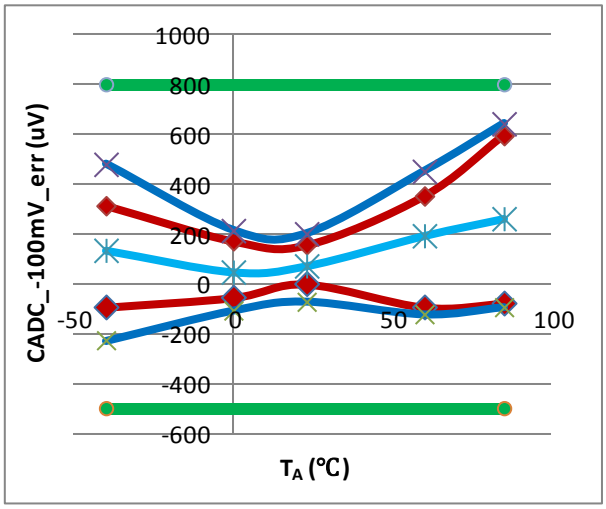


Figure 13: Current Channel - ΣΔ ADC Error (V_{ISN}-V_{ISP} = -100mV) vs. Temperature (-40~85°C)

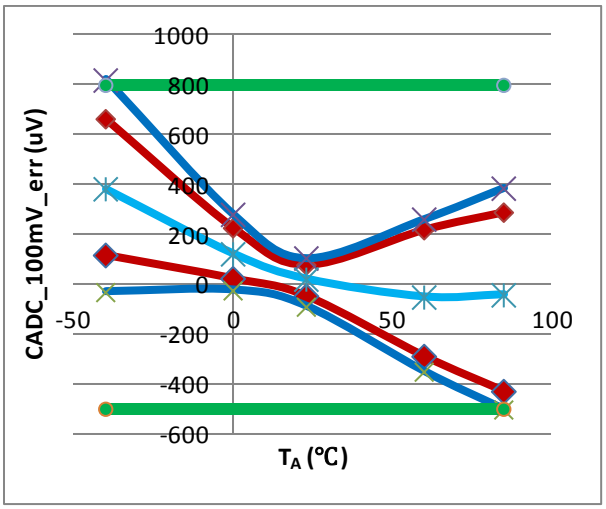


Figure 14: Current Channel - ΣΔ ADC Error (VISN-VISP = 100mV) vs. Temperature (-40~85°C)

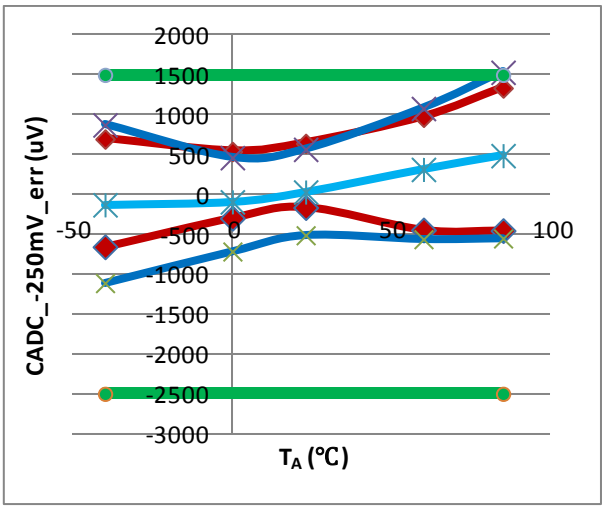


Figure 15: Current Channel - ΣΔ ADC Error (VISN-VISP = -250mV) vs. Temperature (-40~85°C)

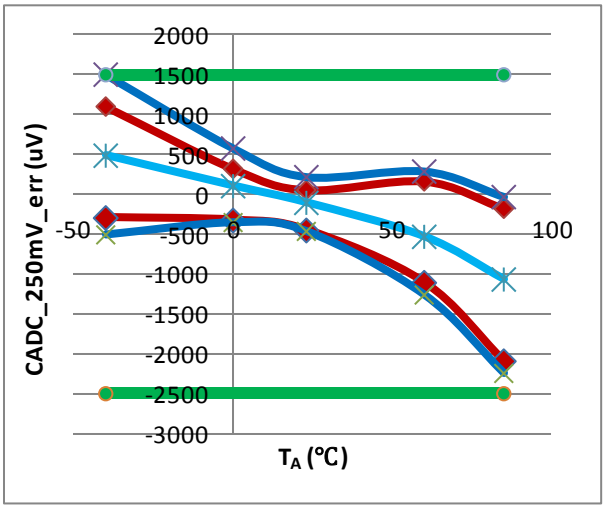


Figure 16: Current Channel - ΣΔ ADC Error (VISN-VISP = 250mV) vs. Temperature (-40~85°C)

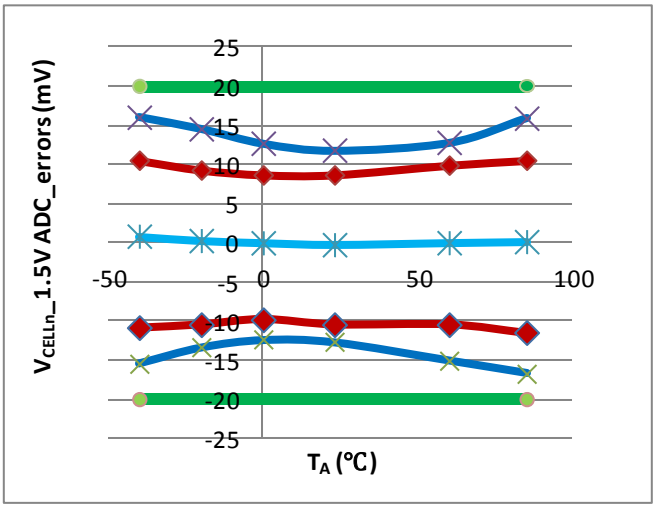


Figure 17: Cell Voltage Channel Error (V_{CELLn} = 1.5V, n = 1, 2, …, 17) vs. Temperature (-40~85°C)

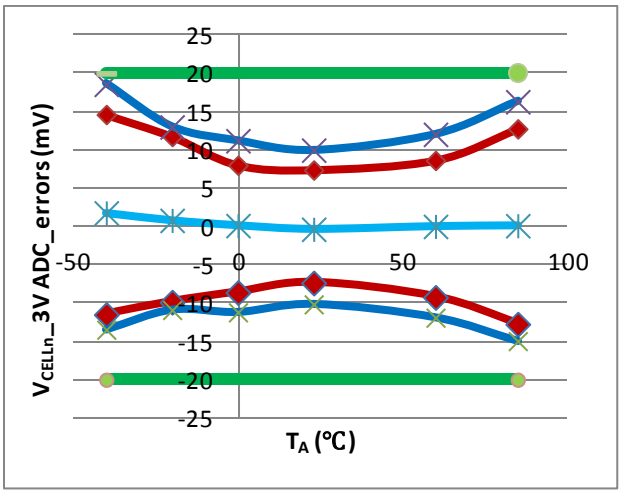


Figure 18: Cell Voltage Channel Error (V_{CELLn} = 3V, n = 1, 2, …, 17) vs. Temperature (-40~85°C)

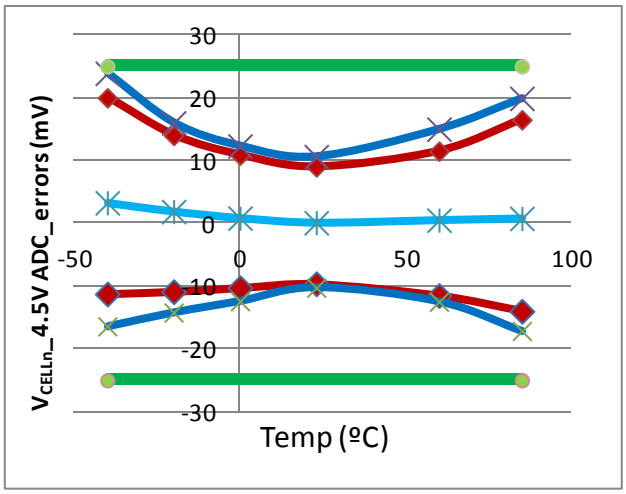


Figure 19: Cell Voltage Channel Error (V_{CELLn} = 4.5V, n = 1, 2, …, 17) vs. Temperature (-40~85°C)

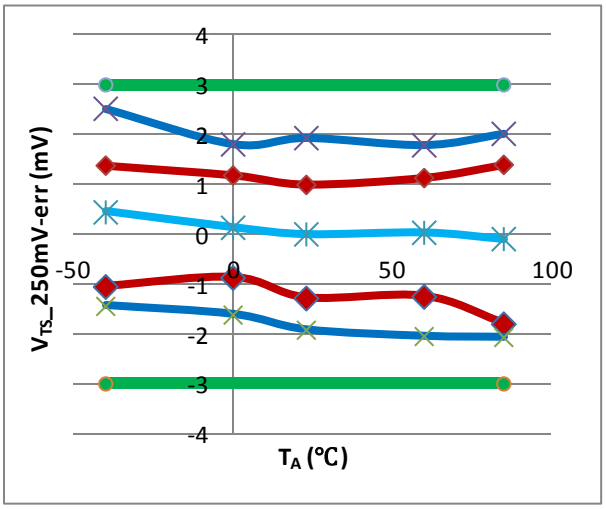


Figure 20: THM-n (n=0,1, 2) Channel Error (V_{THM} = 250mV) vs. Temperature (-40~85°C)

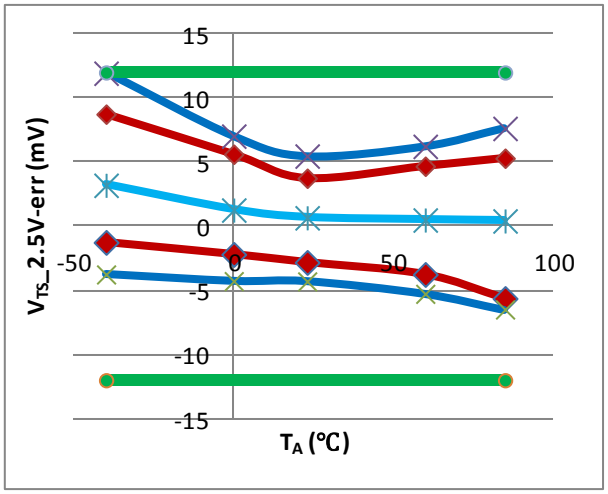


Figure 21: THM-n (n=0,1, 2) Channel Error (V_{THM} = 2.5V) vs. Temperature (-40~85°C)

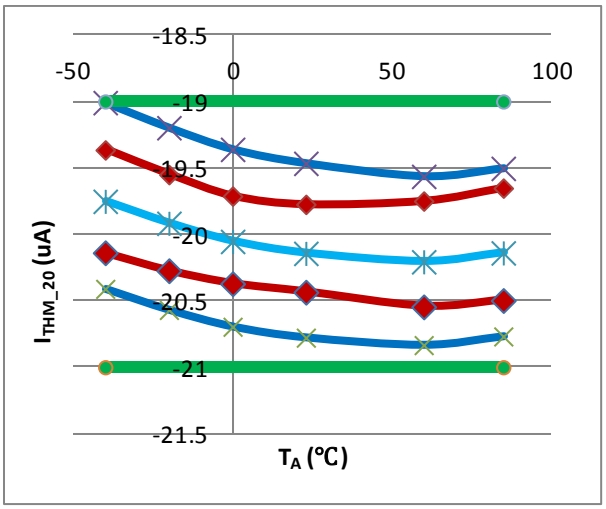


Figure 22: Temperature Characteristics (-40~85°C) of the Current Source on the THM pin (I_{THM}_20)

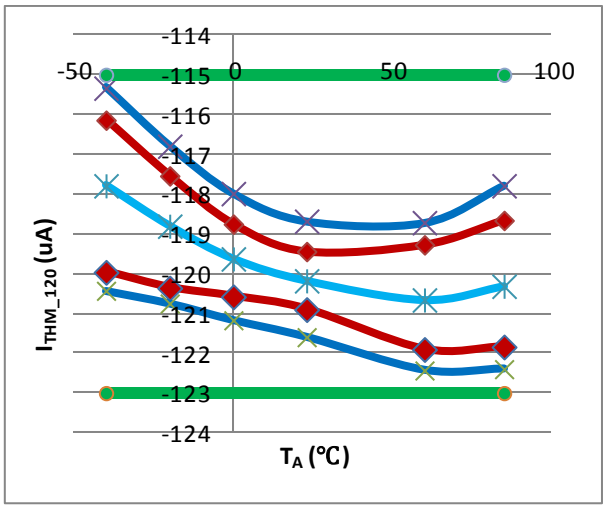


Figure 23: Temperature Characteristics (-40~85°C) of the Current Source on the THM pin (I_{THM}_120)

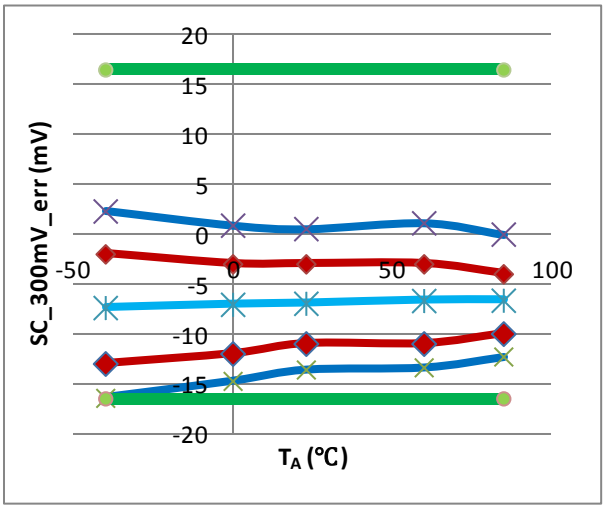


Figure 24: SC Threshold Error (V_{SC} = 300mV) vs. Temperature (-40~85°C)

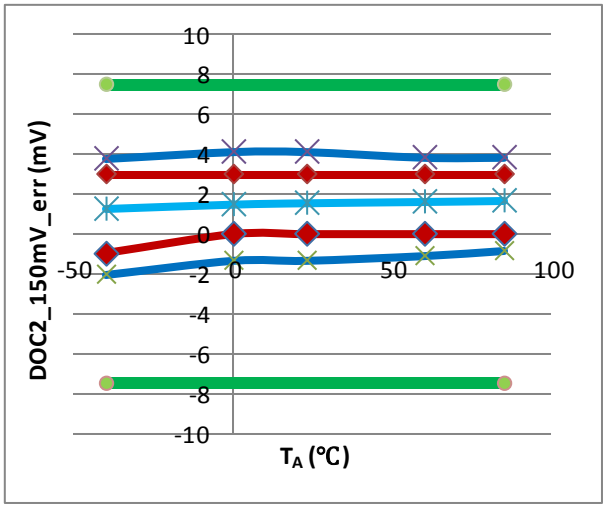


Figure 25: DOC2 Threshold Error (V_{DOC2} = 150mV) vs. Temperature (-40~85°C)

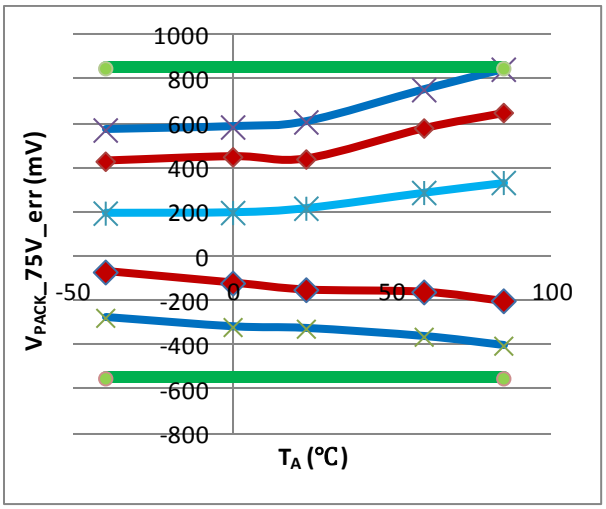


Figure 26: PACK Voltage Channel Error (VPACK = 75V) vs. Temperature (-40~85°C)

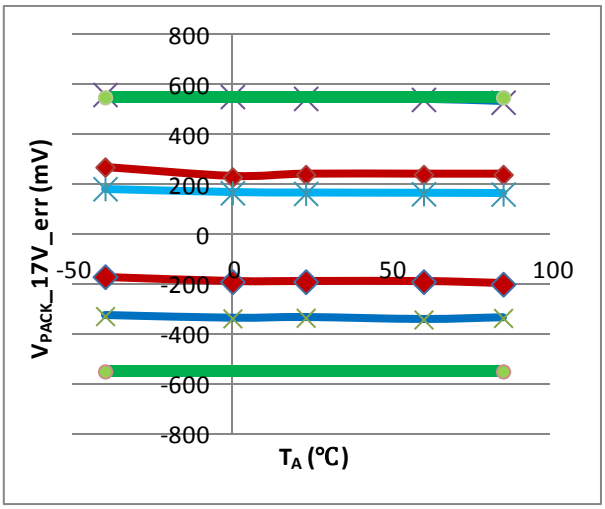


Figure 27: PACK Voltage Channel Error (VPACK = 17V) vs. Temperature (-40~85°C)

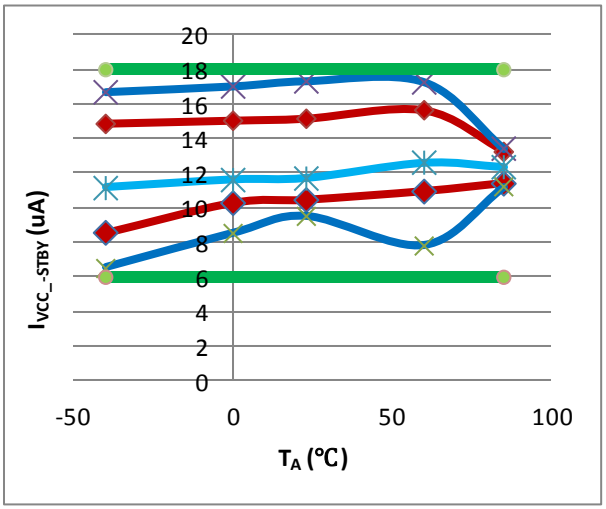


Figure 28: I_{VCC} in Standby Mode ($I_{VCC-STBY}$) vs. Temperature (-40~85°C)

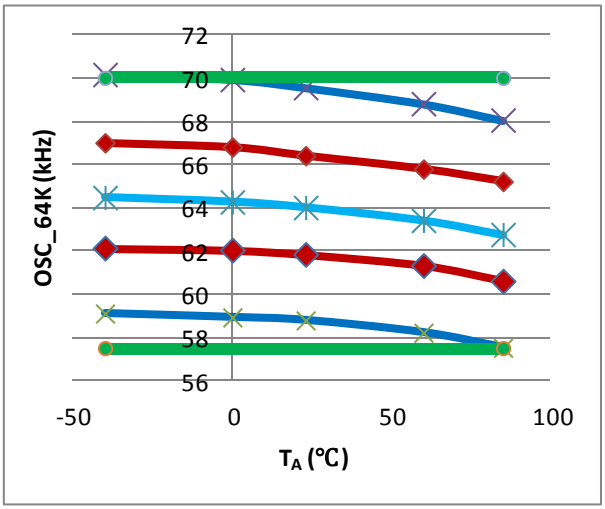


Figure 29: Temperature Characteristics (-40~85°C) of the OSC_64K Clock

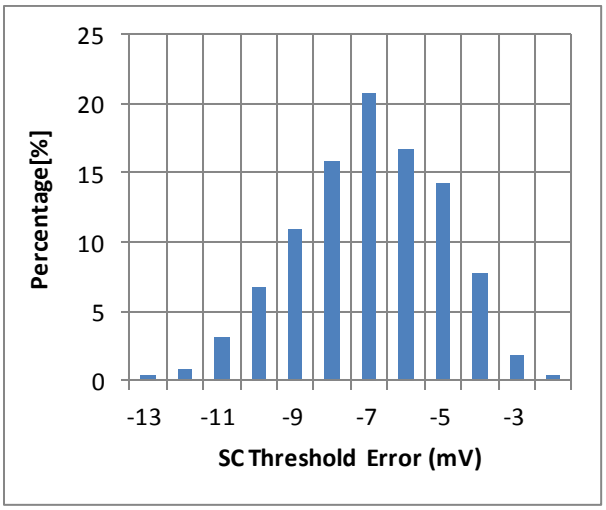


Figure 30: SC Threshold Error (V_{SC} = 300mV) Distribution (TA = -40~85°C)

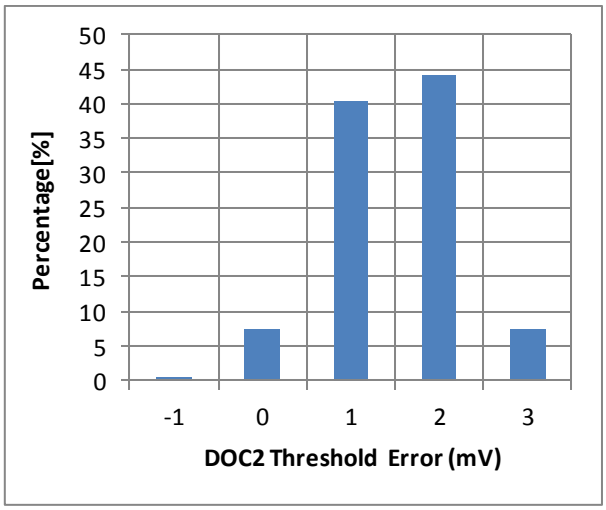


Figure 31: DOC2 Threshold Error (V_{DOC2} = 150mV) Distribution (TA = -40~85°C)

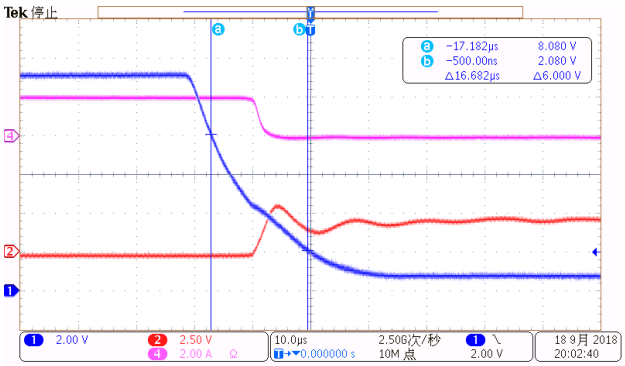


Figure 32: Typical charge FET turn-off characteristics
Channel 1: V_{GS} of charge FET
Channel 2: V_{DS} of charge FET
Channel 4: I_{DS} of charge FET
Test condition: V_{VBAT} = 34V; $V_{CHARGER}$ = 40V; Charge current = 2A (***Note 1***)

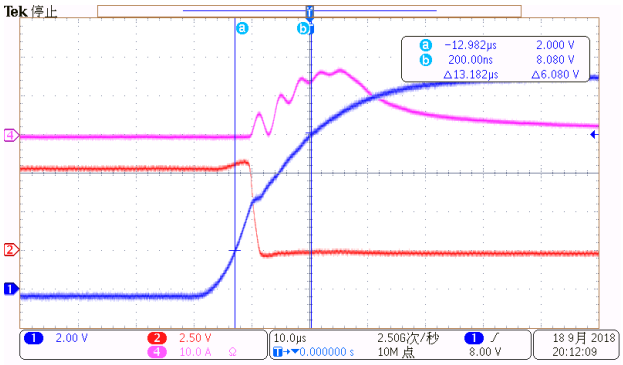


Figure 33: Typical charge FET turn-on characteristics
Channel 1: V_{GS} of charge FET
Channel 2: V_{DS} of charge FET
Channel 4: I_{DS} of charge FET
Test condition: V_{VBAT} = 34V; $V_{CHARGER}$ = 40V; Charge current = 2A (***Note 1***)

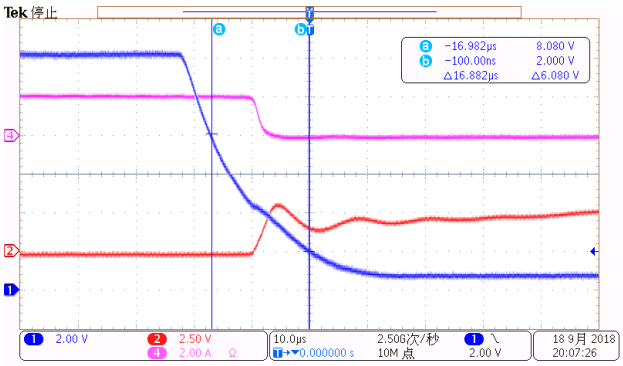


Figure 34: Typical charge FET turn-off characteristics
Channel 1: V_{GS} of charge FET
Channel 2: V_{DS} of charge FET
Channel 4: I_{DS} of charge FET
Test condition: V_{VBAT} = 34V; $V_{CHARGER}$ = 68V; Charge current = 2A (***Note 1***)

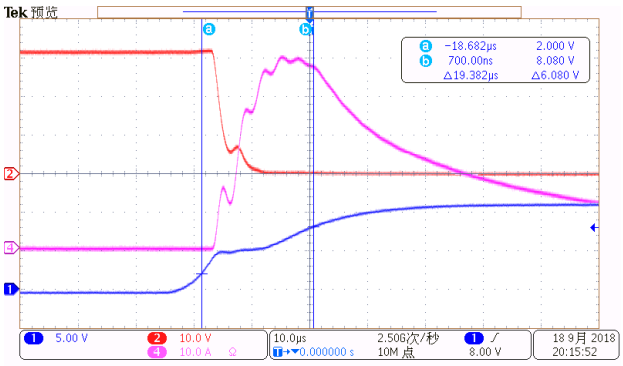


Figure 35: Typical charge FET turn-on characteristics
Channel 1: V_{GS} of charge FET
Channel 2: V_{DS} of charge FET
Channel 4: I_{DS} of charge FET
Test condition: V_{VBAT} = 34V; $V_{CHARGER}$ = 68V; Charge current = 2A (***Note 1***)

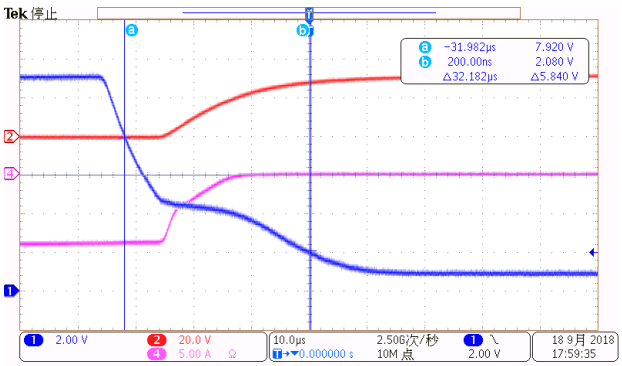


Figure 36: Typical discharge FET turn-off characteristics
Channel 1: V_{GS} of discharge FET
Channel 2: V_{DS} of discharge FET
Channel 4: I_{DS} of discharge FET
Test condition: V_{VBAT} = 34V; Discharge current = 10A (***Note 1***)

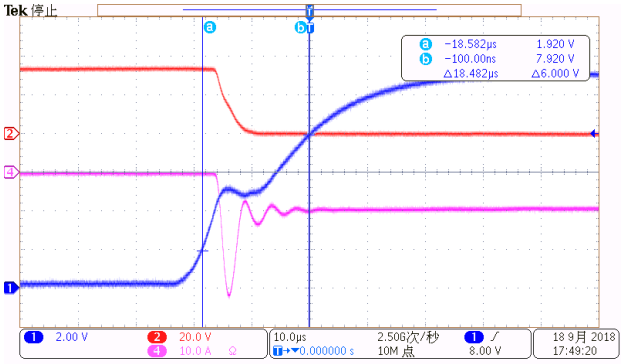


Figure 37: Typical discharge FET turn-on characteristics
Channel 1: V_{GS} of discharge FET
Channel 2: V_{DS} of discharge FET
Channel 4: I_{DS} of discharge FET
Test condition: V_{VBAT} = 34V; Discharge current = 10A (***Note 1***)

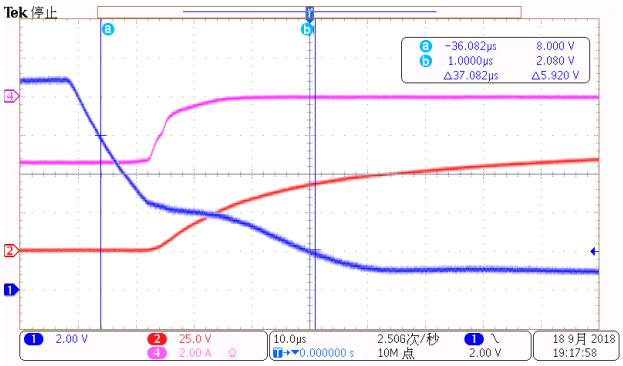


Figure 38: Typical discharge FET turn-off characteristics
Channel 1: V_{GS} of discharge FET
Channel 2: V_{DS} of discharge FET
Channel 4: I_{DS} of discharge FET
Test condition: V_{VBAT} = 68V; Discharge current = 4A (***Note 1***)

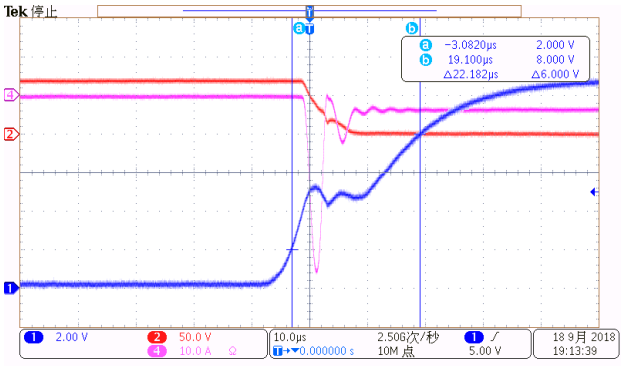


Figure 39: Typical discharge FET turn-on characteristics
Channel 1: V_{GS} of discharge FET
Channel 2: V_{DS} of discharge FET
Channel 4: I_{DS} of discharge FET
Test condition: V_{VBAT} = 68V; Discharge current = 4A (***Note 1***)

Note 1: The other test conditions are as following: C_{CP} = 1uF, $C_{iss\text{-}chg}$ + $C_{iss\text{-}dsg}$ = 18nF, and the charge and discharge FETs are turned on/off simultaneously; where C_{CP} denotes the charge pump capacitor, $C_{iss\text{-}chg}$ denotes the charge FET input capacitance and $C_{iss\text{-}dsg}$ denotes the discharge FET input capacitance.

AC TIMING

SPI BUS AC TIMING

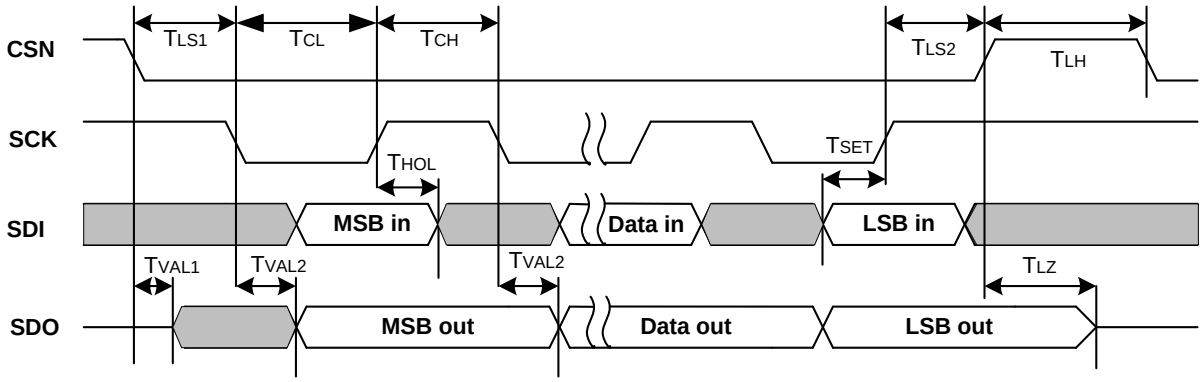


Figure 40: SPI Bus Timing

Table 4: SPI bus AC characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSN, SCK						
CSN assertion to first SCK edge		T_{LS1}	120			ns
Last SCK edge to CSN not asserted		T_{LS2}	120			ns
Terminal SCK						
SCK low period	Load capacitance at SDO < 2 nF	T_{CL}	0.475			µs
SCK high period	Load capacitance at SDO < 2 nF	T_{CH}	0.475			µs
Terminal SDI, SCK						
Data Input valid to SCK edge (Data Input Setup)		T_{SET}	30			ns
SCK sampling edge to data input invalid		T_{HOL}	30			ns
Terminal SDO, CSN						
CSN assertion to data out active	Load capacitance at SDO < 15 pF	T_{VAL1}	10		100	ns
CSN de-assertion to data high impedance	Load capacitance at SDO < 15 pF	T_{LZ}	10		100	ns
Terminal SDO, SCK						
SCK edge to data out valid (Data out delay)	Load capacitance at SDO < 15 pF	T_{VAL2}			100	ns
Terminal CSN						
Time between SPI cycles, CSN at high level (90%)		T_{LH}	15			µs

Note 1: *Test at T_A=23°C.*
Note 2: *Rise and fall times are measured from 10% to 90% of the signal amplitude.*

FUNCTIONAL DESCRIPTION

Auto-Scan

OZ3717 integrates a 14-bit SAR ADC to perform cell voltage, charge/discharge current, external/internal temperature measurements. In addition, OZ3717 provides internal ADC channels for the VBAT, VPACK, VMCU, V5 and AUX pins so that the voltages on these pins can be measured.

If Auto-scan is enabled, OZ3717 performs ADC measurement of all cell voltage and pack current every T_{DET} automatically.

The measurement time slot of Auto-scan is arranged as shown in **Figure 41**.

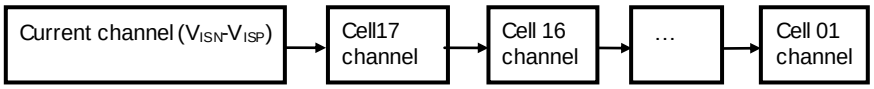


Figure 41: OZ3717 Auto-scan time slot arrangement

When each Auto-Scan cycle is finished, OZ3717 will check whether the OV, COC, DOC1 and UV thresholds are reached.

OZ3717 also provides a high-accuracy Auto-Scan mode by performing 8 consecutive ADC measurements for each channel then uses the average value as the final ADC value.

Trigger-Scan

Auto-Scan is automatically performed by OZ3717 when enabled. However, Trigger-scan can be initiated by external Host via SPI Bus command. Trigger Scan is implemented by setting ***trigger_scan_req*** (bit 7 of Register 0x5F) to "1". Trigger-scan channels are selected by setting ***trigger_scan_channel*** (bit [4:0] of Register 0x5F).

When ***trigger_scan_channel*** is set to 0x1E, OZ3717 will check whether the OV, COC, DOC1 and UV thresholds are activated after the Trigger-Scan is finished (Unless ***cto_detection*** (bit 5 of Register 0x5F) is set to "1"). In Trigger-Scan, OZ3717 also provides an option to select high accuracy mode with 8 consecutive ADC conversions for each channel and then using the average value as the final ADC value.

Trigger-Scan can be initiated anytime in Active mode. However, when Trigger-Scan command is received during performing of Auto-Scan, OZ3717 will not execute it until the present Auto-Scan cycle is completed. After one Trigger-scan is finished, OZ3717 will set ***trigger_scan_flag*** (bit 5 of Register 0x5E) to "1" to inform the external Microcontroller.

When Auto-Scan is disabled, OZ3717 will respond to the Trigger-Scan request immediately and start A/D conversion to the specified channels. Please check Table 5 for the time period to complete each specified Trigger-Scan.

Table 5: Time period to complete each specified Trigger-Scan

Trigger channels	The setting of *trigger_scan_channel[4:0]*	Trigger-1*(1) (ms)	Trigger-8*(2) (ms)
Cell 1	0x01	0.23	0.95
Cell 2	0x02	0.23	0.95
. . .	. . .		
Cell 17	0x11	0.23	0.95
PACK current	0x12	0.89	7.10
THM0	0x13	0.63	1.33
THM1	0x14	0.63	1.33
THM2	0x15	0.63	1.33
Internal temperature	0x18	0.23	0.95
VAUX	0x19	0.23	0.95
VPACK	0x1A	0.23	0.95
VBAT	0x1B	0.23	0.95
V50V	0x1C	0.23	0.95
VMCU	0x1D	0.23	0.95
For safety scan including all cell channels and PACK current channel	0x1E	4.82	23.3
For all channels including 0x01~0x1D	0x1F	9.35	35.6

*(1): Trigger-1 means that only one ADC measurement is performed to the specified channels.
*(2): Trigger-8 means that 8 consecutive ADC measurements are performed to the specified channels and then using the average value as the final ADC value.

Note: All the time values in Table 5 are based on the typical internal operating clock frequency of OZ3717 which may have the tolerance: +/-10%. In addition, all the time values are based on the setting ***sw_vref_enable*** = "1". If ***sw_vref_enable*** (bit 4 of Register 0x5A) is set to "0", OZ3717 needs to first start the reference voltage of the ADC and then performs the ADC to the specified channels, as takes about extra 2ms.

Multiple-Channel Multiplexer for 14Bit SAR ADC

14Bit fully-differential SAR type ADC is implemented with signed output in 16bit format. In single conversion mode, the SAR ADC's effective LSB = 312.5μV and reading LSB = 78.125μV, but 2 LSB bits are not effective data; in 8 consecutive conversion mode its effective LSB = 78.125μV and all 16bits are valid.

Table 6: SAR ADC Channel Gain

ADC Channel Name	ADC Channel Gain (Analog to Digital)	Comment
Cell voltage channels	2:1	LSB = (312.5μV/4)*2 = 156.25μV in 16bit operation register
Current channel	1:10	LSB = (312.5μV/4)/10 = 7.8125μV in 16bit operation register
Temperature, AUX channels	1:1	LSB = (312.5μV/4)*1 = 78.125μV in 16bit operation register
VMCU, V5	2:1	LSB = (312.5μV/4)*2 = 156.25μV in 16bit operation register
VBAT, VPACK	32:1	LSB = (312.5μV/4)*32 = 2.5mV in 16bit operation register

Note: only in high accuracy 8-consecutive conversion mode, are these LSBs effective.

Dedicated 16-bit ΣΔ ADC for High Precision Current Measurement and Coulomb Counting

16Bit fully-differential ΣΔ type ADC can measure the voltage range from -256mV to 256mV, with effective LSB = 7.8125μV, and conversion time = 64ms. Two working modes are provided for the 16Bit ΣΔ ADC: Single trigger conversion and consecutive conversion. Please refer to the description of Register 0x30 for detail.

When the 16Bit ΣΔ ADC works in consecutive conversion mode, the Coulomb counting value measured between ISN and ISP will be accumulated in Register 0x32 and 0x33 – Coulomb counter after each conversion. The 32-bit Coulomb counter provides the count range: -298261uV•h ~ 298261uV•h.

Battery State (Charge, Discharge or Idle) Determination

OZ3717 monitors the voltage drop across the current sense resistor between the ISP pin and ISN pin (the voltage across R_{SENSE} in the application board) to determine whether charge or discharge current is flowing in the battery pack, in order to correctly perform battery protection operations in various situations. In OZ3717's safety engine, 3 battery states related to charge/discharge are defined:

- Discharge-state
- Charge-state
- Idle-state.

OZ3717 determines whether the battery is in Discharge-state by 2 methods:

- Measure the voltage between ISP and ISN every T_{DET} with the SAR ADC
- Detect the voltage between ISN and GNDA with an analog comparator continuously

When the measured voltage is higher than $V_{DSG-TH1}$, or the detected voltage is higher than $V_{DSG-TH2}$, OZ3717 determines that the battery is in Discharge-state.

OZ3717 determines whether the battery is in Charge-state according to the measured voltage between ISP and ISN every T_{DET} by ADC. When the measured voltage (V_{ISN}-V_{ISP}) is lower than V_{CHG-TH}, the battery is in Charge-state.

If the battery is neither in Discharge-state nor in Charge-state, it is in Idle-state.

Power Modes

After power-on reset, OZ3717 will load calibration data into internal registers automatically, and then will enter Standby mode to wait for new command via SPI from the external Microcontroller. During the power-on reset, both discharge and charge MOSFETs are OFF, because the register control bits "***sw_dsg_ctrl***" (bit 0 of Register 0x59) and "***sw_chg_ctrl***" (bit 1 of Register 0x59) are logic low to switch off charge and discharge MOSFET as default.

OZ3717 has 3 power modes: Active mode, Standby mode and Shutdown Mode.

Active Mode:

(1) 5V LDO (V5) and Microcontroller LDO (VMCU) are alive;
(2) Reference (VREF) is alive;
(3) Charge Pump is enabled;
(4) Charge/Discharge MOSFET ON or OFF depends on internal safety events, software MOSFET control and EFETC (please see MOSFET control logic);
(5) Auto-scan will run automatically for safety check including OV, COC, DOC1 and UV if the functions are enabled by Microcontroller;
(6) Cell Balance will run if cell balance is configured by Microcontroller;
(7) Discharge-state/DOC2/SC check will be enabled when discharge MOSFET is ON;
(8) Charger-in detection is enabled when charge MOSFET is OFF, once Charger-in is detected, will send interrupt to Microcontroller;
(9) Load-on/off detection is enabled when discharge MOSFET is OFF, once load-off is detected, will send interrupt to Microcontroller for event release; otherwise, once load-on is detected, will send interrupt to Microcontroller;
(10) OSC512K is enabled;
(11) SPI can access internal registers;

(12) OZ3717 may perform trigger ADC scan at any time;
(13) SPI watchdog timer is enabled if this function is configured, if watchdog timeout, will send interrupt to Microcontroller, if no response from Microcontroller within 256ms, will enter Standby mode;
(14) Receive SPI command to switch to Standby mode or Shutdown mode.

Standby Mode:

(1) 5V LDO (V5) and Microcontroller LDO (VMCU) are alive;
(2) Reference (VREF) is alive;
(3) Charge Pump is disabled;
(4) Both charge and discharge MOSFET are OFF;
(5) Auto-scan is stopped;
(6) Cell-Balance is stopped;
(7) Discharge-state/DOC2/SC detection is disabled;
(8) Charger-in detection can be enabled or disabled by Microcontroller; once it is enabled and charger-in is detected, will send interrupt to Microcontroller;
(9) Load-on/off detection is enabled when discharge MOSFET is OFF (Microcontroller can disable it); once load-on is detected, will send interrupt to Microcontroller. If DOC2/SC flag is still there, once load-off is detected, will also send interrupt to Microcontroller for DOC2/SC release;
(10) OSC512K is disabled, but once Charger-in is detected, or Load-on is detected, or Load-off is detected during DOC2/SC flag = 1, OSC512K will be enabled;
(11) SPI can access internal register;
(12) Can perform trigger ADC or scan at any time, OSC512K will be also enabled when needed;
(13) SPI watchdog timer is disabled;
(14) Receive SPI command to switch to Active mode or Shutdown mode.

Shutdown Mode:

(1) When OZ3717 receives shutdown command (Please refer to Register 0x57) from SPI, it will shut down the power supply for itself and external Microcontroller;
(2) When UV event occurs and persists for the delay scan-cycle set in ***uv_shutdown_dly[1:0]*** (bits [15:14] of Register 0x4F), OZ3717 will enter Shutdown mode. This function can be disabled by setting ***uv_shutdown_th[3:0]*** (bits [3:0] of Register 0x4F) to 4'b0000.
(3) OZ3717 monitors the WKUP pin, when the voltage at this pin is higher than V_{WKUP}, OZ3717 will start power-on reset and then load calibration data into internal registers, finally enter standby mode to wait for the command from external host.

Power Modes Transition Diagram

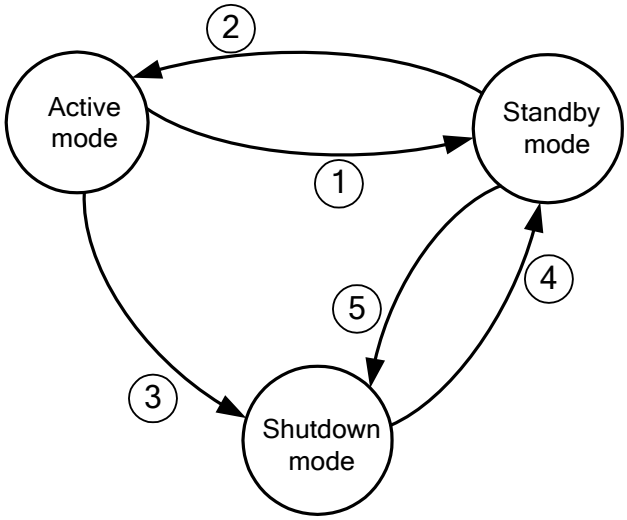


Figure 42: Power Modes Transition Diagram

Power Modes Transition Table

Table 7: OZ3717 Power Mode Transition Description

Transition	Initial Mode	Condition	Final Mode
1	Active	Case 1: Microcontroller sends standby command. Case 2: OZ3717 internal temperature is higher than the Thermal Standby Protection threshold (V_{TSP}).	Standby
2	Standby	Microcontroller sends command of entering Active mode.	Active
3	Active	Case 1: Microcontroller sends shutdown command. Case 2: When UV shutdown function is enabled, UV event occurs and persists for the setting delay scan-cycle.	Shutdown
4	Shutdown	The voltage on the WKUP pin is higher than V_{WKUP}.	Standby
5	Standby	Case 1: Microcontroller sends shutdown command. Case 2: When UV shutdown function is enabled, UV event is detected after Trigger-scan and persists for the setting delay scan-cycle.	Shutdown

Load-on/off Detection

In Standby mode or in Active mode with discharge FET off, OZ3717 can check the load on or off condition between PACK+/PACK- by checking the voltage drop over internal 100K (typical) resistor connected between VBAT and VPACK, If V_{VBAT}-V_{PACK} is higher than V_{LO}, OZ3717 determines that load is on; otherwise, load is off.

Charger-in/out Detection

In Standby mode or in Active mode with charge FET off, OZ3717 can check if a charger is plugged in or not. This is implemented by checking the voltage difference between the WKUP pin and VBAT pin. If the V_{WKUP}-V_{VBAT} is higher than V_{CHGIN}, OZ3717 determines that charger is plugged in; otherwise, charger is out.

Battery Pack Protections

1. Over-Voltage (OV) Protection

Li-ion cell chemistries require over voltage protection to prevent damaging the cell, or worse, thermal runaway, potentially leading to "rapid cell disassembly".

OZ3717 checks for cell over voltage once per detection time period (T_{DET}).
The over voltage protection is activated when:

- Any battery cell voltage is higher than V_{OVP} for T_{OV} (T_{OV} = 2, 4, 6 or 8 scan cycles).

The OV protection is released when:

1) All battery cell voltages decrease to less than V_{OVR}.

AND

2) The ***ovp_flag*** (bit 4 of Register 0x5E) is cleared (writing "1" into the flag bit).

When OZ3717 enters the OV protection state, it will turn off the charge FET, and generate an interrupt signal through INT pin if OV interrupt is enabled.

2. Discharge Over-Current Protection

OZ3717 has 3 levels of Over Current (OC) protection (V_{DOC1}, V_{DOC2} and V_{SC}). It checks for DOC1 once per detection time period (T_{DET}).

OZ3717 measures the voltage between ISP and ISN (V_{ISN}-V_{ISP}) by SAR ADC. When the measured voltage is higher than the V_{DOC1} for T_{DOC1}, the DSG pin outputs a low signal. This immediately turns OFF the discharge FET.
The DOC1 delay time (T_{DOC1}) can be set to 2, 4, 6, …, 16 scan cycles.

OZ3717 checks for DOC2 and SC with analog comparators. If the voltage between ISN and GNDA is higher than V_{DOC2} for T_{DOC2}, or higher than V_{SC} for T_{SC}, the DSG pin outputs a low signal. This immediately turns OFF the discharge FET.

- DOC2 delay time (T_{DOC2}) can be set to 1ms ~ 32ms, with 1ms/step.
- SC delay time (T_{SC}) can be set to 62.5µs ~ 1000µs, with 62.5µs/step.

DOC2 and SC could also generate an interrupt to Microcontroller through the INT pin if their interrupts are enabled.

After the discharge FET is turned off because of DOC2 or SC, the DOC2 and SC detection block will be disabled.

Discharge-Over-Current protections are released by clearing the corresponding flags (writing "1" into the flag bit).

3. Charge Over Current Protection

OZ3717 measures the voltage between ISP and ISN (V_{ISN}-V_{ISP}) with the SAR ADC. When the measured voltage is lower than the V_{COC} for T_{COC}, OZ3717 will turn off the charge FET. The COC delay time (T_{COC}) can be set to 2, 4, 6, …, 16 scan cycles.
When COC event is triggered, it could also generate an interrupt to Microcontroller through the INT pin if its interrupt is enabled.

Charge-Over-Current protection is released by clearing the corresponding flag (writing "1" into the flag bit).

4. Under-Voltage (UV) Protection

When UV shutdown function is enabled, and UV event occurs (any cell voltage is lower than the UV threshold set by ***uv_shutdown_th[3:0]***) and persists for 2 scan-cycle, OZ3717 will generate an interrupt to Microcontroller if its interrupt is enabled. Then after the setting delay scan-cycle (set by ***uv_shutdown_dly[1:0]***) is reached, OZ3717 will directly enter Shutdown mode.

When UV shutdown function is disabled, OZ3717 will not check UV event.

Temperature Measurement and Protection

1. External Temperature Measurement

OZ3717 uses the temperature sensor circuit as shown in below figure to measure the external temperature.

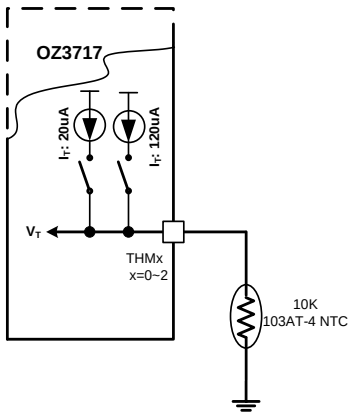


Figure 43: Temperature Sensor Circuit

Temperature sensor voltage V_T observed on the THMx (x=0, 1, 2) pin with 10K NTC Thermistor.

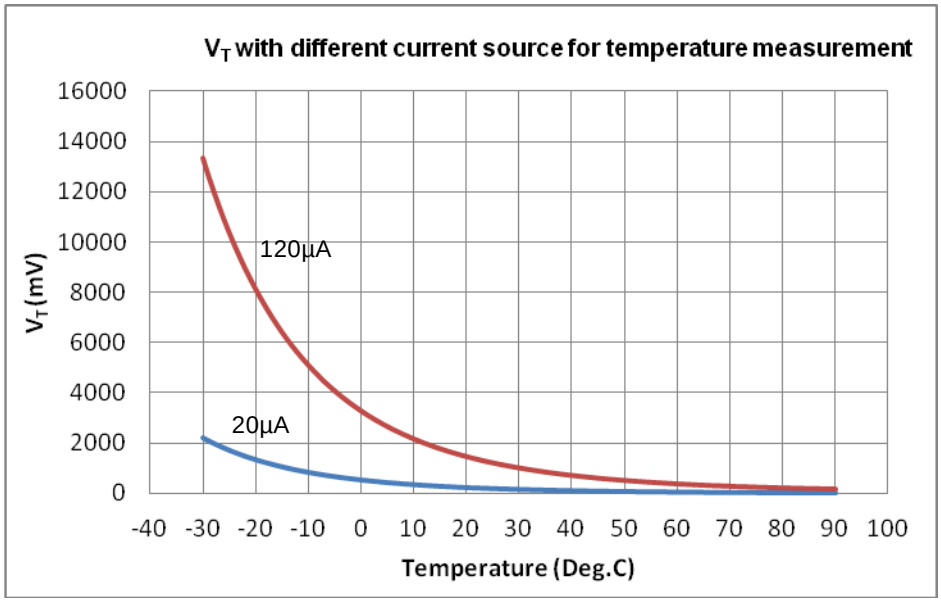


Figure 44: V_T vs. Temperature

2. Internal Over Temperature (IOT) Protection

OZ3717 integrates a die temperature sensor. It converts the chip internal temperature to an analog voltage for Internal Over-Temperature protection:
1) Prohibiting cell balance;
2) Cut off the power supply to external host and enter Standby mode. And could generate the interrupt if its interrupt is enabled

- Cell-Balance Over-Temperature (CBOT) threshold: 125°C @typical
- Cell-Balance Over-Temperature release value: 100°C @typical

- Thermal Standby Protection (TSP) threshold: 150°C @typical
- Thermal Standby release value: 125°C @typical

Cell-Tap-Open Detection (CTO)

All the Battery Pack Protection features described above assume the Cells and Protection Printed Board Assembly are securely connected. However, there may be connectors used between the cells and protection board that may fail; either completely or intermittently. Further, the application may subject the entire system to severe shock and vibration that may result in completely or intermittently broken wires. In short, the wires connecting the Cells to the protection board → Cell-Tap Connections are essential for a safe and protected LiIon Battery Pack. Without protection Li-Ion Battery Packs may experience catastrophic failures; over-heating, fires, explosions.

OZ3717 integrates a CTO detection function. It is initiated by the external host (Microcontroller) but executed by OZ3717 itself. The procedure is as following:

1. OZ3717 receives the trigger scan command with ***cto_detection*** (bit 5 of Register 0x5F) set to "1".
2. OZ3717 follows the Auto-scan sequence to turn on the internal cell-balance switch for the configured cells. When the cell is selected for CTO detection, the cell balance switch will shorten the positive BAT input pin and negative BAT input pin for a few 100us time period first, and then perform the ADC cell voltage measurement and store the measured ADC data into the selected cell register.
3. OZ3717 performs CTO check for the next cell until all the configured cells are finished, OZ3717 sends an interrupt signal to external host (Microcontroller).
4. External host reads all cells ADC data and then determines whether a CTO fault has occurred. If there is CTO fault on a cell channel, the read voltage for this channel will be very low (close to 0).

Cell-Balance

No two Lithium cells are identical. There are always slight differences in the state-of-charge, self-discharge rate, capacity, impedance and temperature characteristics. After numerous charge-discharge cycles, these variations eventually lead to cell voltage differences within the battery pack. Since charging terminates when the highest cell reaches the over voltage condition, even if other cells are at much lower voltages, usable capacity is lost.

The solution to cell in-balance is to equalize cell voltages through "cell balance". OZ3717 equalizes cell voltages by diverting some of the charging current outside the selected cell through load resistors "passive balance". The other cells are receiving full charging current while the selected cell has less charge current. After a period of time the rest of the cells will catch up to the cell voltage of the selected cell.

The cell balance decision is made by external Microcontroller (Host) and also initialized by external Microcontroller. Once receiving the cell balance command, OZ3717 will execute to turn the target cell balance switch. The maximum internal cell balance current is 10mA per cell. If faster cell balance is required by the application, an external cell balance circuit may be used.

It should be noted that cell balance is paused when OZ3717 is performing ADC measurement. In addition, it is prohibited to perform cell balance for adjacent cells at the same time.

Cell balancing automatically stops after T_{CB} (typical: 30 seconds). If further balance is needed, the Host must resend a command to balance the selected cells every T_{CB}.

1. Internal Cell Balance

The internal cell balance switches (equivalent Rdson ≈400 Ω) could be enabled for the selected cell and generate the bypass current. **Figure 45** gives the typical I-V characteristics between BATn and BATn-1 pins(where, n=1, 2, …, 17) when cell balance is being done for cell n (RF=51Ω).

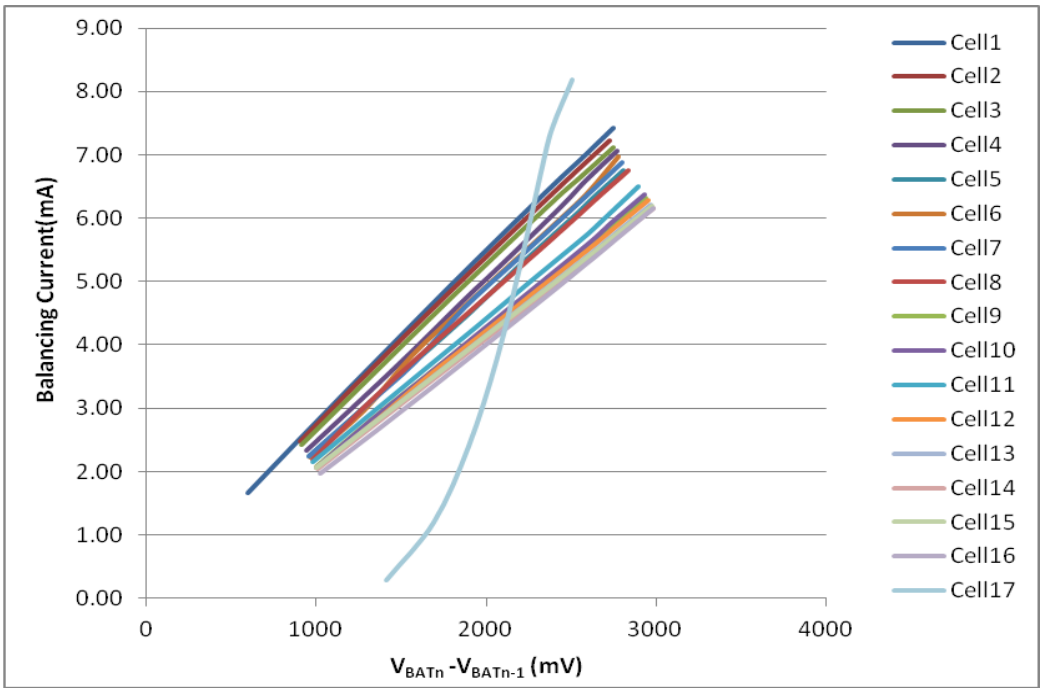


Figure 45: T ypical I-V characteristics between BATn and BATn-1 pins when cell balance is performed for cell n (n=1, 2, …, 17).

Non-neighboring cells can be selected for balancing simultaneously, however, when OZ3717 internal temperature exceeds 125°C (typical value), Cell-Balance Over Temperature (IOT) protection event will be triggered, then internal cell balance will be stopped.

2. External Cell Balance

An external circuit is needed when higher balance current is required. Please refer to **Figure** 46**.** The external balance current is determined by cell voltage, the Collector – Emitter voltage of Qbn and the value of resistor RBn. When the internal balance switch is turned on, the internal balance current flows through RFn-1 and then transistor Qbn will turn on if its Base - Emitter voltage is high enough. When following equation is met, the external cell balance can be turned on.

$$V_{CELLn} * RF_{n-1} / (RF_n + RF_{n-1} + R_{ON-B}) > V_{BE0(QBN)}$$

Where V_{CELLn} denotes the voltage of Celln, $V_{BE0(QBN)}$ denotes Q_{BN} turn-on minimum Base-Emitter voltage; R_{ON-B} denotes the resistance of the internal balance switch during ON state (its typical value is 400Ω). Assuming $V_{BE0(QBN)}$ = 0.7Vs and $RF_n = RF_{n-1}$, and minimum cell balance start voltage V_{CELLn} > 3.5V, the minimum RF_n value could be obtained based upon above the equation to ensure the proper operation of the designed external balance circuit. It is suggested to use 120Ω resistor for RF_n.

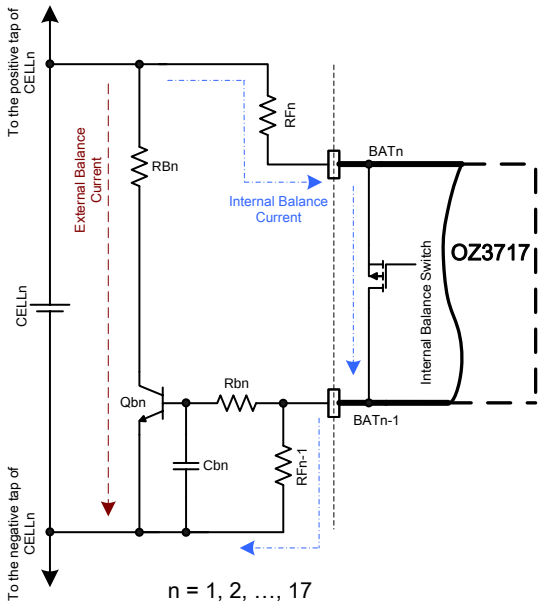
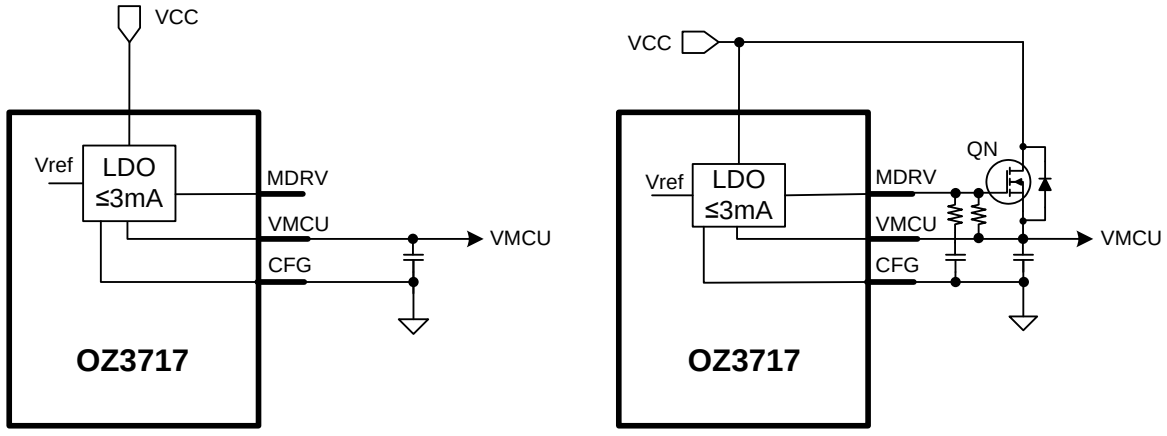


Figure 46: External balance circuit (cell 1 to 17)

Microcontroller LDO

OZ3717 integrates one LDO (VMCU) to power a Microcontroller. The LDO output voltage is selectable: 3.3V or 5V. LDO voltage selection is O2Micro factory configured before product shipment. After configuration, it cannot be changed.

OZ3717 internal LDO VMCU can provide static current of 2mA (typical) current to the Microcontroller and up to 30mA dynamic current (for example, surge current to charge filter capacitors at first power-up).
When higher continuous current driving capability is needed, an external N-type power MOSFET QN can be added.



Light load application (<3mA) **High load application (>3mA)**

Figure 47: Microcontroller LDO configuration

When QN is added, additional RC compensation stability network should be added from the MDRV pin to ground. Also a pull-down resistor is suggested to be added from VMCU to MDRV so that the MDRV pin is not floating when it doesn't drive QN on.
Microcontroller LDO has three working modes

a. Internal LDO only: When the control bit ***sw_vmcu_enable[1:0]*** =2'b10 (Default) in PWRMD register 0x57[5:4], only internal LDO is allowed and external QN will be forced off under any loading condition.
b. External LDO only: When the control bit ***sw_vmcu_enable[1:0]*** =2'b01 in PWRMD register, only external LDO is allowed and there is no working mode change even at light load (<3mA) condition
c. Auto-mode: When the control bit ***sw_vmcu_enable[1:0]*** =2'b11 in PWRMD register, Internal LDO and external pass transistor QN can automatically respond to external load dynamic change from low (<3mA) to high (>3mA) or vice versa

QN selection will depend upon the maximum allowed temperature increase determined by the maximum pack voltage, maximum load current and QN package thermal performance.
Also with QN additional feedback devices can be added to clamp the high transient current. Please refer to typical application schematics in **Figure 4**, where Q20 and R51 provide the feedback loop to protect QN (M1).

FET Driver & Control

OZ3717 integrates a charge pump circuit to raise the voltage on the VCP pin to V_{VCM} + 12V (typical). Then applies the voltage to the CHG and DSG pin for driving the gates of external N channel charge and discharge MOSFETs. The charge pump is always enabled in Active mode, but disabled in Standby Mode. It should be noted that the charge pump needs some time (T_{CP-OK}) to start up after OZ3717 transits from Standby mode to Active mode. The external host can check whether the charge pump voltage is ready by the status of ***cp_ok*** (bit 6 of Register 0x5B), which is asserted by OZ3717 when the charge pump voltage goes up to $V_{CP-FINAL}$ - 2 V, where $V_{CP-FINAL}$ is the final charge pump voltage at the static condition when it is turned on.

The charge pump capacitor (C_{CP}) value is critical for the circuit characteristics. Following equation is used to estimate C_{CP}.

$$C_{CP-MIN} = 50 * (C_{iss-chg} + C_{iss-dsg})$$

where C_{CP-MIN} is the minimum available charge pump capacitor, $C_{iss-chg}$ is the charge FET input capacitance, $C_{iss-dsg}$ is the discharge FET input capacitance. By using the charge pump capacitor value calculated with above equation, it can be ensured that $V_{VCP} - V_{VCM} < 2V$ when the charge and discharge FETs are turned on simultaneously.

A simple safety engine is also integrated in OZ3717. The engine will check for OV, UV, COC and DOC1 events according to the Cell ADC and current ADC reading during Auto-Scan or Trigger-Scan. However, the OV, UV, COC and DOC1 protections may be enabled or disabled independently. Please refer to the description of Registers 0X4F, 0x50, 0x51 and 0x52.

OZ3717 provides for external host control of the charge and discharge FET with the EFETC pin. The EFETC pin can be set to control either the charge FET or the discharge FET or both FETs. Please refer to the description of Register bits ***efetc_mode[1:0]*** (bits [12:11] of Register 0x51) for detail.

OZ3717 also provides the charge FET and discharge FET control bits (***sw_chg_ctrl*** and ***sw_dsg_ctrl***) enabling the external host to force the charge FET or discharge FET off. After charge pump enabled, ***dsg_drv***/***chg_drv*** will not be allowed to be enabled until ***cp_ok*** = "1" has been active for ≥64ms.

However, the ON or OFF status of the charge FET and discharge FET depends upon:

- The control bits
- Safety engine output
- and the EFETC pin status and setting.

OZ3717 integrates constant current Pre-charge and Pre-discharge control.
This feature is implemented by regulating the:

- Charge FET in linear mode during Pre-charge mode
- Discharge FET in linear mode during Pre-discharge mode

In either Pre-charge or Pre-discharge mode, the predefined charge or discharge current can be set to regulate charging or discharging in constant current mode.

The Pre-discharge can be enabled only when the following conditions are all met:

1) OZ3717 in Active mode

AND

2) The safety engine in OZ3717 permits discharge, when the flag bits ***doc1p_flag***, ***doc2p_flag*** and ***scp_flag*** are all "0"

AND

3) If the EFETC pin is set to control the discharge FET (please refer to Register 0x51 for EFETC configuration), its status should permit discharge

AND

4) The register bit ***sw_dsg_ctrl*** is set to "1"

The Pre-charge can be enabled only when following conditions are all met:

1) OZ3717 in Active mode

AND

2) The safety engine in OZ3717 permits charge, it means the flag bits ***cocp_flag*** and ***ovp_flag*** are both "0"

AND

3) If the EFETC pin is set to control the charge FET, its status should permit charge

AND

4) The register bit ***sw_chg_ctrl*** is set to "1".

The Pre-charge and Pre-discharge have one enable setting: ***pre_sel[1:0]*** (Register 0x59[3:2]).

- When it is set to "01", pre-charge is enabled.
- When it is set to "10", pre-discharge is enabled.
- When it is set to "00" or "11", Pre-charge and pre-discharge are both disabled.

So either pre-charge ***OR*** pre-discharge can be enabled. ***It is impossible to enable both.***

The Pre-charge or Pre-discharge current is set by ***pre_set[6:0]*** (Register 0x59[14:8]).
The setting range is from 100uV/R_{SENSE} to 12.8mV/R_{SENSE}. The setting step is 100uV/ R_{SENSE}.

If the discharge FET has been on before Pre-discharge is enabled, when OZ3717 receives the Pre-discharge command from Microcontroller, it will first turn off the discharge FET for 250us, and then start Pre-discharge.

When the discharge FET is off because "***sw_dsg_ctrl***" is "0", setting ***pre _sel[1:0]*** to "10" and "***sw_dsg_ctrl***" to "1" at the same time (the 2 settings are in the same Register) can initiate pre-discharge directly.

If the charge FET has been on before Pre-charge is enabled, when OZ3717 receives the Pre-charge command from Microcontroller, it will first turn off the charge FET for 250us, and then start Pre-charge.

When the charge FET is off because "***sw_chg_ctrl***" is "0", setting ***pre _sel[1:0]*** to "01" and "***sw_chg_ctrl***" to "1" at the same time (the 2 settings are in the same Register) can initiate pre-charge directly.

Force Charge FET on when Battery in Discharge-state

In 2-terminal applications, when charge FET is off but discharge FET is still on, OZ3717 would turn on the charge FET immediately when it detects that battery is in Discharge-state.

With this feature, the low or high discharge current would not go through the charge FET body diode as this would cause the charge FET to overheat or burn in 2-terminal applications.

In 3-terminal applications, when charge FET is off but discharge FET is on, OZ3717 would not turn on the charge FET when battery is in Discharge-state.

2-terminal or 3-terminal application is specified by the parameter ***type_cfg***.
Please refer to the description of Register 0x52 for detail.

Force Discharge FET on when Battery in Charge-state

In 2-terminal applications, when discharge FET is off but charge FET is on, OZ3717 would force the discharge FET on immediately when it detects that battery is in Charge-state.

In 3-terminal applications, when discharge FET is off but charge FET is on, OZ3717 would not turn on the discharge FET when battery is in Charge-state.

Interrupt to External Host

OZ3717 provides a digital push-pull output pin, named INT, used to inform the external host that a fault event has occurred and the host should take some battery management action. The interrupt signal may be low Active signal or 100Hz square wave, as is selected by Register bit ***intrpt_type*** (bit 13 in Register 0x53).

SPI Bus

4-wire SPI bus (CSN, SCK, SDI, SDO) is used to generate corresponding direct read/write operation for OZ3717 register file.

SPI has 4 modes for data transmission format. OZ3717 adopts the clock phase (CPHA=1) and polarity mode (CPOL=1). That means the SDI is latched on the rising edge of SCK and the SDO is clocked out on the falling edge of SCK. In a data transmission, every byte consists of 8 bits and it is transmitted with the most significant bit (MSB) first. SPI's clock from the external master is asynchronous to the local clock, so the synchronization mechanism between two clock domains is executed.

OZ3717 supports SPI parallel configuration. As shown in following Figure 48, in SPI parallel configuration, all the slave devices' SCK, SDI and SDO pin are paralleled to the SPI master; every slave device has its own CSN and it will response only when its CSN is active.

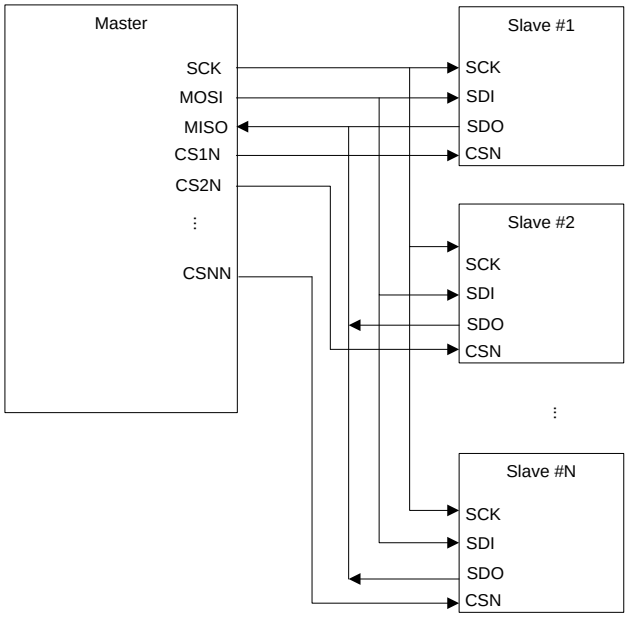
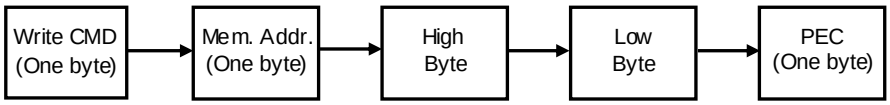


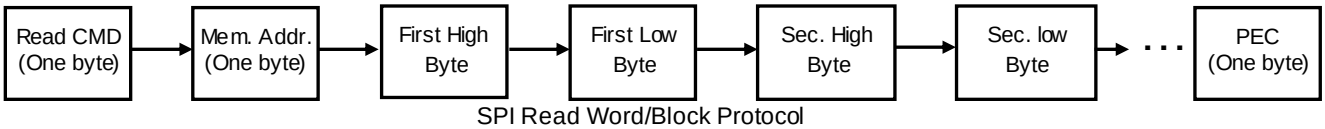
Figure 48: SPI Parallel Configuration

The read/write protocols are shown at the following.

OZ3717



SPI Word Write Protocol



SPI Read Word/Block Protocol

Write/Read Command Definition:

Command	Memory Type	Description
0011nnnn	Register Read & Write	Register Read Command, nnnn is used to specify the block size, where nnnn=0 for one word read, and nnnn=M for block size M+1 words read. It supports 16 words, maximum in one block.
11000101		Register Write Command, it can only support one word write.

Note 1: for each "Write" command, if the PEC check failed, OZ3717 will abort this command and record the PEC failure in corresponding register.

Note 2: The word will be written into corresponding memory at the rising edge of CSN pin.

During SPI communication, the SDI is looped back to SDO for all byte data in write command, so that the host can compare the sent data and received data if same or not, if not the same, that means an error occurred. For read command, just the first two bytes (Read command and Memory address) are looped back to the host, and after that, the slave data will be sent on SDO, and the PEC will be calculated for all data including command and memory address. Besides this method, host can check SDO before the first falling edge of SCK, if it is low, that means there was CRC error in the last write command, or check SDO after the last rising edge of SCK during CSN = "0", if it is low, that means the current write command has CRC error.

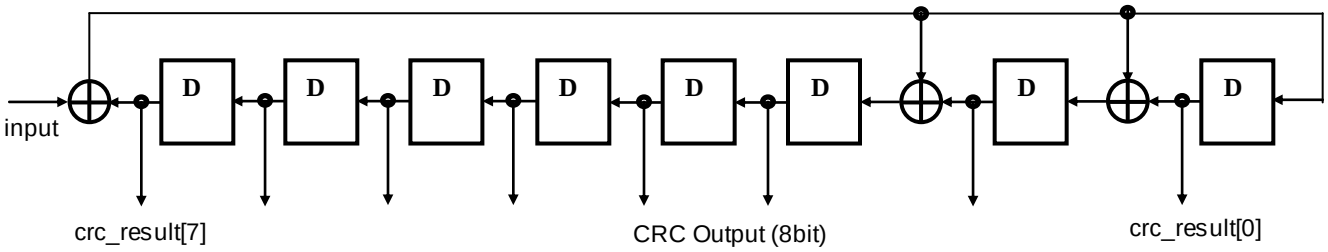
PEC (Packet Error Correction) Algorithm

The Cyclical Redundancy Check (CRC) generation polynomial is x^8+x^2+x+1, and the PEC calculation covers all data in each protocol. The initial PEC code is 8'h00, for every bit is transmitted or received, the PEC calculation as follows:

> new PEC <= {PEC[6:2], PEC[1]^PEC[7]^bit, PEC[0]^PEC[7]^bit, PEC[7]^bit}, where bit is the received or transmitted bit.

For the receiver, if the final PEC code is 8'h00, the PEC is OK; otherwise, the PEC is failed.

The corresponding implementation is shown as follows.



SPI WDT (Watch-Dog Timer) Function

OZ3717 supports SPI watchdog function. The watchdog timer range is defined in the register "***spiwdt_timer***" (Register 0x54[7:0]). If this function is enabled and the corresponding interrupt is not masked, OZ3717 will perform following actions:

1) Send an interrupt if no normal SPI communication (including no SPI communication or the time of communication too long) within the defined time (selectable;1Sec ~ 255Sec range with 1Sec/step).
2) Send out reset signal (active low for 64ms) on the WDT pin to reset Microcontroller if no SPI communication within 256ms after the interrupt. Meanwhile, OZ3717 will enter Standby mode automatically.

APPLICATION GUIDELINES

Cell Connection Sequence

To ensure proper operation of the OZ3717, the following cell connection sequence is recommended:

1) Connect Ground
2) Connect VCC
3) Connect cells in any order

Input filter Considerations

For best measurement accuracy, input filters are required. The design of each input filter must take into account the characteristics of the application as well as overall system considerations.

In applications with inductive loads or motor commutation brushes, noise is generated during normal operation while the battery is in discharge mode. Noise reduces the accuracy of cell voltage measurement.

O2Micro recommends a filter configuration in which a capacitor is placed in-between each input and analog ground (**Figure 49**). This configuration provides high attenuation of input noise. The breakdown voltage rating of the capacitors must be considered.

O2Micro recommends a filter resistor value of 120 Ω to improve cell voltage measurement accuracy. Considering that the resistor may suffer high power during pack assembly or cell balance, 0805 package or bigger size is preferred.

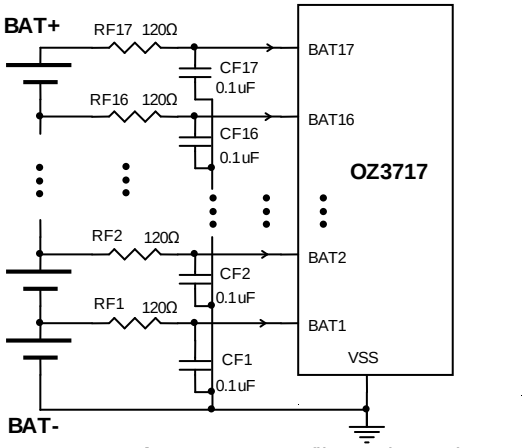


Figure 49: Input filter schematic

The filter capacitors (CF_1 to CF_{17}) can be computed by taking into consideration the worst case noise:

$$C_F = \frac{\Delta t \times V_{PP}}{\Delta V_{MAX} \times R_F} \quad (1)$$

Where:

- C_F [µF] is the filter's capacitor value.
- R_F [Ω] is the filter's resistor value, 120Ω in typical application schematics.
- V_{pp} [V] is the peak to peak noise magnitude.
- ΔV_{MAX} [V] is the maximum voltage perturbation acceptable at the output of the input filter.
- Δt [µs] is the ON time of the perturbation.

Let's take an application with worst case peak-to-peak noise magnitude of 20 V for 1 µs. We set ΔV_{MAX} = 500 mV and obtain:

$$C_F = \frac{1 \times 20}{0.5 \times 120} = 0.33 \mu F \quad (2)$$

C_F value of 0.33 µF is appropriate for most applications. System designers can make tradeoff between the cost of C_F capacitors and the maximum acceptable voltage perturbation. O2Micro uses 0.1 µF for the C_F value in the typical application schematics of OZ3717.

VCC filter recommendation

If OZ3717 is used in a high-noise environment, the input voltage at the VCC pin must be properly filtered.

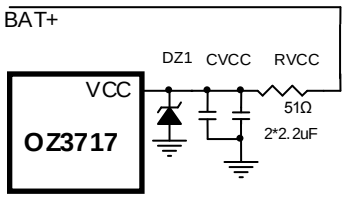


Figure 50: Typical power supply input filter

The input capacitor for VCC must be large enough to maintain VCC > V_{P-DN} during normal operation when the battery voltage drops while supplying a highly inductive load in PWM working mode. A total 4.4 µF CVCC capacitor is more than sufficient for most applications.

If V_{BAT+} is above the regulation voltage of DZ1, all excess power will be dissipated in the Zener diode DZ1 and the resistor R_{VCC}. Moreover, R_{VCC} must be able to withstand inrush current during pack assembly when CVCC is initially at 0V. The system designer should consider the following component parameters

For DZ1:

- Non-repetitive peak reverse current
- Total power dissipation

For RVCC:

- Total power dissipation

Reduced Cell Count Applications

OZ3717 may be used in applications from 10 cells in series, 10S, up to 17 cells in series, 17S.
For applications with less than 17 cells in series it is necessary to short input pins together as shown in the diagram below.

***Warning**: Do not leave any BATn (n=9, 10, … , 16) pins open circuited. BATn (n=9, 10, … , 16) pins must be either connected to cells or shorted to an upper pin.* BAT17 must always be connected to the positive pin of the highest cell, through the appropriate discrete component network.

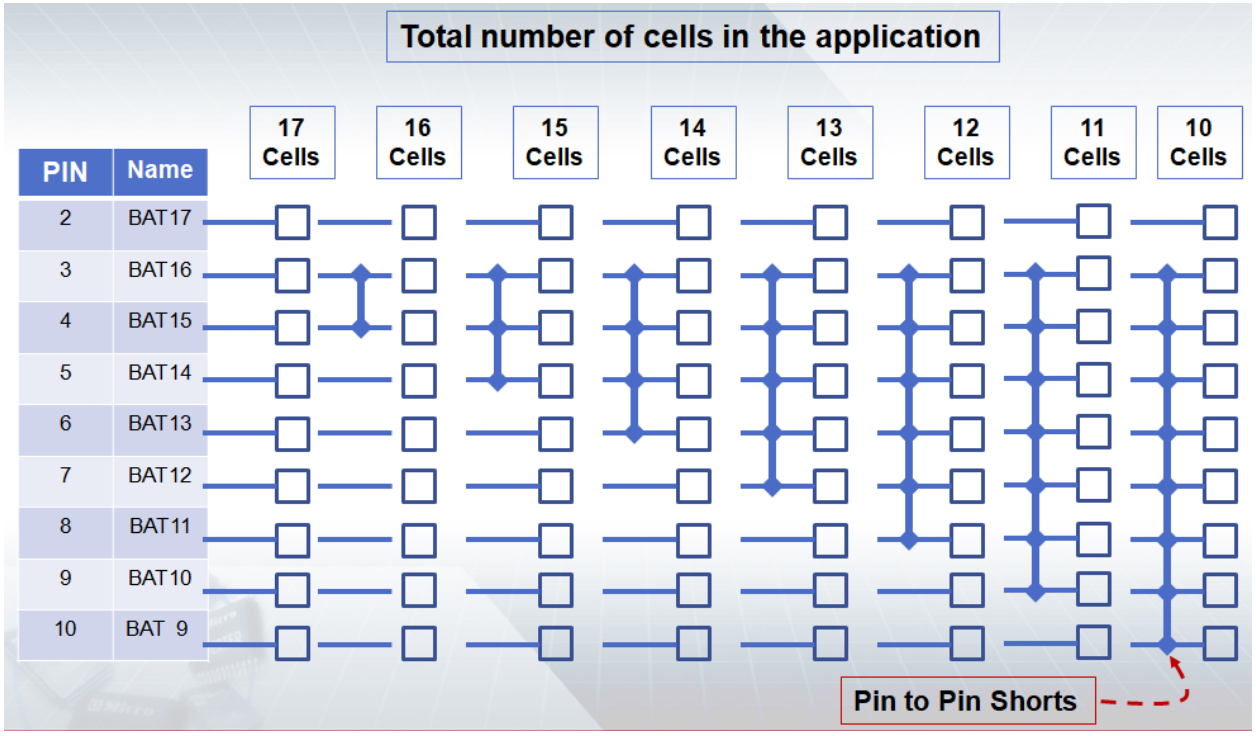


Figure **51**: Pin-to-pin shorting connections when using OZ3717 with less than 17 cells.

REGISTER MAP AND DEFINITIONS

Reg. Index (h)	Reg. Name	Bit Number															
		High byte								Low byte							
		15(7)	14(6)	13(5)	12(4)	11(3)	10(2)	9(1)	8(0)	7	6	5	4	3	2	1	0
0x00	HWID (RO)	***chip_id[15:0]*** = 0x7717															
		Use the part number as the chip ID.															
0x01	CELL1	***cell01_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x02	CELL2	***cell02_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x03	CELL3	***cell03_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x04	CELL4	***cell04_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x05	CELL5	***cell05_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x06	CELL6	***cell06_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x07	CELL7	***cell07_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x08	CELL8	***cell08_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x09	CELL9	***cell09_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0A	CELL10	***cell10_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0B	CELL11	***cell11_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0C	CELL12	***cell12_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0D	CELL13	***cell13_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0E	CELL14	***cell14_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x0F	CELL15	***cell15_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.															
0x10	CELL16	***cell16_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4,															

0x11	CELL17	***cell17_adc_data[15:0]*** (read only) signed data with LSB = 0.625mV/4.
0x12	PACKC	***packc_adc_data[15:0]*** (read only) pack current ADC value by SAR ADC, signed data with LSB = (0.3125mV/10)/4, (positive means charge, negative means discharge)
0x13	THM0	***thm0_adc_data[15:0]*** (read only) signed data with LSB = 0.3125mV/4.
0x14	THM1	***thm1_adc_data[15:0]*** (read only) signed data with LSB = 0.3125mV/4.
0x15	THM2	***thm2_adc_data[15:0]*** (read only) signed data with LSB = 0.3125mV/4.
0x16 ~ 0x17	Reserved	***Reserved***
0x18	INTMP	
0x19	VAUX	***vaux_adc_data[15:0]*** (read only) signed data with LSB = 0.3125mV/4.
0x1A	VPACK	***vpack_adc_data[15:0]*** or ***wkup_adc_data[15:0]*** (read only) signed data with LSB = (0.3125mV/4) * 32.
0x1B	VBAT	***vbat_adc_data[15:0]*** (read only) signed data with LSB = (0.3125mV/4) * 32.
0x1C	V50V	***v50v_adc_data[15:0]*** (read only) signed data with LSB = 1.25mV/4.
0x1D	VMCU	***vmcu_adc_data[15:0]*** (read only) signed data with LSB = 1.25mV/4 (May be 5V output or 3.3V output).
0x1E	Reserved	***Reserved***
0x1F~ 0x2F	Reserved	***Reserved***

<table>
<tr><td rowspan="2">0x30</td><td rowspan="2">CADCTRL</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>hw_ cadc_ ctrl</td><td>N/A</td><td>N/A</td><td>cc_ always_ enable</td><td>conse_ cadc_ rdy_ enable</td><td>hi_ acy_ mode</td><td>sw_cadc_ ctrl[1:0]</td></tr>
<tr><td colspan="15">hw_cadc_ctrl: (R/W, default = “1”), this bit is used to tune the CADC performance. O2Micro recommends setting it to “0” to get lower noise amplitude on CADC value.
cc_always_enable: (R/W, default = ”0”)
“1”: always enable CADC to perform Coulomb counting. Meanwhile, when a single CADC trigger request is received, will perform CADC trigger and add triggered CADC value to Coulomb counter. After trigger is finished it will automatically perform CADC for Coulomb counting;
“0”: CADC operation depends on sw_cadc_ctrl[1:0].
conse_cadc_rdy_enable: (R/W, default=”0”), when cc_always_enable is set to “1”, CADC is performed continuously. It means there is no time interval between one conversion and the next conversion. In this case, if conse_cadc_rdy_enable is set “1”, no matter hi_acy_mode is set to “0” or “1”, once a CADC conversion is finished, OZ3717 will average the latest 4 CADC values (the average is also called moving average) and then write the averaged value into register 0x39, and meanwhile set conse_cadc_rdy_flag to “1”.
hi_acy_mode: (R/W, default = “0”), “1”: enable the high accuracy mode of CADC, but CADC is slower than setting to “0”. When hi_acy_mode = “0”, the conversion time for a single trigger CADC is about 128ms; When hi_acy_mode = “1”, the conversion time for a single trigger CADC is about 320ms.
sw_cadc_ctrl[1:0]: (R/W, default = ”2’b00”)
“00”: ΣΔ current ADC is disabled;
“01”: Reserved setting;
“10”: single trigger CADC request, automatically cleared to “00” once single trigger CADC is finished, also set cadc_trigger_flag to “1” when single trigger CADC is finished; be careful that the triggered CADC value would not be added to Coulomb counter when cc_always_enable = “0”.
“11”: Reserved setting.</td></tr>
<tr><td>0x31</td><td>Reserved</td><td colspan="15">Reserved</td></tr>
<tr><td>0x32</td><td>CCH (R/W)</td><td colspan="15">coulomb_counter[31:16]</td></tr>
<tr><td>0x33</td><td>CCL (R/W)</td><td colspan="15">coulomb_counter[15:0]</td></tr>
<tr><td>0x34~ 0x37</td><td>Reserved</td><td colspan="15">Reserved</td></tr>
<tr><td>0x38</td><td>CTDATA (RO)</td><td colspan="15">cadc_trigger_data[15:0]: trigger CADC data, signed data (positive means charge, negative means discharge) with LSB=7.8125uV.</td></tr>
<tr><td>0x39</td><td>CMDATA (RO)</td><td colspan="15">conse_cadc_data[15:0]: consecutive CADC data, signed data (positive means charge, negative means discharge) with LSB=7.8125uV. It should be read in 64ms after conse_cadc_rdy_flag is set to “1”.</td></tr>
<tr><td>0x3A~ 0x43</td><td>Reserved</td><td colspan="15">Reserved</td></tr>
<tr><td rowspan="2">0x44</td><td rowspan="2">CXCN (RO)</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="4">which_cell_min[4:0]</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="4">which_cell_max[4:0]</td></tr>
<tr><td colspan="15">Save the number of the cell which has the max/min cell voltage in last ADC scan (Trigger-scan or Auto-scan).
Auto-scan must be disabled before reading this register.</td></tr>
</table>

0x45	MAXCELL (RO)	***max_cell_data[15:0]:*** Save the max cell voltage in last ADC scan (Trigger-scan or Auto-scan). Auto-scan must be disabled before reading this register. Signed data with LSB=0.625mV/4.
0x46	MINCELL (RO)	***min_cell_data[15:0]:*** Save the min cell voltage in last ADC scan (Trigger-scan or Auto-scan). Auto-scan must be disabled before reading this register. Signed data with LSB=0.625mV/4.
0x47~ 0x4E	Reserved	***Reserved***
0x4F	UVSTDN (R/W)	***uv_shutdown_dly[1:0]*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***N/A*** | ***uv_shutdown_th[3:0]***
		uv_shutdown_dly[1:0]: UV shutdown delay scan cycle. "00": 3 cycles; "01": 6 cycles (default); "10": 9 cycles; "11": 12 cycles. ***uv_shutdown_th[3:0]:*** UV shutdown threshold, this function can be disabled by setting ***uv_shutdown_th[3:0]*** = 4'b0000, the range is 1.5V (4'b0001) ~ 2.9V (4'b1111), 100mV/step, default is 4'b0110 for 2.0V.
0x50	OVP (R/W)	***ovp_dly[1:0]*** | ***ovp_rls_hys[5:0]*** | ***ovp_th[7:0]***
		ovp_dly[1:0]: OV delay scan cycle, "00": 2 cycles (default); "01": 4 cycles; "10": 6 cycles; "11": 8 cycles. ***ovp_rls_hys[5:0]:*** (default is 200mV, i.e. 6'b010100 = 20) hysteresis voltage for OV release, the range is 10~630mV, 10mV/step, where OVP is disabled when ovp_rls_hys[5:0] = 6'd0. ***ovp_th[7:0]:*** (default is 4.2V, i.e. 8'b10110100 = 180) threshold for OV protection, the range is 3.3V~4.575V, 5.0mV/step, the base is 3.3V.
0x51	DOC1P (R/W)	***cell_num[2:0]*** | ***efetc_mode[1:0]*** | ***doc1p_dly[2:0]*** | ***doc1p_th[7:0]***
		cell_num[2:0]: (default = 3'b111 for 17 cells), cell number configuration, "000"~"111" for 10 cells ~ 17 cells expectedly. ***efetc_mode:*** (default = 2'b00) "00": only switch off discharge MOSFET with EFETC pin = High; "01": switch off both discharge MOSFET and charge MOSFET with EFETC pin = High; "10": only switch off discharge MOSFET with EFETC pin = Low; "11": switch off both discharge MOSFET and change MOSFET with EFETC pin = Low. ***doc1p_dly[2:0]:*** delay scan cycles for doc1p. "000": 2 cycles; "001": 4 cycles; "010": 6 cycles; "011": 8 cycles; "100": 10 cycles; "101": 12 cycles; "110": 14 cycles; "111": 16 cycles. ***doc1p_th[7:0]:*** threshold for DOC1 protection, the range is 5.0mV~163.75mV (corresponding to the setting from 1 to 255), 0.625mV/step (i.e. 20LSB/step), the base is 5mV. If the setting is 8'h00, it means DOC1 protection is disabled.

<table>
<tr><td rowspan="2">0x52</td><td rowspan="2">COCP
(R/W)</td><td>N/A</td><td>N/A</td><td>vmcu_
wkmd</td><td>wkup_
adc_
option</td><td>type_
cfg</td><td colspan="2">cocp_dly[2:0]</td><td colspan="2">cocp_th[7:0]</td></tr>
<tr><td colspan="8">vmcu_wkmd: (default = “0”), “0”: automatically enable the external LDO when large current on VMCU is detected; “1”: the LDO operation mode follows the setting of sw_vmcu_enable[1:0] in Reg.0x57.
wkup_adc_option: (default = “0”), “0”: no effect; “1”: WKUP pin voltage ADC channel will be selected when VPACK ADC channel is requested, so the WKUP ADC data will share the same register (Reg.0x1A) with the VPACK ADC data register.
type_cfg: “0” for two-terminal application as default (i.e. series), “1” for three-terminal application (i.e. parallel).
cocp_dly[2:0]: (default = 3’b000), delay scan cycles for COC protection,
“000”: 2 cycles; “001”: 4 cycles; “010”: 6 cycles; “011”: 8 cycles; “100”: 10 cycles; “101”: 12 cycles; “110”: 14 cycles; “111”: 16 cycles.
cocp_th[7:0]: (default = 8’h00), when this parameter is set to ”0”, COC protection is disabled; otherwise it selects the COC protection threshold which can be set within the range 2.8125mV~82.1875mV, 0.3125mV/step (i.e. 10LSB/step).</td></tr>
<tr><td rowspan="2">0x53</td><td rowspan="2">DOCSC
(R/W)</td><td colspan="2">scp_th[1:0]</td><td>intrpt_
type</td><td colspan="3">doc2p_dly[4:0]</td><td colspan="2">scp_dly[3:0]</td><td>doc2p_th[3:0]</td></tr>
<tr><td colspan="8">scp_th[1:0]: (default = 2’b00), it selects the SC threshold factor, i.e. the multiple relative to DOC2 protection threshold. “00”: 2X; “01”: 4X; “10”: 6X; “11”: 8X. The setting is directly transmitted to analog comparator.
intrpt_type: “0” for low level interrupt on the INT pin (default); “1”for 100Hz edge interrupt.
doc2p_dly[4:0]: (default = 5’b00000), DOC2 protection delay time, 1ms ~ 32ms, 1ms/step.
scp_dly[3:0]: (default = 4’b0000), SC protection delay time, 62.5us ~ 1000us, 62.5us/step.
doc2p_th[3:0]: (default = 4’b0000), it selects the DOC2 protection threshold which can be set within the range 10mV~160mV, 10mV/step. The setting is directly transmitted to analog comparator, and also used for SC threshold.</td></tr>
<tr><td rowspan="2">0x54</td><td rowspan="2">SPIWDT
(R/W)</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="2">spiwdt_timer[7:0]</td></tr>
<tr><td colspan="10">spiwdt_timer[7:0]: SPI watchdog timer control, default is 8’h00 to disable SPI WDT timer, the time range is 1s~255s with 1s/step. If no SPI communication within this defined time, will generate spiwdt_flag to interrupt, then if no SPI communication within 256ms, will enter standby mode. When SPI communication has occurred, the internal counter is reset to 0 then starts re-counting after each SPI communication finished.</td></tr>
<tr><td rowspan="2">0x55</td><td rowspan="2">IDLETH</td><td colspan="5">dsg_threshold[7:0]</td><td colspan="5">chg_threshold[7:0]</td></tr>
<tr><td colspan="10">dsg_threshold[7:0]: (default = 8’h00), it selects the discharge-state threshold that can be set within the range 0.125mV ~ 8.09375mV, 0.03125mV/step (i.e. 1LSB/step), the base is 0.125mV (4LSB).
chg_threshold[7:0]: (default = 8’h00), it selects the charge-state threshold that can be set within the range 0.125mV ~ 8.09375mV, 0.03125mV/step (i.e. 1LSB/step), the base is 0.125mV (4LSB).</td></tr>
<tr><td rowspan="2">0x56</td><td rowspan="2">UNLOCK
(R/W)</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>unlock_
cfg_
wrt</td></tr>
<tr><td colspan="16">unlock_cfg_wrt: (default = “0”), active high to unlock writing for the configuration registers above, otherwise they can’t be written (i.e. they are protected). To unlock; set unlock_cfg_wrt = “1”, the chip ID 0x7717 has to be written into this register.</td></tr>
</table>

0x57	PWRMD (R/W)	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***unlock_pwrmd_wrt***	***active_mode***	***N/A***	***sw_vmcu_enable[1:0]***	***pwrmd_ctrl[3:0]***				
		unlock_pwrmd_wrt: (R/W, default = "0"), active high to allow this register be written. To make ***unlock_pwrmd_wrt*** = "1", 0x7717 has to be written into this register. It is cleared to 0 when writing other value into this register. ***active_mode:*** (Read only), active high to indicate it is in Active mode, else it is in Standby mode. ***sw_vmcu_enable[1:0]:*** (R/W, default = 2'b10), bit 1 used for internal LDO enable, bit 0 used for external LDO enable, 2'b00 is not allowed (i.e. writing 2'b00 will change nothing). ***pwrmd_ctrl[3:0]:*** (RW, default = 4'b0011) 4'b0011: Standby mode; 4'b0101: Active mode; 4'b1010: Shutdown mode; The other value is not allowed to be written (i.e. power mode will not changed if other value is written).															
0x58	AUTOSCAN (R/W)	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***sw_mapping_req***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***auto_scan_save_allow***	***auto_one_or_eight***	***auto_scan***
		sw_mapping_req: (default = "0"), write "1" to this bit to request mapping from e-memory into internal registers, Cleared to "0" automatically after mapping is finished. ***auto_scan_save_allow:*** (default = "0"), set to "1" to allow saving ADC data in registers in Auto-scan. When Auto-scan is enabled, this bit can be used to select whether the ADC values (SAR current ADC and cell 17 - 1) during Auto-scan are stored in the corresponding registers (0x01 – 0x12) or not. ***auto_one_or_eight:*** (default = "0"), "0" for one time ADC in Auto-scan; "1" for eight times ADC in Auto-scan. ***auto_scan:*** (default = "0"), "0": disable Auto-scan, "1": enable Auto-scan with scan rate = 250ms in Active mode.															
0x59	FETCTRL (R/W)	***N/A***	***pre_set[6:0]***						***sw_load_detec_enable***	***sw_chgr_detect_enable***	***N/A***	***N/A***	***pre_sel[1:0]***		***sw_chg_ctrl***	***sw_dsg_ctrl***	
		pre_set[6:0]: (R/W, default = 7'b0000000), to set current value for pre-charge or pre-discharge; ***sw_load_detect_enable:*** (R/W, default = "0"), active high to allow load-on/load-off detection during discharge FET OFF. ***sw_chgr_detect_enable:*** (R/W, default = "0"), active high to allow charger-in detection during charge FET OFF. ***pre_sel[1:0]:*** (R/W, default = 2'b00), "01": to select pre-charge, "10": to select pre-discharge, others: pre-charge and pre-discharge are both disabled. ***sw_chg_ctrl***: (R/W, default = "0") write "0" into this bit to switch off high side charge MOSFET. ***sw_dsg_ctrl:*** (R/W, default = "0") write "0" into this bit to switch off high side discharge MOSFET.															

<table>
<tr><td rowspan="2">0x5A</td><td rowspan="2">CRRTSEL
(R/W)</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>sw_vref_enable</td><td>N/A</td><td>N/A</td><td>thm_crrt_sel[1:0]</td></tr>
<tr><td colspan="15">sw_vref_enable: (R/W, default = 1’b0), in order to save power, this bit can be set to “0” to disable the reference for ADC. Active high to enable the reference for ADC. After the reference is enabled, a delay of more than 2ms should be inserted before doing ADC.
thm_crrt_sel[1:0]: (default = 2’b00) constant current selection for THM0~THM2 measurement, “01”: select 20uA; “10”: select 120uA; the others settings do not select any current. Normally 20uA is selected for low temperature; 120uA is selected for high temperature, fully controlled by Microcontroller.</td></tr>
<tr><td rowspan="2">0x5B</td><td rowspan="2">CBSEL1
(R/W)</td><td>Iotp_state</td><td>ovp_event</td><td>In_chg_state</td><td>In_dsg_state</td><td>pre_chg</td><td>pre_dsg</td><td>chg_drv</td><td>dsg_drv</td><td>ohtp_state</td><td>cp_ok</td><td>efetc_dig</td><td>loadoff_valid</td><td>loadon_valid</td><td>chgrin_valid</td><td>indsg_dig</td><td>cell_bal_sel[16]</td></tr>
<tr><td colspan="16">iotp_state: (read only) active high to indicate CBOT event occurred.
ovp_event: (read only) active high to indicate OV event occurred.
in_chg_state: (read only) active high to indicate charge current is detected by ADC;
in_dsg_state: (read only) active high to indicate discharge current is detected by ADC, or detected by the analog comparator.
pre_chg: (read only) read back to check pre-charge is enabled or not.
pre_dsg: (read only) read back to check pre-discharge is enabled or not.
chg_drv: (read only) read back the charge MOSFET driving signal.
dsg_drv : (read only) read back the discharge MOSFET driving signal.
ohtp_state: (read only) active high to indicate Thermal Standby protection occurred (for test or debug).
cp_ok: (read only) active high to indicate charge pump is OK when enabled (for test or debug).
efetc_dig: (read only) input High/Low from pin EFETC.
loadoff_valid: (read only), active high to indicate load OFF during discharge FET OFF when load detection is allowed.
loadon_valid: (read only), active high to indicate load ON during discharge FET OFF when load detection is allowed.
chgrin_valid, indsg_dig: (read only) read back for confirmation, chgrin_valid is similar to chgrin_flag, but the difference is that the chgrin_flag needs to be cleared by external host, but chgrin_valid is determined only by the Charge-in/out detection block of OZ3717; indsg_dig is similar to indsg_flag, but the difference is that the indsg_flag needs to be cleared by external host, but indsg_dig is determined only by the discharge current detection block (analog comparator) of OZ3717.
cell_bal_sel[16]: (default = “0”), active high to do cell17 balance.</td></tr>
<tr><td rowspan="2">0x5C</td><td rowspan="2">CBSEL2</td><td colspan="16">cell_bal_sel[15:0]</td></tr>
<tr><td colspan="16">Default = 16’h0000. Active high to do cell01~cell16 balance respectively,
cell_bal_sel[0] → cell01, cell_bal_sel[1] → cell02, …, cell_bal_sel[15] → cell16.

Note: adjacent cell balance configuration is forbidden.</td></tr>
</table>

0x5D	IE (R/W)	***cadc_trigger_ie***	***cc_overflow_ie***	***N/A***	***N/A***	***iotp_ie***	***cb_timeout_ie***	***loadoff_ie***	***loadon_ie***	***chgrin_ie***	***spiwdt_ie***	***trigger_scan_ie***	***ovp_ie***	***cocp_ie***	***doc1p_ie***	***doc2p_ie***	***scp_ie***
		Interrupt enable. Default = "1" to enable. ***cadc_trigger_ie***: active high to enable single trigger ∑Δ current ADC interrupt; ***cc_overflow_ie***: active high to enable Coulomb Counting overflow/underflow interrupt; ***iotp_ie***: active high to enable Internal OT interrupt; ***cb_timeout_ie***: active high to enable cell balance timeout interrupt; ***loadoff_ie***: active high to enable load off interrupt; ***loadon_ie***: active high to enable load on interrupt; ***chgrin_ie***: active high to enable charger in interrupt; ***spiwdt_ie***: active high to enable SPI Watchdog timer overflow interrupt; ***trigger_scan_ie***: active high to enable trigger scan interrupt when trigger scan is finished; ***ovp_ie***: active high to enable OV interrupt; ***cocp_ie***: active high to enable COC interrupt; ***doc1p_ie***: active high to enable DOC1 interrupt; ***doc2p_ie***: active high to enable DOC2 interrupt; ***scp_ie***: active high to enable SC interrupt.														

0x5E	STATUS (R/C)	***cadc_ trigger_ flag***	***cc_ overflow _flag***	***spi_ crc_err_ flag***	***porn_ flag***	***iotp_ flag***	***cb_ timeout_ flag***	***loadoff_ flag***	***loadon_ flag***	***chgrin_ flag***	***spiwdt_ flag***	***trigger_ scan_ flag***	***ovp_ flag***	***cocp_ flag***	***doc1_ flag***	***doc2_ flag***	***scp_ flag***

Status register.

cadc_trigger_flag: (R/C), set to 1 when single trigger ∑Δ current ADC is finished, clear to 0 by writing 1 to this bit;
cc_overflow_flag: (R/C), set to 1 when coulomb counting overflow/underflow, clear to 0 by writing 1 to this bit.
spi_crc_err_flag: (R/C), set to 1 when SPI CRC error occurred during writing, clear to 0 by writing 1 to this bit, but this flag doesn't involve the interrupt.
porn_flag: (R/C), set to 1 when power on reset occurred (unmasked interrupt), clear to 0 by writing 1 to this bit;
iotp_flag: (R/C), set to 1 when internal OT occurred, clear to 0 by writing 1 to this bit;
cb_timeout_flag: (R/C), set to 1 when cell balance timeout, clear to 0 by writing 1 to this bit;
loadoff_flag: (R/C), set to 1 when load off is detected during discharge MOSFET is OFF, clear to 0 by writing 1 to this bit;
loadon_flag: (R/C), set to 1 when load on is detected during discharge MOSFET is OFF, clear to 0 by writing 1 to this bit;
chgrin_flag: (R/C), set to 1 when charger-in is detected during charge MOSFET is OFF, clear to 0 by writing 1 to this bit;
spiwdt_flag: (R/C), set to 1 when SPI watchdog occurred, clear to 0 by writing 1 to this bit;
trigger_scan_flag: (R/C), set to 1 when trigger scan finished, clear to 0 by writing 1 to this bit;
ovp_flag: (R/C), set to 1 when OV occurred, clear to 0 by writing 1 to this bit;
cocp_flag: (R/C), set to 1 when COC occurred, clear to 0 by writing 1 to this bit;
doc1p_flag: (R/C), set to 1 when DOC1 occurred, clear to 0 by writing 1 to this bit;
doc2p_flag: (R/C), set to 1 when DOC2 occurred, clear to 0 by writing 1 to this bit;
scp_flag: (R/C), set to 1 when SC occurred, clear to 0 by writing 1 to this bit.

<table>
<tr><td rowspan="2">0x5F</td><td rowspan="2">TRIG
(R/W)</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>trigger_scan_req</td><td>trigger_one_or_eight</td><td>cto_detection</td><td>trigger_scan_channel[4:0]</td></tr>
<tr><td colspan="13">trigger_scan_req: write “1” into this bit to request one time of ADC scan, the channel(s) to be scanned is defined in trigger_scan_channel[4:0]. When this requested ADC is completed, this bit is cleared automatically, meanwhile trigger_scan_flag is set to “1”.
trigger_one_or_eight: (default = “0”), “0” for one ADC measurement cycle time; “1” for eight ADC cycle times.

cto_detection: (default = “0”), active high to enable Cell-Tap-Open detection, which means the cell balance will be forced ON when performing a cell ADC trigger scan, otherwise cell balance will be forced OFF for trigger scan and Auto-scan even if the cell balance is ON by cell_bal_sel[16:0].

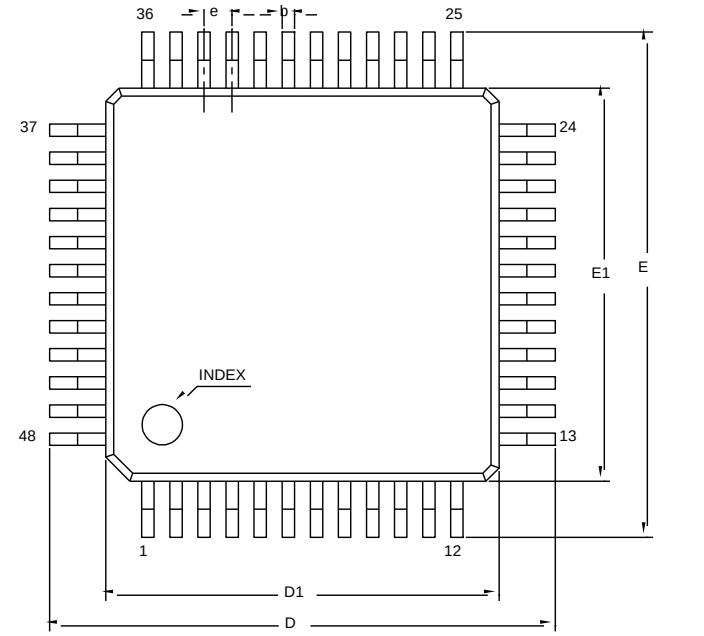
trigger_scan_channel[4:0]: (default = 5’b00000)
0x00: do nothing;
0x01~0x11: for CELL01 ~ CELL17 respectively;
0x12: for current channel;
0x13~0x15: for THM0 ~ THM2 respectively;
0x16,0x17: Reserved;
0x18: for internal temperature channel;
0x19: for VAUX channel;
0x1A: for VPACK channel;
0x1B: for VBAT channel;
0x1C: for V50V channel;
0x1D: for VMCU channel;
0x1E: for safety scan including all cell channels and current channel;
0x1F: for all channels including 0x01~0x1D channels.</td></tr>
<tr><td rowspan="2">0x60</td><td rowspan="2">IER2</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>conse_cadc_rdy_ie</td><td>uv_ie</td><td>indsg_ie</td></tr>
<tr><td colspan="15">conse_cadc_rdy_ie: (R/W), (default = “1”), interrupt enable, active high.
uv_ie: (R/W), (default = “1”) interrupt enable, active high.
indsg_ie: (R/W), (default = “1 “), interrupt enable, active high.</td></tr>
</table>

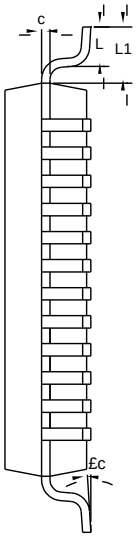
0x61	STR2	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***N/A***	***conse_cadc_rdy_flag***	***uv_flag***	***indsg_flag***
		conse_cadc_rdy_flag: (R/C), set to "1" when consecutive CADC is finished, clear to "0" by writing "1" to this bit. ***uv_flag:*** (R/C), set to "1" once UV is detected (consecutive 2 scan cycles) to provide interrupt to Microcontroller in advance because of UV shutdown function, clear to "0" by writing "1" to this bit. ***indsg_flag:*** (R/C), set to "1" once in-discharge current (by analog comparator) is confirmed with 32us filter, clear to "0" by writing "1" to this bit.															
0x62~ 0x6F	Reserved	***Reserved***															
0x70	Reserved	***Reserved***															
0x71	Reserved	***Reserved***															
0x72~ 0x7F	Reserved	***Reserved***															
0x80~ 0x8F	Reserved	***Reserved***															
0x90~ 0x9F	Reserved	***Reserved***															
0xA0~ 0xFF	Reserved	***Reserved***															

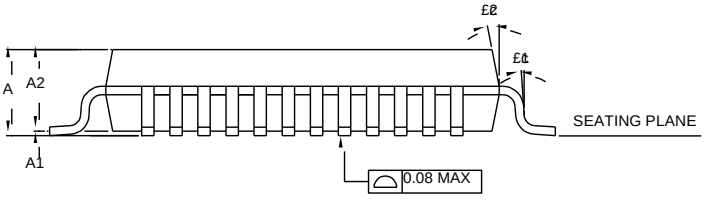
Note: N/A *read as "0" and the writing operation to the reserved bits must be prohibited.*

PACKAGE INFORMATION

48L LQFP 7x7mm Package Outline Drawing







SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	-	0.75
L1	1.00 REF		
01	0°	-	7°
02	0°	-	-
03	12°TYP		

NOTE:
1. REFER TO JEDEC STD MS-026 BBC

Figure 52: LQFP 48 Package Outline Drawing

APPENDIX A: RECOMMENDED COMPONENT'S RANGE

Designator	Description	Min	Typical	Max	Unit	Manufacturer
CF0,CF1~CF8	CAP, CERM, 50V, +/-10%, XR7, 0603	0.1		0.47	µF	TDK
CF9, CF10 ~CF17	CAP, CERM, 100V, +/-10%, XR7, 0603	0.1		0.47	µF	YAGEO
C1,C2	CAP, CERM, 100V, +/-10%, XR7, 1210		2.2		µF	AVX
C3, C4, C5	CAP, CERM, 16V, +/-10%, XR7, 0603		0.1		µF	YAGEO
C6	CAP, CERM, 25V, +/-10%, XR7, 0603	4.7	10	22	nF	YAGEO
C7,C14	CAP, CERM, 16V, +/-10%, XR7, 0603	2.2	4.7	10	µF	FH
C8,C9,C10	CAP, CERM, 25V, +/-10%, XR7, 0603	470		1000	pF	MuRata
C13	CAP, CERM, 16V, +/-10%, XR7, 0603		1		µF	YAGEO
C15	CAP, CERM, 50V, +/-10%, XR7, 0603	4.7	10	22	nF	YAGEO
C16	CAP, CERM, 50V, +/-10%, XR7, 0603	4.7		10	nF	MuRata
C17	CAP, CERM, 100V, +/-10%, XR7, 0603	1		4.7	nF	YAGEO
C18	CAP, CERM, 100V, +/-10%, XR7, 0603	4.7	10	22	nF	MuRata
C19	CAP, CERM, 50V, +/-10%, XR7, 0603	***Note 1***			µF	FH
C20,C21	CAP, CERM, 100V, +/-10%, XR7, 0603	0.047	0.1	0.22	µF	YAGEO
C22	CAP, CERM, 100V, +/-10%, XR7, 0603		0.1		µF	YAGEO
C23	CAP, CERM, 100V, +/-10%, XR7, 1210		2.2		µF	AVX
C24,C25	CAP, CERM, 100V, +/-10%, XR7, 0805		0.1		µF	SAMSUNG
CON4	Pin-Header 1X5, 2mm					BOOMELE
D1,D5,D23,D24	Diode, Schottky, BAT46W, 100V, 0.15A, SOD-123		100V			DIODES
D3,D8	Diode, TVS, SMBJ78A, 78V, 4.7A, DO-214AA		78V			DIODES
D4	Diode, Zener, KDZTR5.6B, 5.6V, 1W, SOD-123		5.6V			ROHM

Designator	Description	Min	Typical	Max	Unit	Manufacturer
D6,D7	Diode, Zener, DDZ9702-7, 15V, 0.5W, SOD-123		15V			DIODES
D9	Diode, TVS, SMBJ78A, 78V, 4.7A, DO-214AA		78V/NC			DIODES
D18 ~ D21	Diode, ESD, PESD5V0S1BA, 5V, 5A, SOD-323		5V			YENJI
D22	Diode, Ultrafast, ES3D, 200V, 3A, SMC		200V			Vishay
D100, D101~D117	Diode, Schottky, BAT46W, 100V, 0.15A, SOD-123		100V/NC			DIODES
J1	Pin-Header 3X1, 2mm					BOOMELE
LED18	LED, Red, 0603, SMD		Red			EVERLIGHT
M1	MOSFET, N-CH, 100V, AM2370N, 1.3A, SOT-23		100V			Analog Power
Q18,Q19	MOSFET, N-CH, 100V, AM90N10, 90A, TO-263		100V			Analog Power
Q20	TRANS, MMBT3904, 40V, 0.2A, NPN, SOT-23		40V			DIODES
RF0, RF1~RF17	RES, +/-1%, 1/4W, 0805	120		330	Ω	YAGEO
RSENS1,RSENS2	RES, +/-1%, 2W, 2512		0.005		Ω	YAGEO
RT1, RT2, RT3	RES, NTC, 103AT-4, +/-1%, B Value 3435K		10		KΩ	SEMITEC
R18	RES, +/-5%, 1W, 1210		51		Ω	YAGEO
R20,R21	RES, +/-1%, 1/8W, 0603		100		Ω	YAGEO
R22	RES, +/-5%, 1/8W, 0603		1		KΩ	YAGEO
R23	RES, +/-5%, 1/8W, 0603		2		KΩ	YAGEO
R24	RES, +/-5%, 1/8W, 0603		10		KΩ	YAGEO
R25	RES, +/-5%, 1/8W, 0603	51	100	200	Ω	YAGEO
R26	RES, +/-5%, 1/8W, 0603	100		220	KΩ	YAGEO
R28	RES, +/-5%, 1/8W, 0603	330	390	470	KΩ	YAGEO
R29	RES, +/-5%, 1/4W, 0805	10	100	200	KΩ	YAGEO

Designator	Description	Min	Typical	Max	Unit	Manufacturer
R30,R31,R32,R33, R35	RES, +/-5%, 1/4W, 0805	51	100	220	Ω	YAGEO
R34,R36	RES, +/-5%, 1/8W, 0603	4.7		10	MΩ	YAGEO
R41, R42, R43, R44	RES, +/-5%, 1/8W, 0603		100		Ω	YAGEO
R49, R50	RES, +/-5%, 1/4W, 0805		0		Ω	YAGEO
R51	RES, +/-1%, 1/4W, 0805	***Note 2***			Ω	YAGEO
PACK-, PACK+, BAT-, BAT+	PCB - PAD					
U1	Digital Front End (DFE) IC for 10 to 17 LiIon Cells with high side drivers for N-FETs - LQFP48		OZ3717			**O2MICRO**
C26 *****	CAP, CERM, 100V, +/-10%, XR7, 0603		0.1		μF	YAGEO
D10 *****	Diode, Ultrafast, 1N4148W, 100V, 0.15A, SOD-123		100V			DIODES
R37 *****	RES, +/-5%, 1/8W, 0603	1	2	3.3	MΩ	YAGEO
Q21 *****	TRANS, MMBT5401L, -150V, 0.2A, PNP, SOT-23		-150			ON

*******: these parts are used for 3-terminal application.*

Note 1*: please refer to the "FET Driver & Control" section for the details.*

Note 2: *please select this part based on the demanded current. Generally, R51=~(0.66V/ I_{MCU}) Ω .*

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