FAIRCHILD SEMICONDUCTOR®

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74LVT373, 74LVTH373
Low Voltage Octal Transparent Latch with 3-STATE Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH373), also available without bushold feature (74LVT373)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Functionally compatible with the 74 series 373
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

General Description

The LVT373 and LVTH373 consist of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in a high impedance state.

The LVTH373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 and LVTH373 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

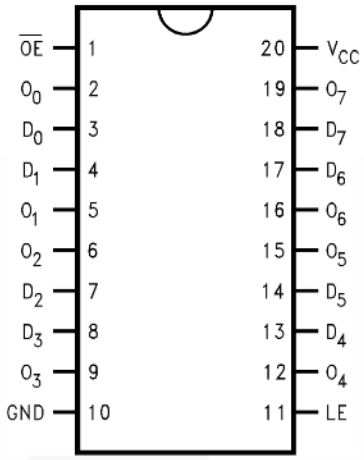
Ordering Information

Order Number	Package Number	Package Description
74LVT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

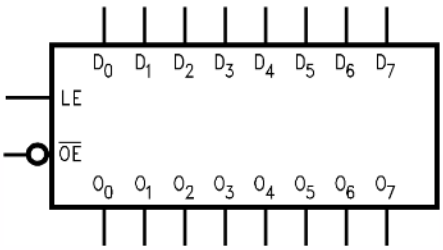
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

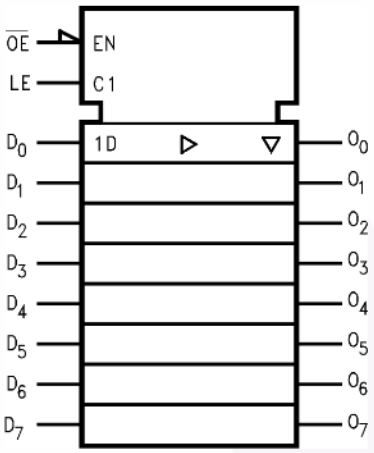
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Description

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Latch Outputs

Functional Description

The LVT373 and LVTH373 contain eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level

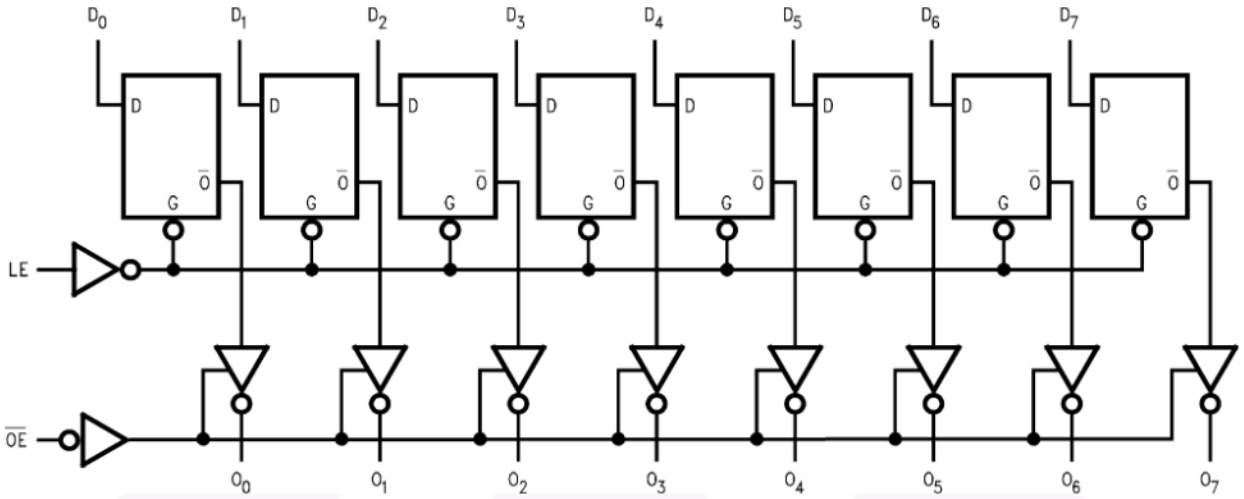
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(1)	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current, V_O < GND	–50mA
I_O	DC Output Current, $V_O > V_{CC}$	
	Output at HIGH State	64mA
	Output at LOW State	128mA
I_{CC}	DC Supply Current per Supply Pin	±64mA
I_{GND}	DC Ground Current per Ground Pin	±128mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		–32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C			Units
				Min.	Typ.(2)	Max.	
V_{IK}	Input Clamp Diode Voltage	2.7	I_I = –18mA			–1.2	V
V_{IH}	Input HIGH Voltage	2.7–3.6	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$	2.0			V
V_{IL}	Input LOW Voltage	2.7–3.6				0.8	V
V_{OH}	Output HIGH Voltage	2.7–3.6	I_{OH} = –100µA	V_{CC}–0.2			V
		2.7	I_{OH} = –8mA	2.4			
		3.0	I_{OH} = –32mA	2.0			
V_{OL}	Output LOW Voltage	2.7	I_{OL} = 100µA			0.2	V
			I_{OL} = 24mA			0.5	
		3.0	I_{OL} = 16mA			0.4	
			I_{OL} = 32mA			0.5	
			I_{OL} = 64mA			0.55	
$I_{I(HOLD)}$(3)	Bushold Input Minimum Drive	3.0	V_I = 0.8V	75			µA
			V_I = 2.0V	–75			
$I_{I(OD)}$(3)	Bushold Input Over-Drive Current to Change State	3.0	(4)	500			µA
			(5)	–500			
I_I	Input Current	3.6	V_I = 5.5V			10	µA
	Control Pins	3.6	V_I = 0V or V_{CC}			±1	
	Data Pins	3.6	V_I = 0V			–5	
			V_I = V_{CC}			1	
I_{OFF}	Power Off Leakage Current	0	$0V \le V_I$ or $V_O \le 5.5V$			±100	µA
$I_{PU/PD}$	Power up/down 3-STATE Output Current	0–1.5V	V_O = 0.5V to 3.0V, V_I = GND or V_{CC}			±100	µA
I_{OZL}	3-STATE Output Leakage Current	3.6	V_O = 0.5V			–5	µA
I_{OZH}	3-STATE Output Leakage Current	3.6	V_O = 3.0V			5	µA
I_{OZH}+	3-STATE Output Leakage Current	3.6	$V_{CC} < V_O \le 5.5V$			10	µA
I_{CCH}	Power Supply Current	3.6	Outputs HIGH			0.19	mA
I_{CCL}	Power Supply Current	3.6	Outputs LOW			5	mA
I_{CCZ}	Power Supply Current	3.6	Outputs Disabled			0.19	mA
I_{CCZ}+	Power Supply Current	3.6	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled			0.19	mA
ΔI_{CC}	Increase in Power Supply Current(6)	3.6	One Input at V_{CC} – 0.6V, Other Inputs at V_{CC} or GND			0.2	mA

Notes:

2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Applies to bushold versions only (74LVTH373).
4. An external driver must source at least the specified current to switch from LOW-to-HIGH.
5. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
6. This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics[7]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$			Units
			$C_L = 50pF$, $R_L = 500\Omega$	Min.	Typ.	Max.	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	[8]		0.8		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	[8]		–0.8		V

Notes:

7. Characterized in SOIC package. Guaranteed parameter, but not tested.

8. Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = –40°C$ to $+85°C$, $C_L = 50pF$, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min.	Typ.[9]	Max.	Min.	Max.	
t_{PHL}	Propagation Delay, D_n to O_n	1.5		4.5	1.5	5.0	ns
t_{PLH}		1.5		4.5	1.5	4.9	
t_{PHL}	Propagation Delay, LE to O_n	1.7		4.6	1.7	4.9	ns
t_{PLH}		1.7		4.5	1.7	5.0	
t_{PZL}	Output Enable Time	1.3		4.8	1.3	5.9	ns
t_{PZH}		1.3		4.8	1.3	5.5	
t_{PLZ}	Output Disable Time	1.9		4.6	1.9	4.9	ns
t_{PHZ}		1.9		4.6	1.9	4.9	
t_W	LE Pulse Width	3.0			3.0		ns
t_S	Setup Time, D_n to LE	1.1			1.0		ns
t_H	Hold Time, D_n to LE	1.4			1.4		ns

Note:

9. All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Capacitance[10]

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN, $V_I = 0V$ or V_{CC}	3	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	5	pF

Note:

10. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

Physical Dimensions

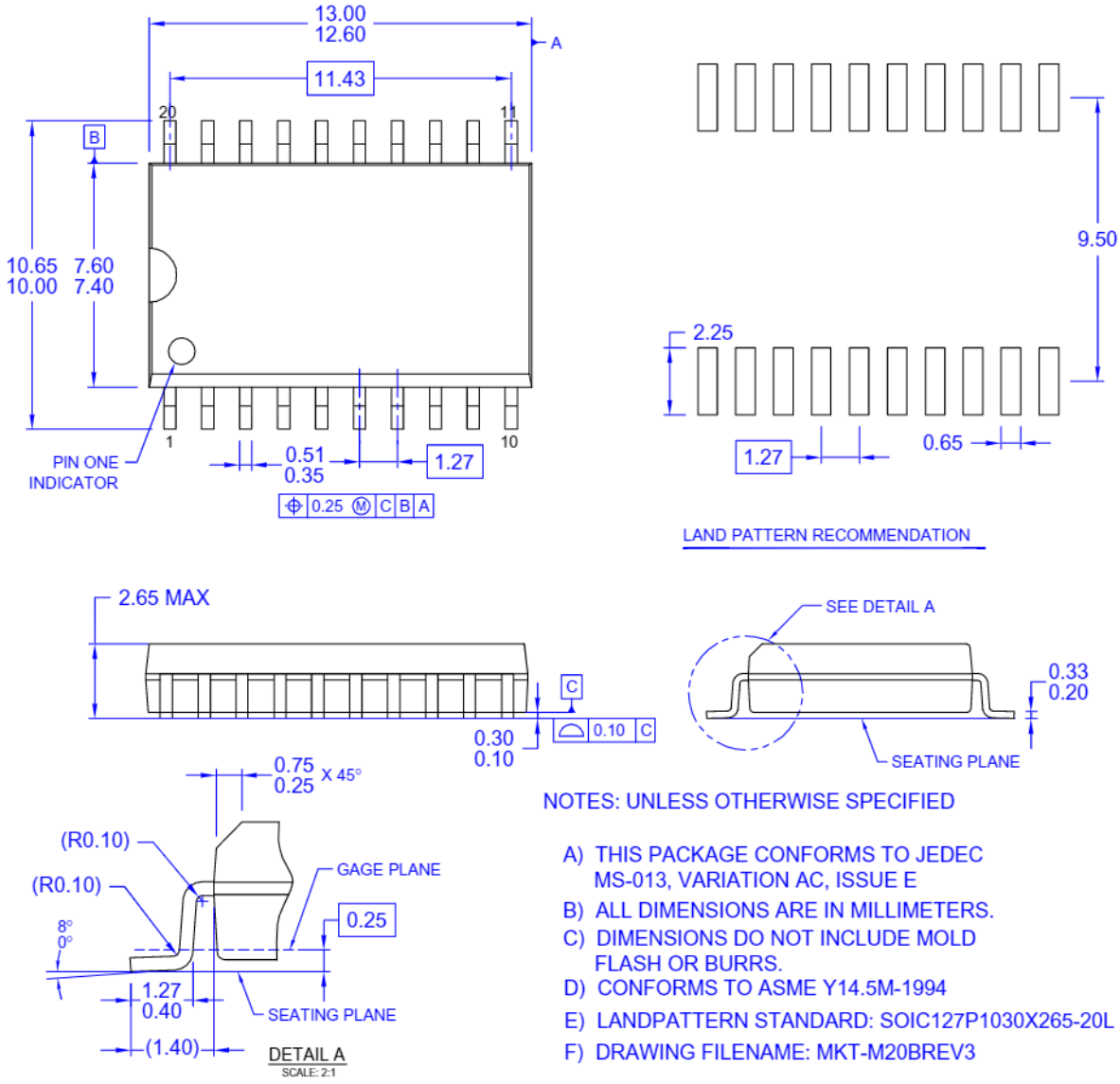


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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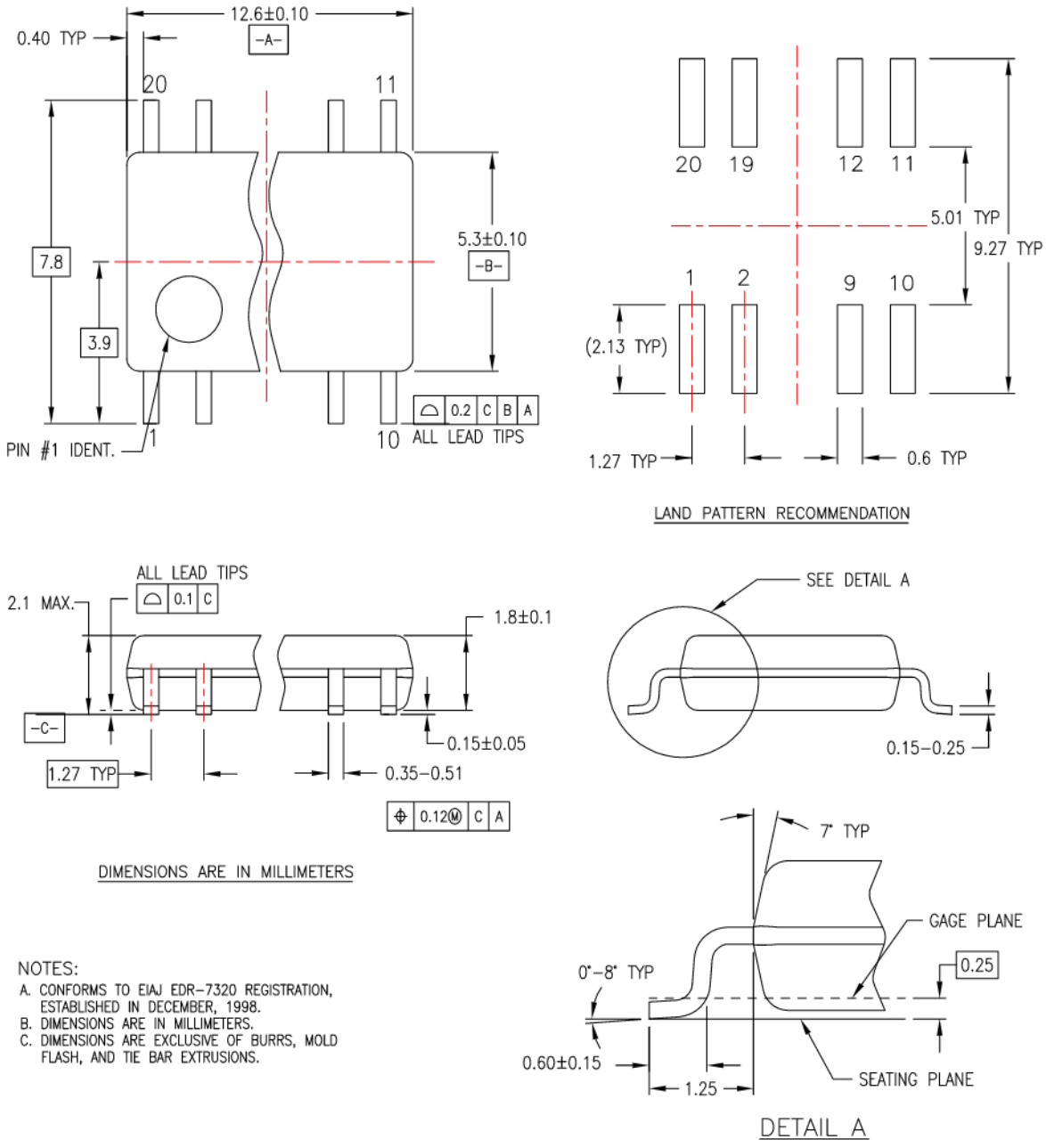
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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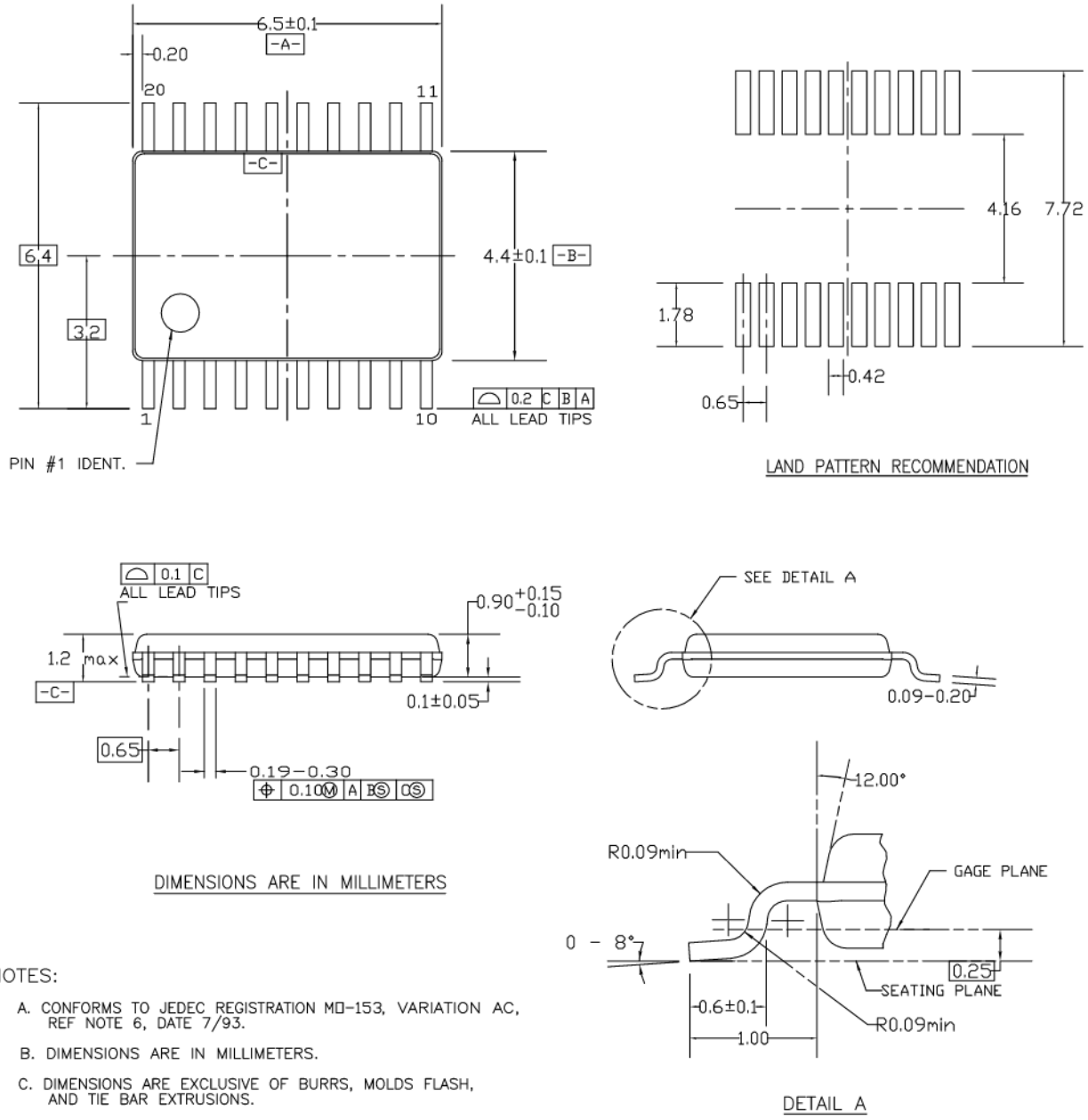
Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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