

## 3.3 V ECL 2:8 Differential Fanout Buffer

### MC100LVE310

#### Description

The MC100LVE310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE310, as with most ECL devices, can be operated from a positive  $V_{CC}$  supply in LVPECL mode. This allows the LVE310 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE310's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of  $V_{CC} - 2.0$  V will need to be provided. For more information on using PECL, designers should refer to Application Note [AN1406/D](#).

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

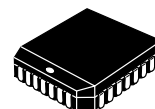
#### Features

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range:  
 $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  
 $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Q Output will Default LOW with All Inputs Open or at  $V_{EE}$
- The 100 Series Contains Temperature Compensation
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



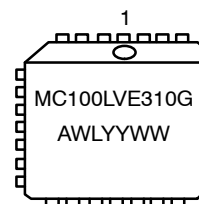
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



PLCC-28  
FN SUFFIX  
CASE 776

#### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

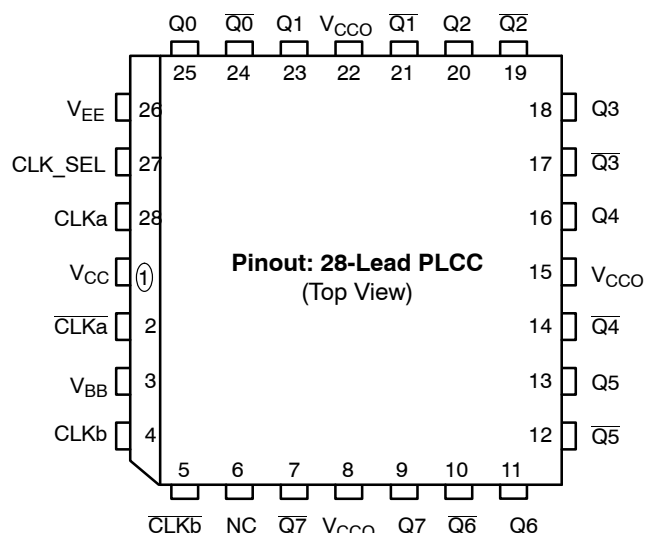
\*For additional marking information, refer to Application Note [AND8002/D](#).

#### ORDERING INFORMATION

Device	Package	Shipping†
MC100LVE310FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

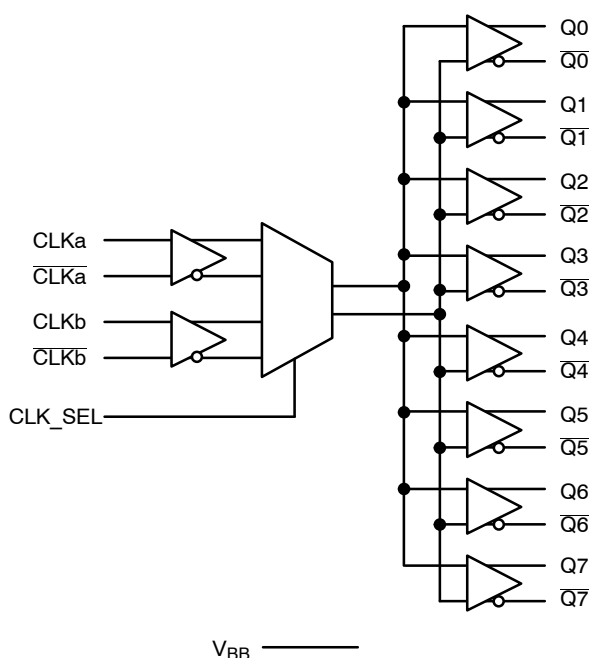
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LVE310



Warning: All V<sub>CC</sub>, V<sub>CCO</sub>, and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout Assignment**



**Figure 2. Logic Symbol**

**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
CLKa, $\overline{\text{CLKa}}$ , CLKb, $\overline{\text{CLKb}}$	ECL Differential Input Clocks
Q0:7, $\overline{\text{Q0:7}}$	ECL Differential Outputs
CLK_SEL	ECL Input Clock Select
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub> , V <sub>CCO</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect

**Table 2. TRUTH TABLE**

CLK_SEL	Input Clock
L	CLKa Selected
H	CLKb Selected

**Table 3. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	YES
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) PLCC-28	Pb-Free Pkg Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	212 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

# MC100LVE310

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26 $\pm 5\%$	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder (Pb-Free)			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 $^{\circ}\text{C}$			25 $^{\circ}\text{C}$			85 $^{\circ}\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		55	60		55	60		65	70	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{BB}$	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	1.8		2.9	1.8		2.9	1.8		2.9	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .  $V_{IHCMR}$  is defined as the range within which the  $V_{IH}$  level may vary, with the device still meeting the propagation delay specification. The  $V_{IL}$  level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to  $V_{PP}(\text{min})$ .

# MC100LVE310

**Table 6. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		55	60		55	60		65	70	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-1.5		-0.4	-1.5		-0.4	-1.5		-0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .  $V_{IHCMR}$  is defined as the range within which the  $V_{IH}$  level may vary, with the device still meeting the propagation delay specification. The  $V_{IL}$  level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to  $V_{PP}(\text{min})$ .

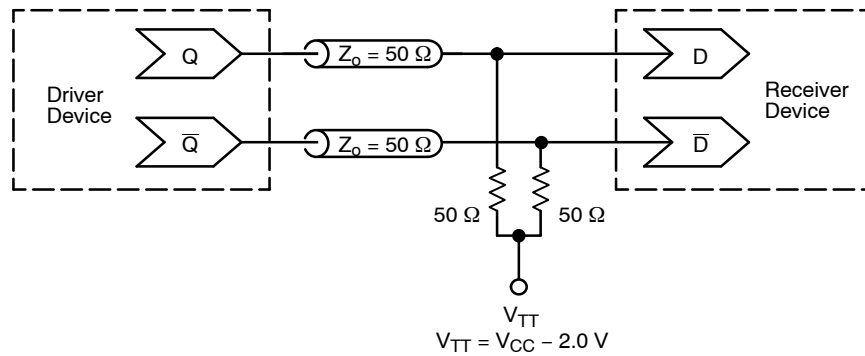
**Table 7. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{max}}$	Maximum Toggle Frequency @ $V_{\text{out}} > 500\text{ mV}_{\text{pp}}$	0.5	1.0		0.5	1.0		0.5	1.0		GHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay to Output IN (Differential Configuration) (Note 2) IN (Single-Ended) (Note 3)	525 500		725 750	550 550		750 800	575 600		775 850	ps
$t_{\text{skew}}$	Within-Device Skew (Note 4) Part-to-Part Skew (Differential Configuration)			75 250			50 200			50 200	ps
$t_{\text{JITTER}}$	Additive CLOCK Jitter (RMS) < 0.5 GHz		1.5	2.0		1.5	2.0		1.5	2.0	ps
$V_{\text{PP}}$	Input Swing (Note 5)	500		1000	500		1000	500		1000	mV
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5.  $V_{\text{PP}}(\text{min})$  is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The  $V_{\text{PP}}(\text{min})$  is AC limited for the LVE310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

## MC100LVE310



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

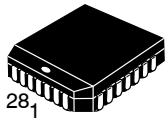
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

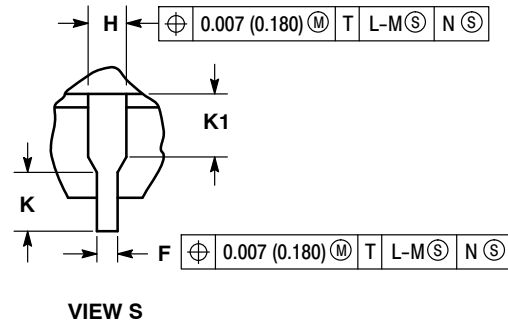
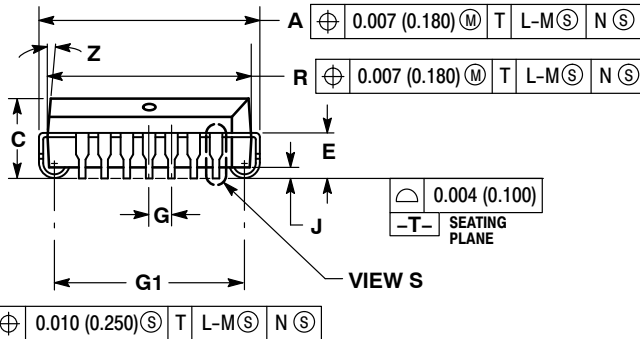
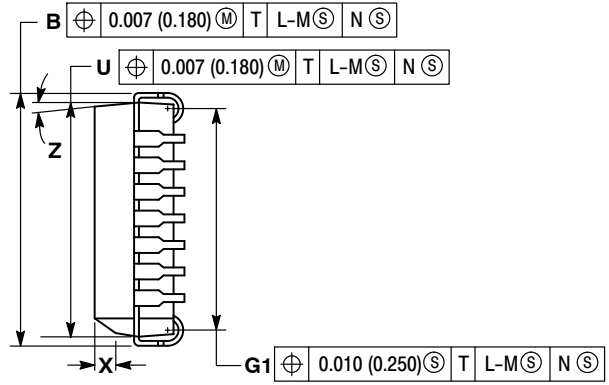
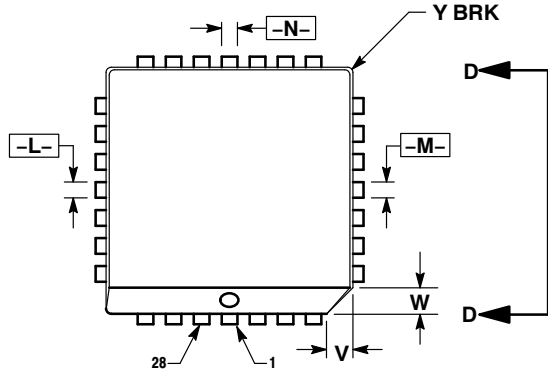
ON Semiconductor®



SCALE 1:1

28 LEAD PLCC  
CASE 776-02  
ISSUE G

DATE 06 APR 2021

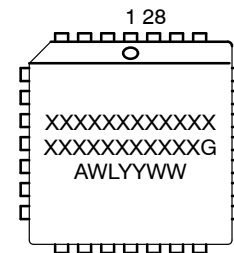


NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER:	98ASB42596B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	28 LEAD PLCC	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

### Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative