

MOSFET - Single N-Channel

100 V, 9.0 mΩ, 60 A

NTBS9D0N10MC

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	100	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State $T_C = 25^\circ\text{C}$	I_D	60	A
Power Dissipation $R_{\theta JC}$ (Note 2)		P_D	68	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State $T_A = 25^\circ\text{C}$	I_D	14	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		P_D	3.8	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 100 \mu\text{s}$	I_{DM}	239	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		I_S	57	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 11 \text{ A}_{pk}, L = 3 \text{ mH}$)		E_{AS}	181.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

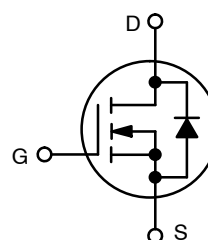
1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



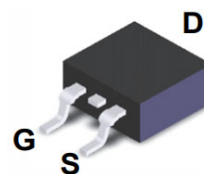
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	9.0 mΩ @ 10 V	60 A



N-CHANNEL MOSFET



**D²PAK3
TO-263
CASE 418AJ**

MARKING DIAGRAM

AYWWZZ NTBS9D0 N10MC

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability
NTBS9D0N10MC = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBS9D0N10MC	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	2.2	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, referenced to 25°C		56		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 150^\circ\text{C}$		100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 131\ \mu\text{A}$	2.0	3.0	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 131\ \mu\text{A}$, referenced to 25°C		-9.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$		7.8	9.0	m Ω
		$V_{GS} = 6\text{ V}, I_D = 12\text{ A}$		12	22.2	
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 23\text{ A}$		59		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		0.6		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		1695		pF
Output Capacitance	C_{OSS}			935		
Reverse Transfer Capacitance	C_{RSS}			13		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 23\text{ A}$		23		nC
Threshold Gate Charge	$Q_{G(TH)}$			5		
Gate-to-Source Charge	Q_{GS}			8		
Gate-to-Drain Charge	Q_{GD}			5		
Output Charge	Q_{OSS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		59		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 23\text{ A}, R_G = 6\ \Omega$		15		ns
Rise Time	t_r			6		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 25^\circ\text{C}$		0.87	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 150^\circ\text{C}$		0.72		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 300\text{ A}/\mu\text{s}, I_S = 12\text{ A}$		29		ns
Reverse Recovery Charge	Q_{RR}			61		nC
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 12\text{ A}$		23		ns
Reverse Recovery Charge	Q_{RR}			147		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperature

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TYPICAL CHARACTERISTICS

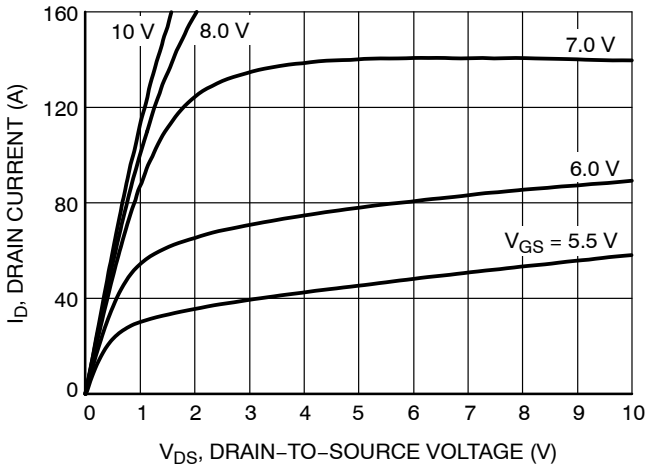


Figure 1. On-Region Characteristics

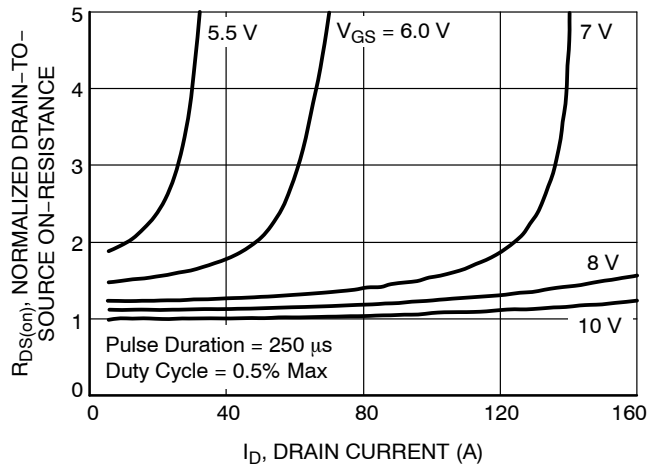


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

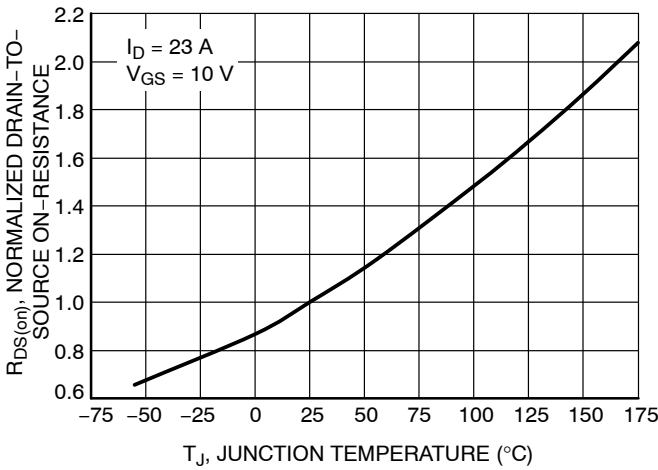


Figure 3. Normalized On-Resistance vs. Junction Temperature

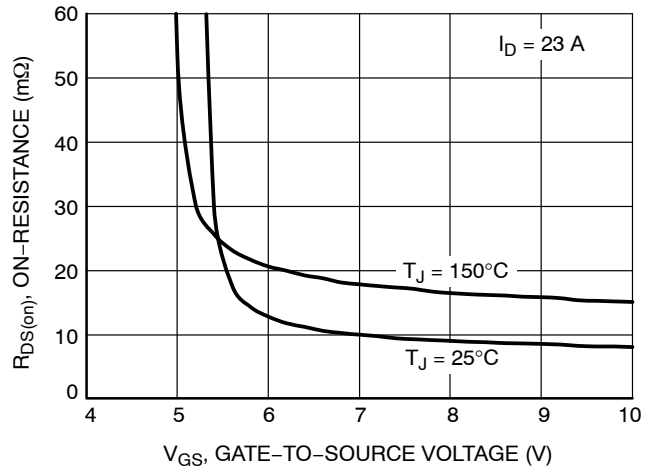


Figure 4. On-Resistance vs. Gate-to-Source Voltage

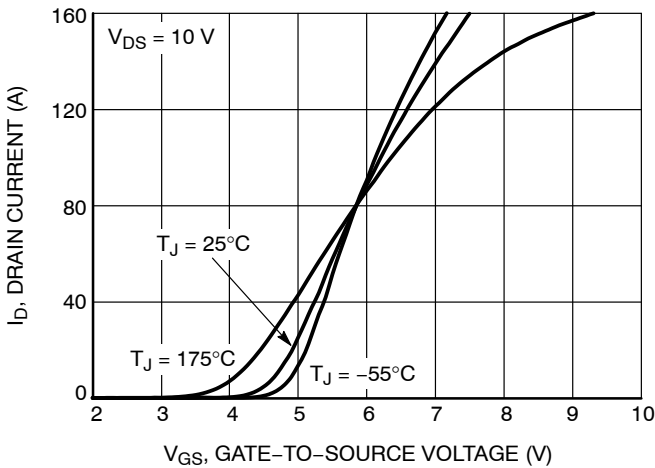


Figure 5. Transfer Characteristics

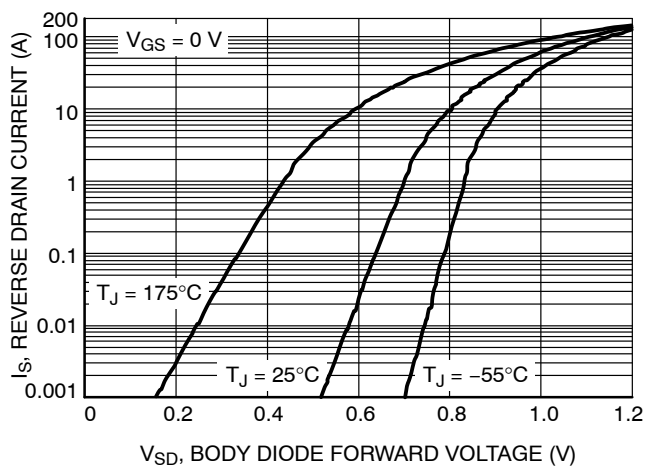


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

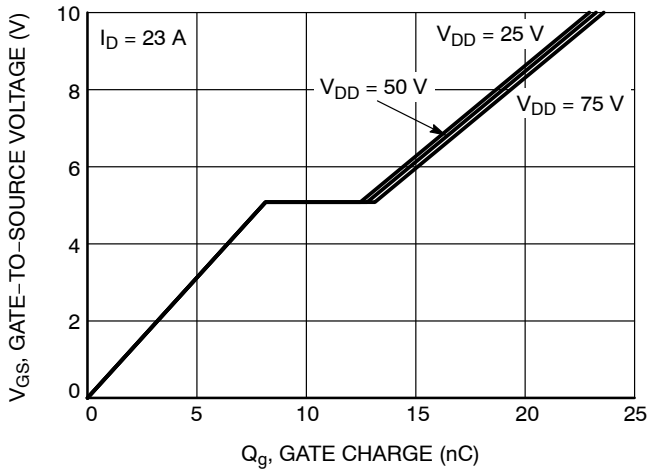


Figure 7. Gate Charge Characteristics

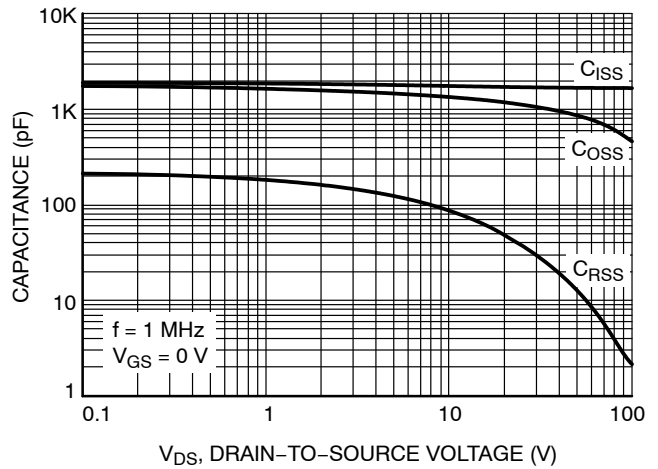


Figure 8. Capacitance vs. Drain-to-Source Voltage

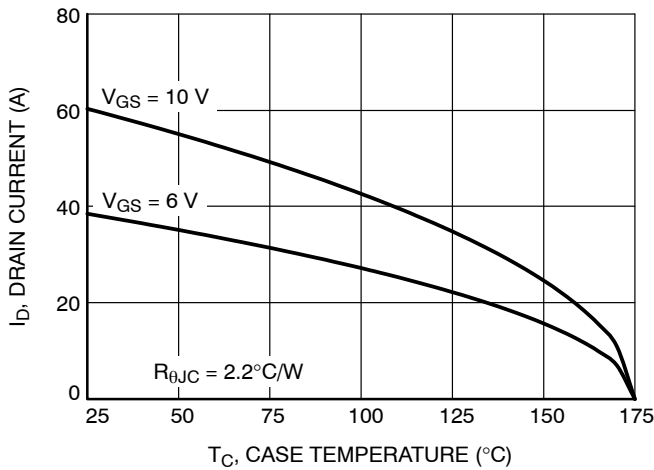


Figure 9. Drain Current vs. Case Temperature

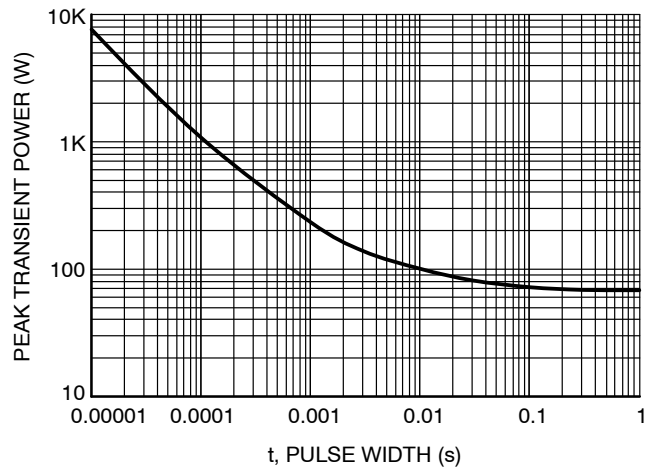


Figure 10. Peak Power

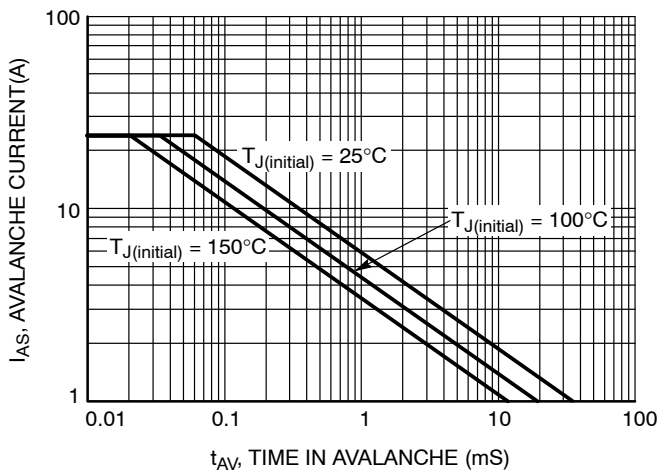


Figure 11. Unclamped Inductive Switching Capability

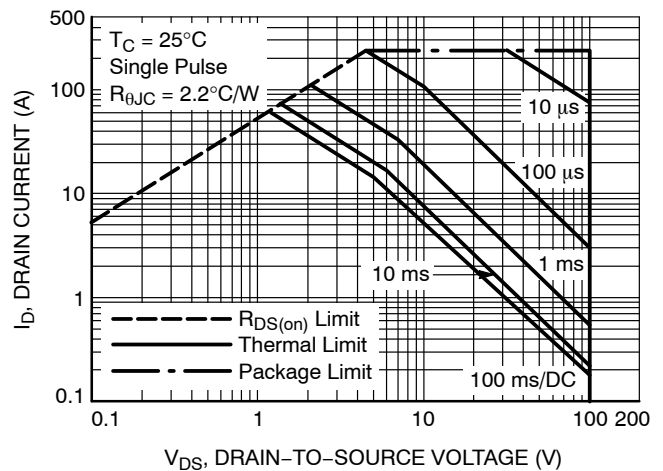


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

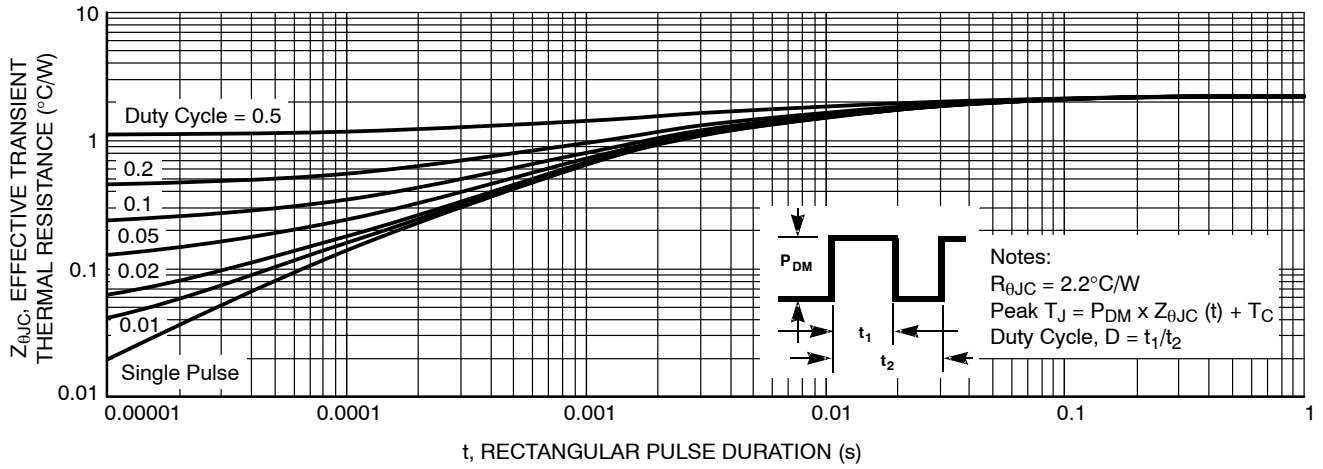
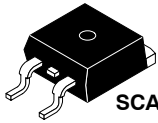


Figure 13. Transient Thermal Impedance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



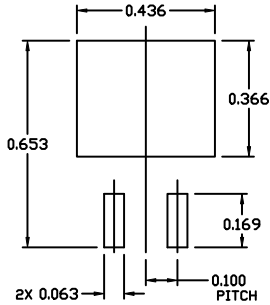
SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

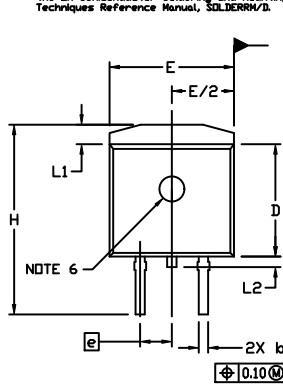
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

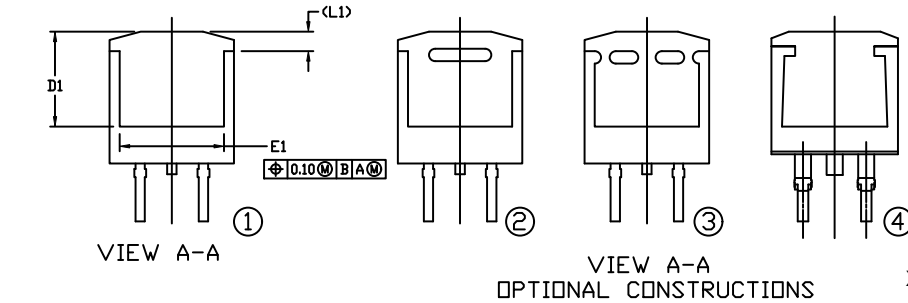
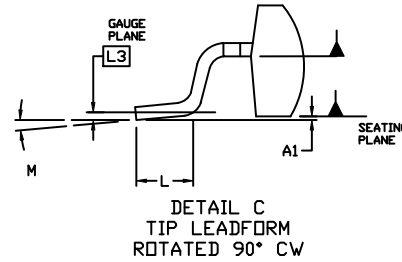
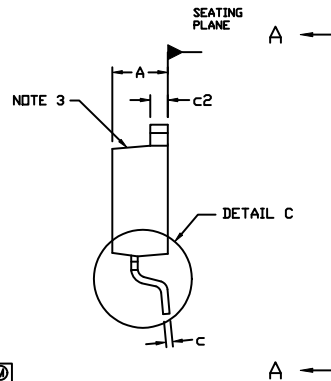
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



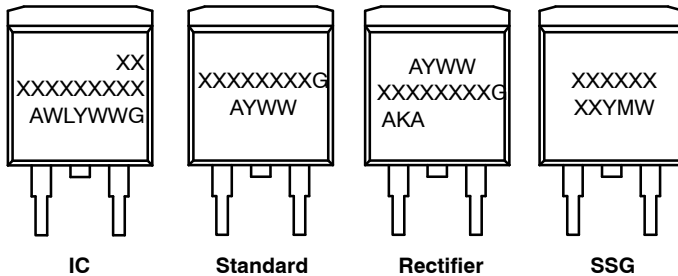
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*



GENERIC MARKING DIAGRAMS*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D²PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

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