AiP74HC/HCT164
8-bit Serial-in, Parallel-out Shift Register

Product Specification

Specification Revision History：

Version	Date	Description
2019-05-A1	2019-05	New

1、General Description

The AiP74HC/HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For AiP74HC164: CMOS level
  For AiP74HCT164: TTL level
- Gated serial data inputs
- Asynchronous master reset
- Specified from -40℃ to +85℃
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information:

Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
AiP74HC164DA.TB	DIP14	74HC164	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT164DA.TB	DIP14	74HCT164	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC164SA.TB	SOP14	74HC164	50 PCS/tube	200 tube/box	10000 PCS/box	5 box/pack	50000 PCS/pack	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HCT164SA.TB	SOP14	74HCT164	50 PCS/tube	200 tube/box	10000 PCS/box	5 box/pack	50000 PCS/pack	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HC164TA.TB	TSSOP14	74HC164	94 PCS/tube	200 tube/box	18800 PCS/box	10 box/pack	188000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT164TA.TB	TSSOP14	74HCT164	94 PCS/tube	200 tube/box	18800 PCS/box	10 box/pack	188000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Type number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Packing quantity	Notes
AiP74HC164SA.TR	SOP14	74HC164	2500 PCS/reel	5000 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HCT164SA.TR	SOP14	74HCT164	2500 PCS/reel	5000 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HC164TA.TR	TSSOP14	74HC164	4000 PCS/reel	8000 PCS/box	64000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT164TA.TR	TSSOP14	74HCT164	4000 PCS/reel	8000 PCS/box	64000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

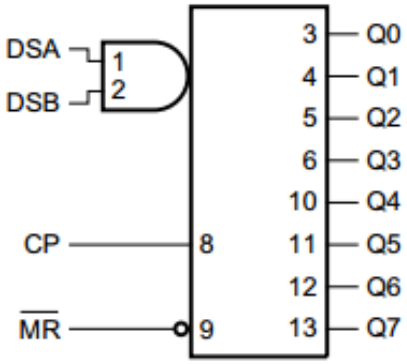


Figure 1. Logic symbol

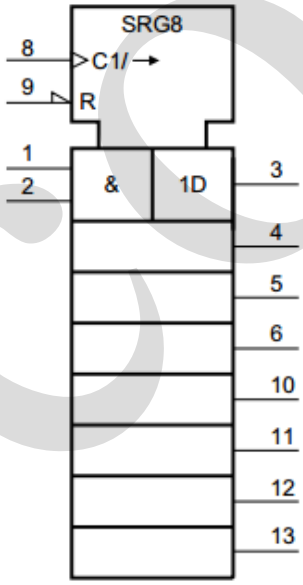


Figure 2. IEC logic symbol

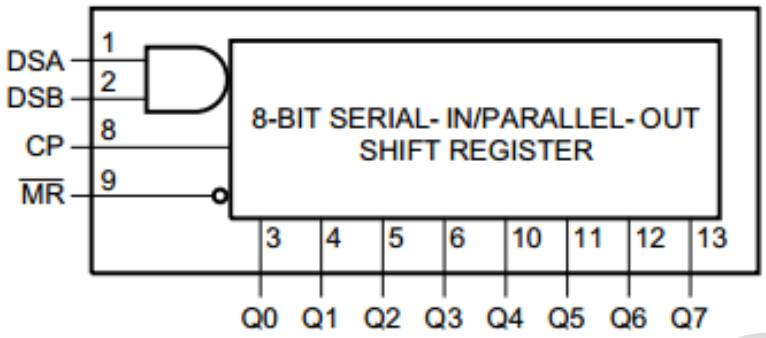


Figure 3. Logic diagram

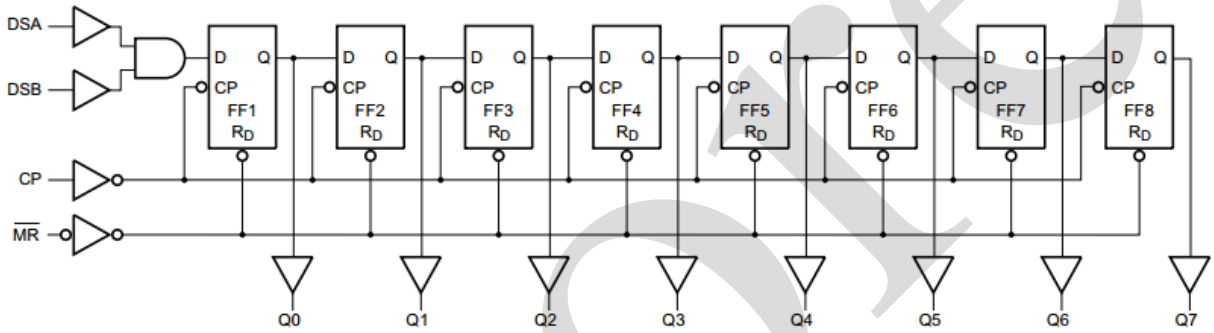
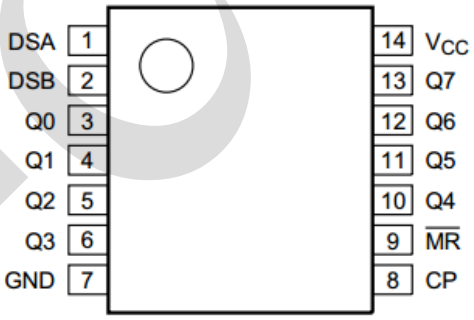


Figure 4. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	DSA	data input
2	DSB	data input
3	Q0	output
4	Q1	output
5	Q2	output
6	Q3	output
7	GND	ground (0V)

8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
10	Q4	output
11	Q5	output
12	Q6	output
13	Q7	output
14	V_{CC}	supply voltage

2.4、Function Table

Operating modes	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

Note: H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH clock transition;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q=lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC164						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃
AiP74HCT164						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC164							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA

input capacitance	C_I	-	-	3.5	-	pF
AiP74HCT164						
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
		$V_I = V_{IH}$ or V_{IL}; I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
		$V_I = V_{IH}$ or V_{IL}; I_O=5.2mA; V_{CC}=6.0V	-	0.15	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V	-	-	8	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	-	100	360	uA
input capacitance	C_I	-	-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
AiP74HC164						
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
		$V_I = V_{IH}$ or V_{IL}; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		$V_I = V_{IH}$ or V_{IL}; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		$V_I = V_{IH}$ or V_{IL}; I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
		$V_I = V_{IH}$ or V_{IL}; I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		$V_I = V_{IH}$ or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		$V_I = V_{IH}$ or V_{IL}; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		$V_I = V_{IH}$ or V_{IL}; I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
		$V_I = V_{IH}$ or V_{IL}; I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	80	uA
input capacitance	C_I	-	-	-	-	pF

AiP74HCT164							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	-	450	uA
input capacitance	C_I	-		-	-	-	pF

3.3.3、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC164							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	41	170	ns
			V_{CC}=4.5V	-	15	34	ns
			V_{CC}=5.0V;C_L=15pF	-	12	-	ns
			V_{CC}=6.0V	-	12	29	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	39	140	ns
			V_{CC}=4.5V	-	14	28	ns
			V_{CC}=5.0V;C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	11	24	ns
transition time	t_t	see Figure 6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
CP pulse width	t_W	see Figure 6	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
$\overline{MR}$ pulse width	t_W	see Figure 7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
$\overline{MR}$ to CP recovery time	t_{rec}	see Figure 7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
DSA and DSB to CP set-up time	t_{su}	see Figure 8	V_{CC}=2.0V	60	8	-	ns
			V_{CC}=4.5V	12	3	-	ns
			V_{CC}=6.0V	10	2	-	ns

DSA and DSB to CP hold time	t_h	see Figure 8	V_{CC}=2.0V	+4	-6	-	ns
			V_{CC}=4.5V	+4	-2	-	ns
			V_{CC}=6.0V	+4	-2	-	ns
CP maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	6	23	-	MHz
			V_{CC}=4.5V	30	71	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	78	-	MHz
			V_{CC}=6.0V	35	85	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}		-	40	-	pF
AiP74HCT164							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=4.5V	-	17	36	ns
			V_{CC}=5.0V;C_L=15pF	-	14	-	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	see Figure 7	V_{CC}=4.5V	-	19	38	ns
			V_{CC}=5.0V;C_L=15pF	-	16	-	ns
transition time	t_t	see Figure 6	V_{CC}=4.5V	-	7	15	ns
CP pulse width	t_W	see Figure 6	V_{CC}=4.5V	18	7	-	ns
$\overline{MR}$ pulse width	t_W	see Figure 7	V_{CC}=4.5V	18	10	-	ns
$\overline{MR}$ to CP recovery time	t_{rec}	see Figure 7	V_{CC}=4.5V	16	7	-	ns
DSA and DSB to CP set-up time	t_{su}	see Figure 7	V_{CC}=4.5V	12	6	-	ns
DSA and DSB to CP hold time	t_h	see Figure 8	V_{CC}=4.5V	+4	-2	-	ns
CP maximum frequency	f_{max}	see Figure 8	V_{CC}=4.5V	27	55	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	61	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}-1.5V		-	40	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC164							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	-	215	ns
			V_{CC}=4.5V	-	-	43	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	37	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	-	175	ns
			V_{CC}=4.5V	-	-	35	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	30	ns
transition time	t_t	see Figure 6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
CP pulse width	t_W	see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
$\overline{MR}$ pulse width	t_W	see Figure 7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
$\overline{MR}$ to CP recovery time	t_{rec}	see Figure 7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
DSA and DSB to CP set-up time	t_{su}	see Figure 8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
DSA and DSB to CP hold time	t_h	see Figure 8	V_{CC}=2.0V	4	-	-	ns
			V_{CC}=4.5V	4	-	-	ns
			V_{CC}=6.0V	4	-	-	ns
CP maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}		-	-	-	pF
AiP74HCT164							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=4.5V	-	-	45	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	see Figure 7	V_{CC}=4.5V	-	-	48	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
transition time	t_t	see Figure 6	V_{CC}=4.5V	-	-	19	ns
CP pulse width	t_W	see Figure 6	V_{CC}=4.5V	23	-	-	ns

$\overline{MR}$ pulse width	t_W	see Figure 7	V_{CC}=4.5V	23	-	-	ns
$\overline{MR}$ to CP recovery time	t_{rec}	see Figure 7	V_{CC}=4.5V	20	-	-	ns
DSA and DSB to CP set-up time	t_{su}	see Figure 8	V_{CC}=4.5V	15	-	-	ns
DSA and DSB to CP; hold time	t_h	see Figure 8	V_{CC}=4.5V	+4	-	-	ns
CP maximum frequency	f_{max}	see Figure 6	V_{CC}=4.5V	22	-	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	-	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}-1.5V		-	-	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

4、Testing Circuit

4.1、AC Testing Circuit

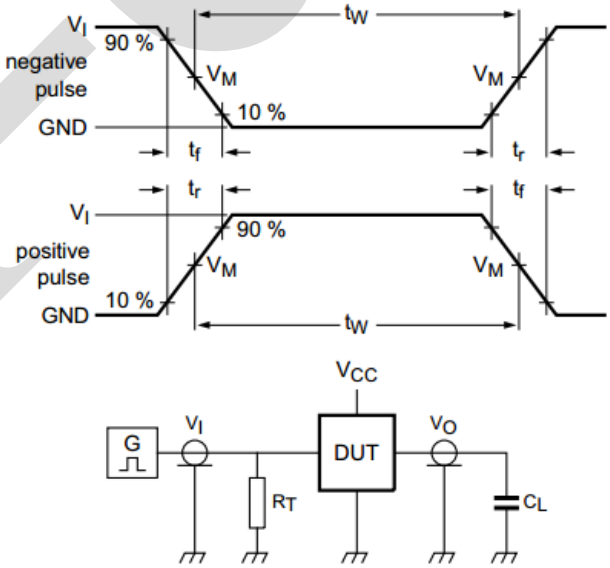


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

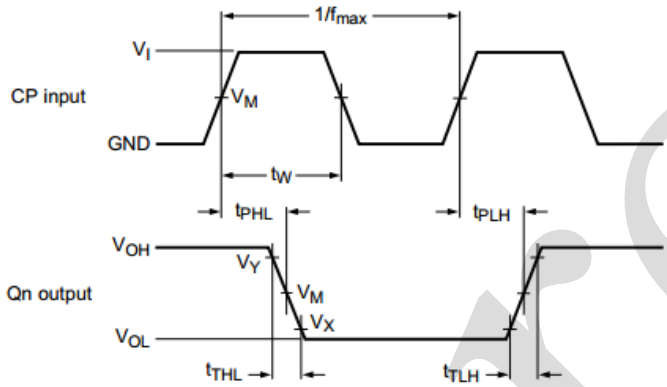


Figure 6. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

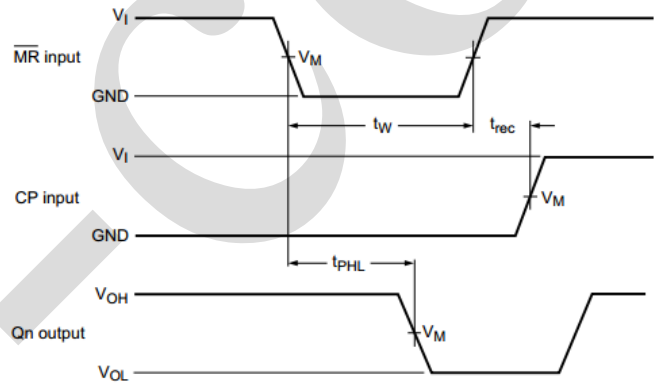


Figure 7. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

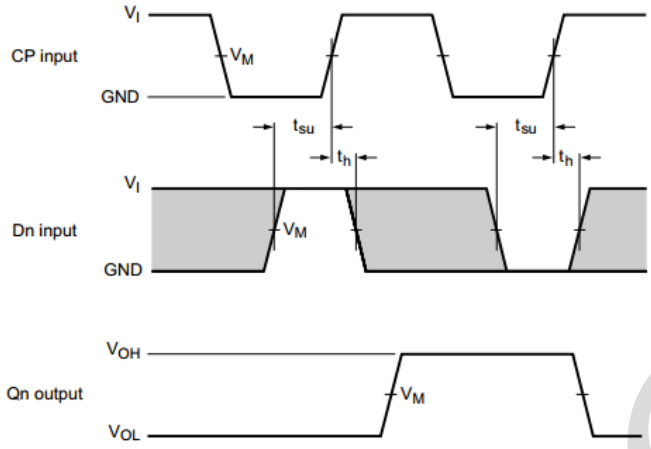


Figure 8. Waveforms showing the data set-up and hold times for Dn inputs

4.3、Measurement Points

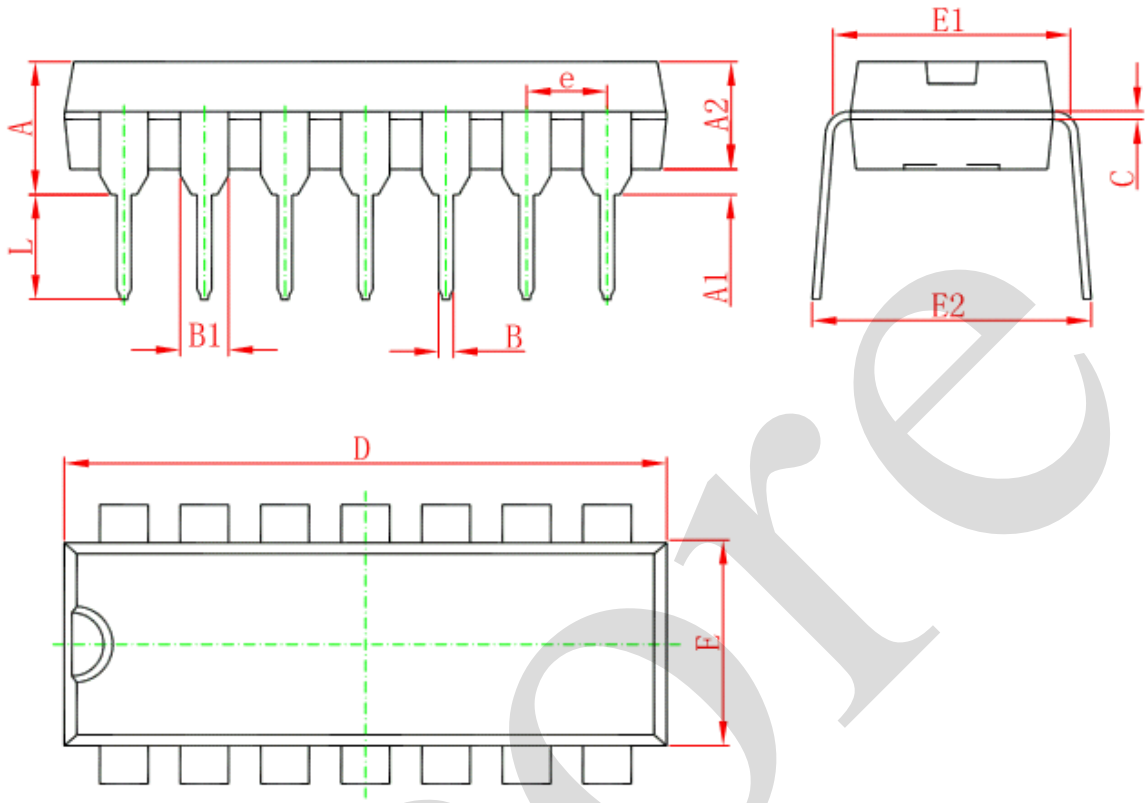
Type	Input	Output		
	V_M	V_M	V_X	V_Y
AiP74HC164	$0.5\times V_{CC}$	$0.5\times V_{CC}$	$0.1\times V_{CC}$	$0.9\times V_{CC}$
AiP74HCT164	1.3V	1.3V	$0.1\times V_{CC}$	$0.9\times V_{CC}$

4.4、Test Data

Type	Input		Load	Test
	V_I	t_r , t_f	C_L	
AiP74HC164	V_{CC}	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}
AiP74HCT164	3.0V	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}

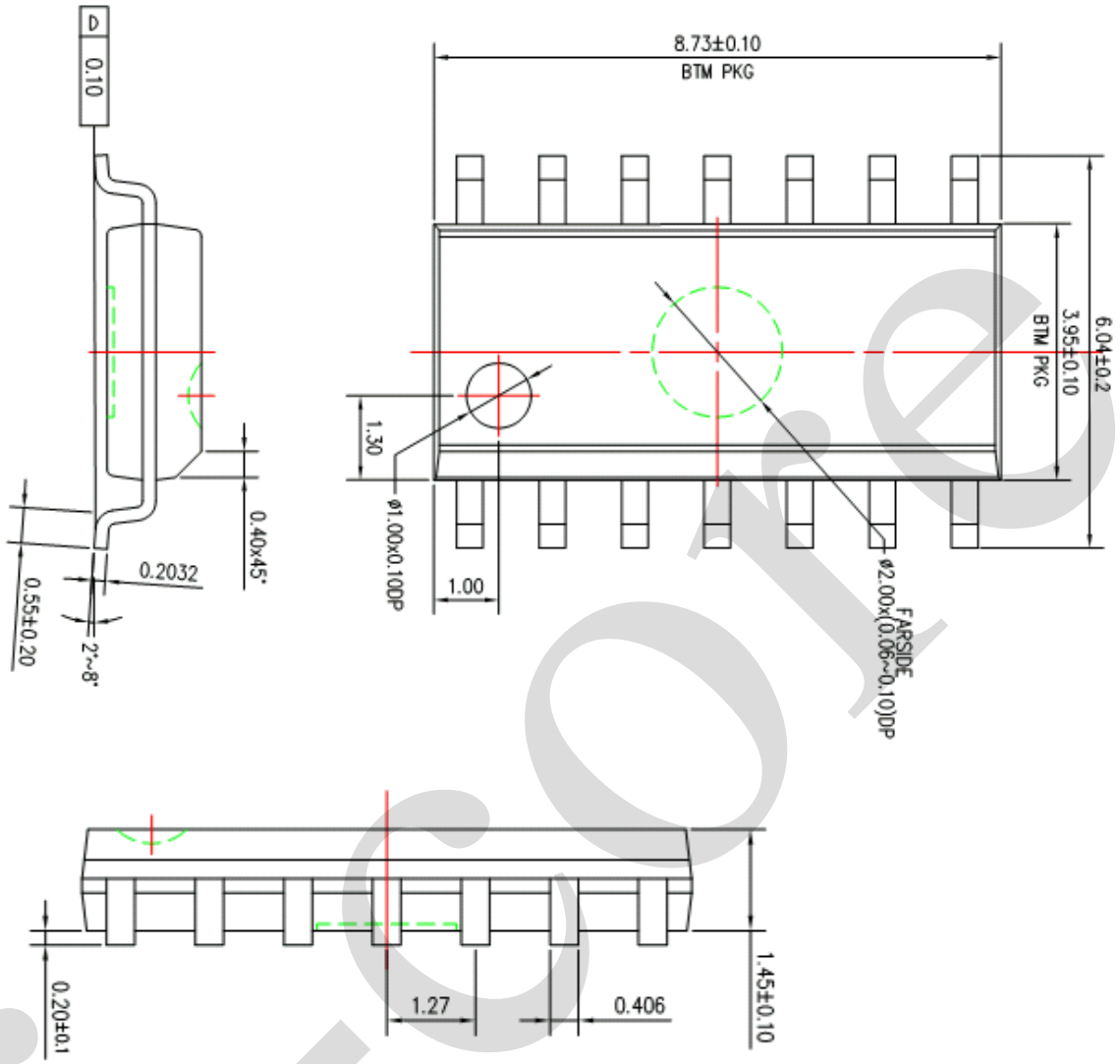
5、Package Information

5.1、DIP14

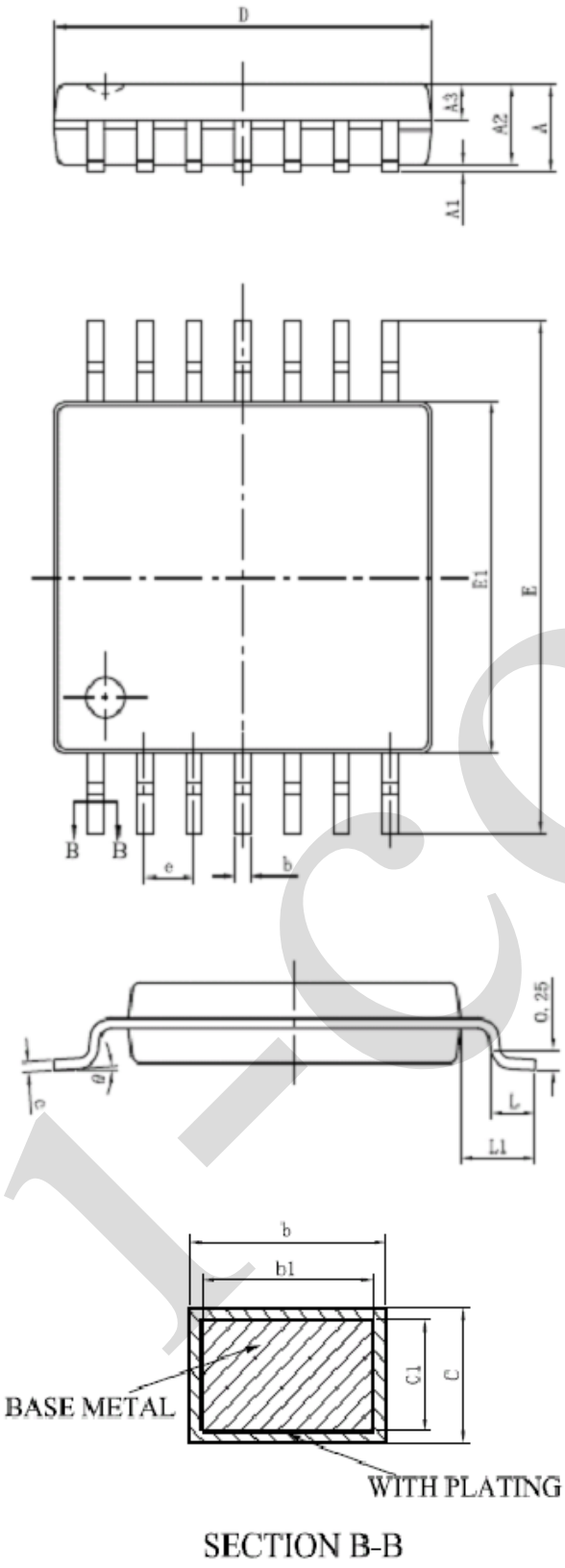


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOP14


0.10
8.73±0.10
BTM PKG
6.04±0.2
3.95±0.10
BTM PKG
1.30
Ø1.00x0.100P
1.00
Ø2.00x(0.06~0.10)DP
FARSIDE
0.40x45°
0.2032
0.55±0.20
2°~8°
0.20±0.1
1.27
0.406
1.45±0.10

5.3、TSSOP14



SECTION B-B

SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。									

6.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.