

# **Dual N-Channel 30 V (D-S) MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
30	0.016 at V <sub>GS</sub> = 10 V	8.5	7.1		
30	0.020 at V <sub>GS</sub> = 4.5 V	7.6	7.1		

#### **FEATURES**

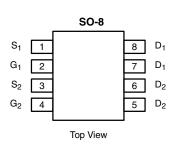
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

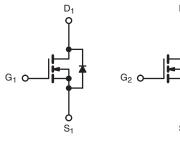


ROHS COMPLIANT

#### **APPLICATIONS**

- Notebook System Power
- Low Current DC/DC





N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (TA	$_{\rm A}$ = 25 °C, unless othe	rwise noted)			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	$V_{DS}$	30	V		
Gate-Source Voltage	$V_{GS}$	± 20	, v		
	T <sub>C</sub> = 25 °C		8.5		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	7.5		
Continuous Diam Current (1) = 130 °C)	T <sub>A</sub> = 25 °C	'D	7.2 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		5.9 <sup>b, c</sup>		
Pulsed Drain Current		I <sub>DM</sub>	30	Α	
Source-Drain Current Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	2.8	Α	
Source-Drain Guitent Diode Guitent	T <sub>A</sub> = 25 °C	'S	1.8 <sup>b, c</sup>	1	
Pulsed Source-Drain Current	·	I <sub>SM</sub>	30		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	10		
Single Pulse Avalanche Energy	L = 0.1 IIII1	E <sub>AS</sub>	5		
	T <sub>C</sub> = 25 °C		3.1		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	$P_{D}$	2.0	W	
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	י ט	2.0 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		1.25 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Тур.	Max.	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	52	62.5	°C/W		
Maximum Junction-to-Foot (Drain)	Steady-State	$R_{thJF}$	30	40	7 5/11		

#### Notes:

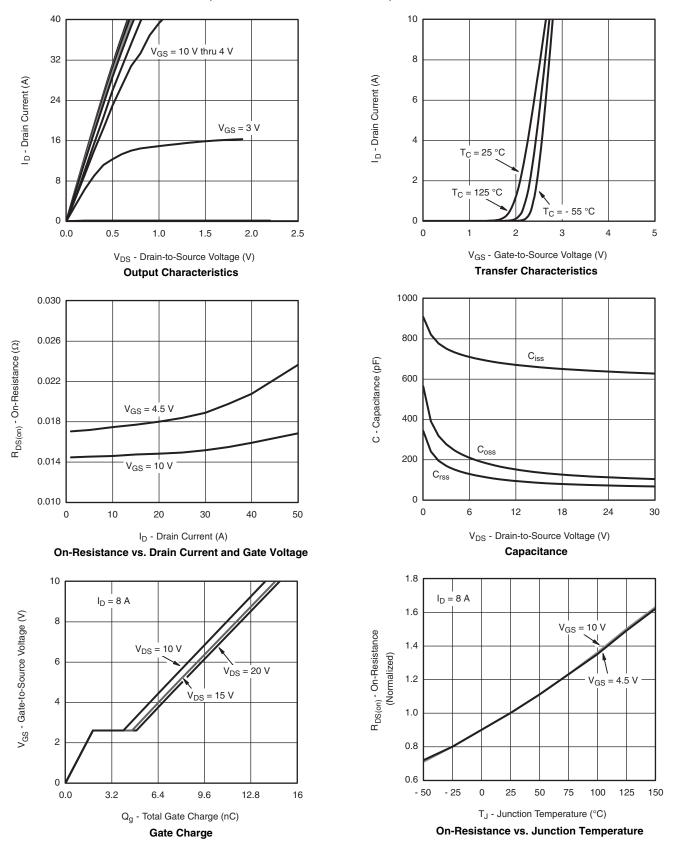
- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 110 °C/W.



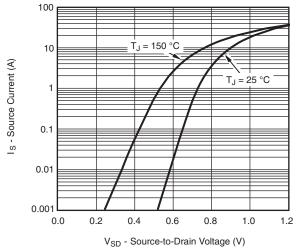
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	l .						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA	3.0			m\//°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 5.2		mV/°C	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2		2.5	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			100	nA	
Zava Cata Valtaga Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, TJ = 55 °C			10	μΑ	
On -State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	20			Α	
	В	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$			0.016		
Drain-Source On-State Resistance <sup>D</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$			0.020	Ω	
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8 A		27		S	
Dynamic <sup>a</sup>	l .				•		
Input Capacitance	C <sub>iss</sub>			660		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 MHz		140			
Reverse Transfer Capacitance	C <sub>rss</sub>			86			
Tabal Oada Obaara		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 8 \text{ A}$		14.5	22	22 11 nC	
Total Gate Charge	Q <sub>g</sub>			7.1	11		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 8 \text{ A}$		1.9			
Gate-Drain Charge	$Q_{gd}$			2.7			
Gate Resistance	$R_g$	f = 1 MHz	0.5	2.6	5.2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			14	28		
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega$		45	80		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		18	35		
Fall Time	t <sub>f</sub>			12	24	20	
Turn-On Delay Time	t <sub>d(on)</sub>			7	14	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$		10	20	_	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		15	30		
Fall Time	t <sub>f</sub>			7	14		
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.8	Λ	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	SM			30	А	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 2 A		0.77	1.1	٧	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			17	34	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	l <sub>F</sub> = 5 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		9	18	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	1   - 3 A, αι/αι = 100 A/μs, 1   = 25 °C   -		10		r.C	
Reverse Recovery Rise Time	t <sub>b</sub>	1		7		nS	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

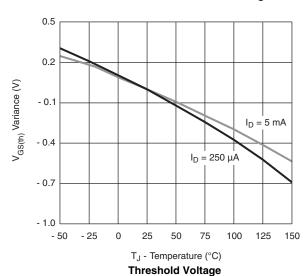






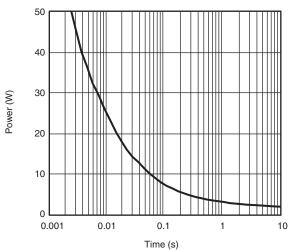


Source-Drain Diode Forward Voltage

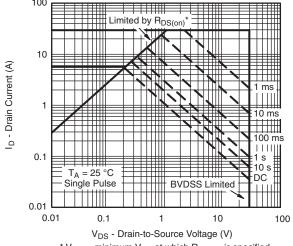


0.10
0.08
0.08
0.08
0.06
0.04
0.02
0.00
0 1 2 3 4 5 6 7 8 9 10  $V_{GS}$  - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



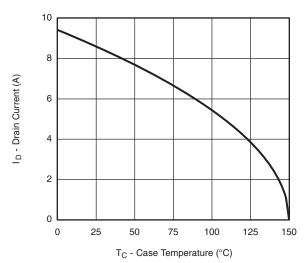
Single Pulse Power, Junction-to-Ambient



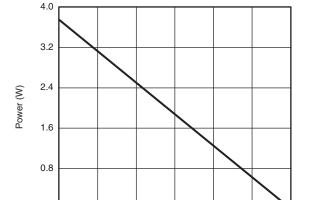
\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

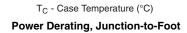
Safe Operating Area, Junction-to-Ambient





#### **Current Derating\***



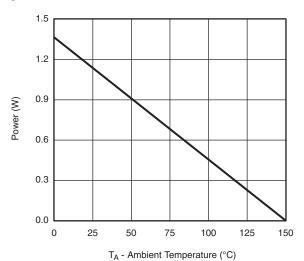


75

100

125

150



Power Derating, Junction-to-Ambient

E-mail: China@VBsemi TEL:86-755-83251052

0.0

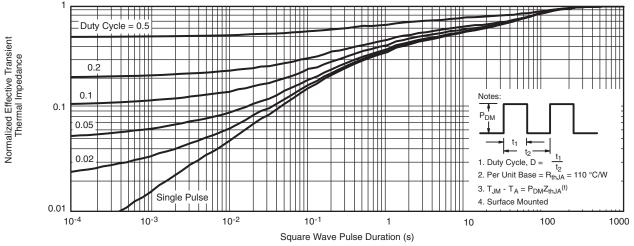
0

25

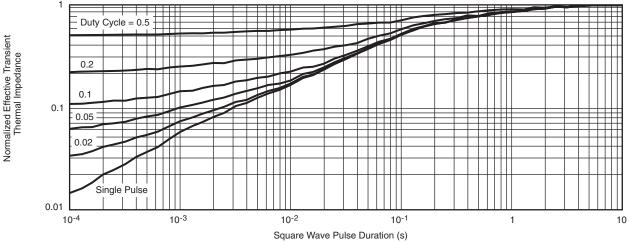
50

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





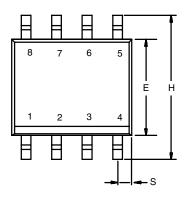
Normalized Thermal Transient Impedance, Junction-to-Ambient

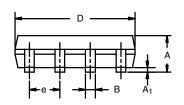


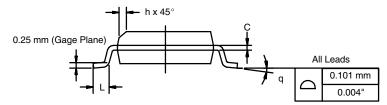
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





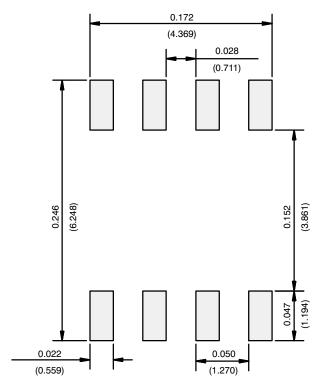


	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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