

## NCE N-Channel Super Trench Power MOSFET

### Description

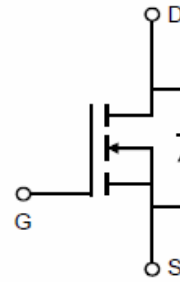
The NCEP40T13GU uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

### General Features

- $V_{DS} = 40V, I_D = 130A$
- $R_{DS(ON)} = 1.8m\Omega$  (typical) @  $V_{GS} = 10V$
- $R_{DS(ON)} = 2.8m\Omega$  (typical) @  $V_{GS} = 4.5V$
- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

### Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View

Bottom View

**100% UIS TESTED!**

**100% ΔVds TESTED!**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP40T13GU	NCEP40T13GU	DFN5X6-8L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous ( <b>Silicon Limited</b> )	$I_D$	130	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	100	A
Pulsed Drain Current ( <b>Package Limited</b> )	$I_{DM}$	400	A
Maximum Power Dissipation	$P_D$	130	W
Derating factor		1.04	W/°C
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	600	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.96	$^{\circ}C/W$
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**Electrical Characteristics ( $T_C=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.7	2.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=65A$	-	1.8	2.3	m $\Omega$
		$V_{GS}=4.5V, I_D=65A$	-	2.8	3.6	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=65A$	-	62	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	3334	3990	PF
Output Capacitance	$C_{oss}$		-	650	750	PF
Reverse Transfer Capacitance	$C_{rss}$		-	57	68	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=65A$ $V_{GS}=10V, R_G=1.6\Omega$	-	10	-	nS
Turn-on Rise Time	$t_r$		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	$t_f$		-	3	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=65A,$ $V_{GS}=10V$	-	49	70	nC
Gate-Source Charge	$Q_{gs}$		-	9.4		nC
Gate-Drain Charge	$Q_{gd}$		-	5		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=65A$	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	130	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-		23	nS
Reverse Recovery Charge	$Q_{rr}$		-		67	nC

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}C, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

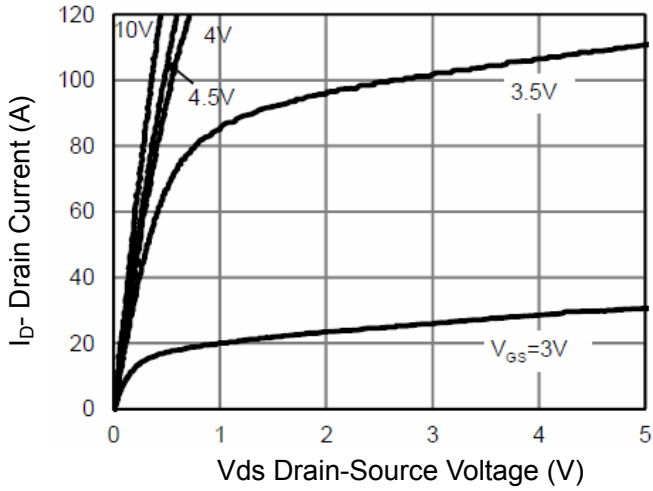


Figure 1 Output Characteristics

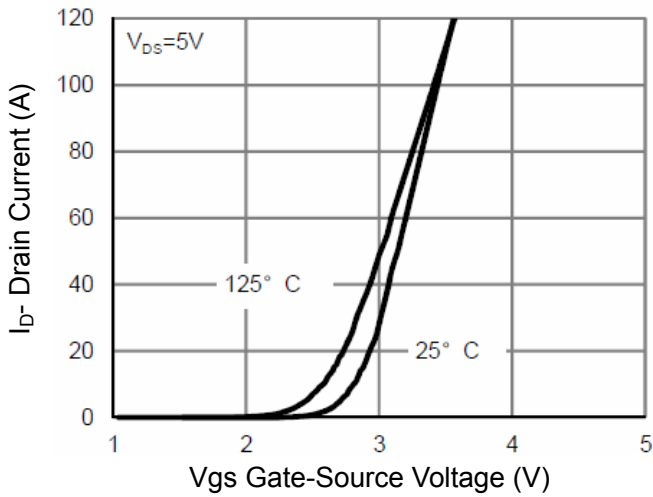


Figure 2 Transfer Characteristics

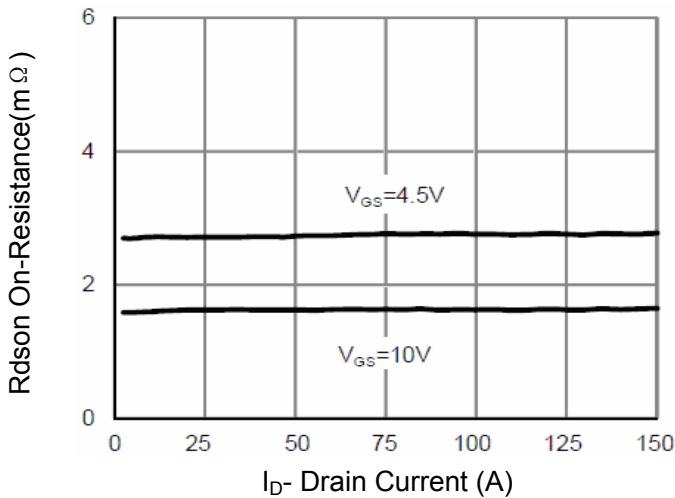


Figure 3  $R_{DS(on)}$  vs. Drain Current

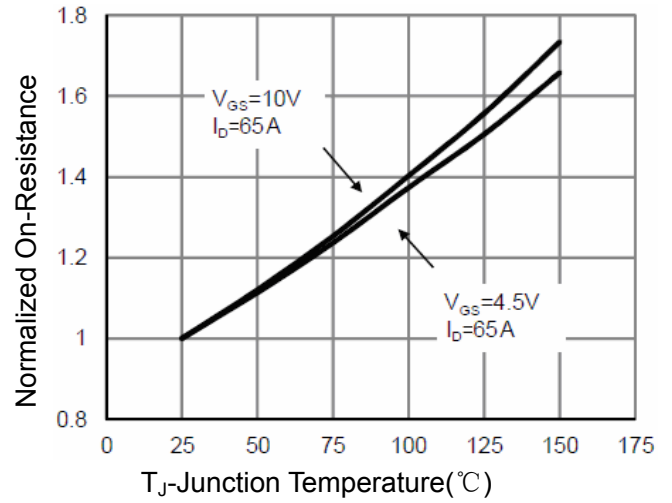


Figure 4  $R_{DS(on)}$  vs. Junction Temperature

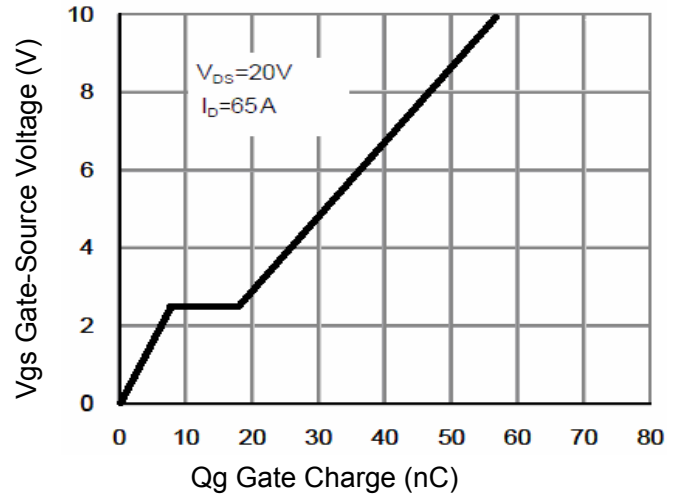


Figure 5 Gate Charge

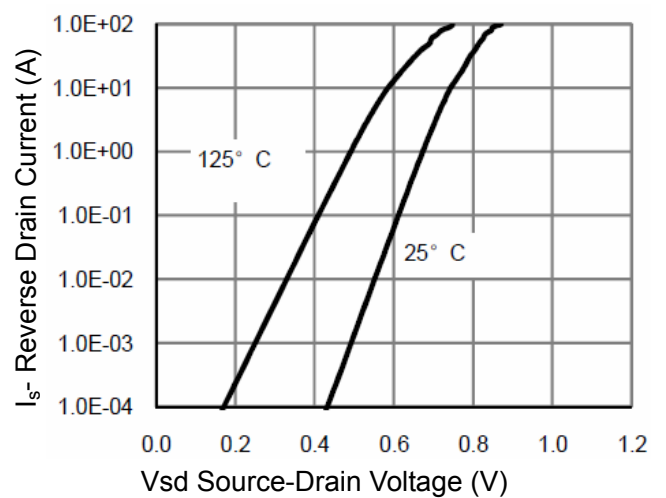


Figure 6 Source-Drain Diode Forward

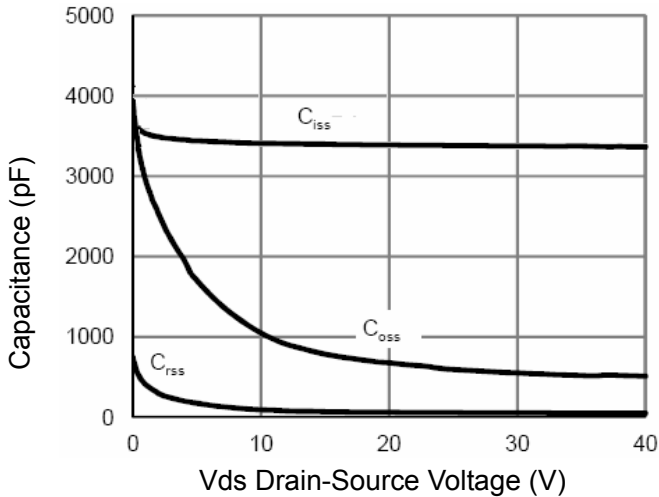


Figure 7 Capacitance vs Vds

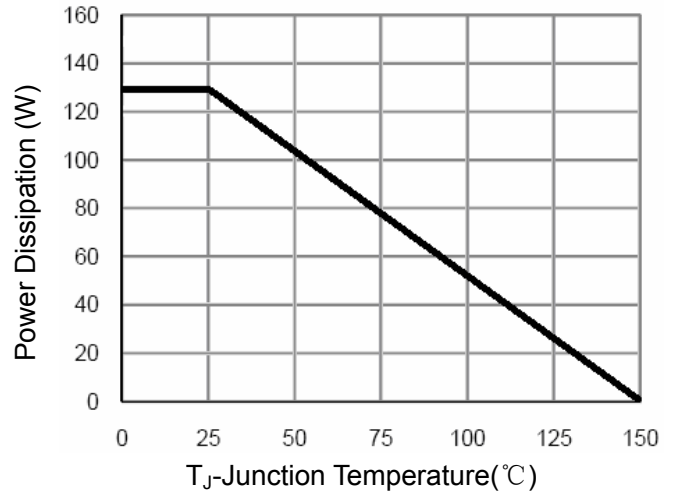


Figure 9 Power De-rating

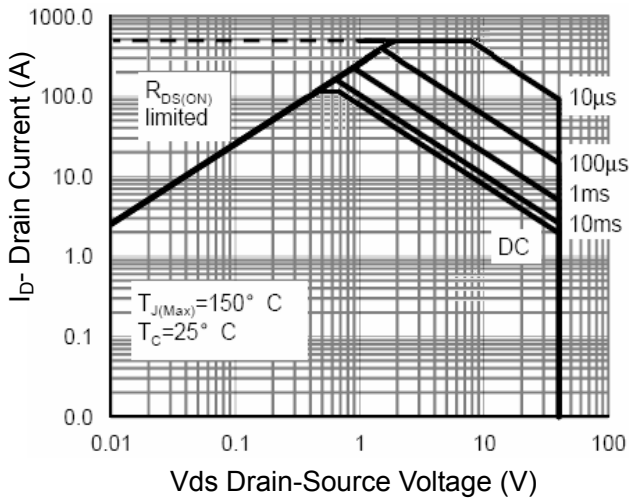


Figure 8 Safe Operation Area

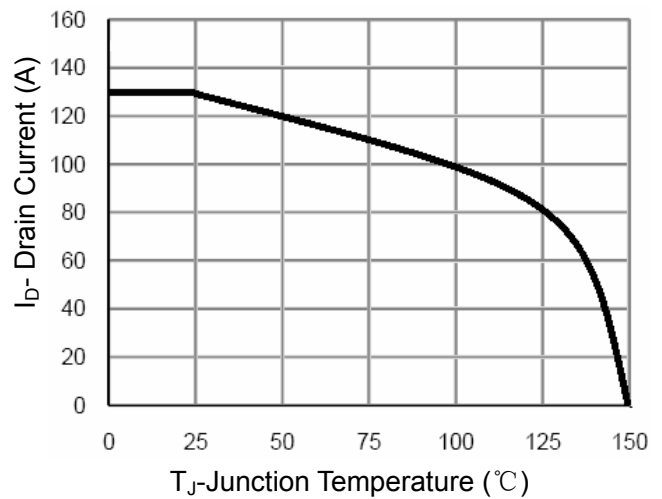


Figure 10 Current De-rating

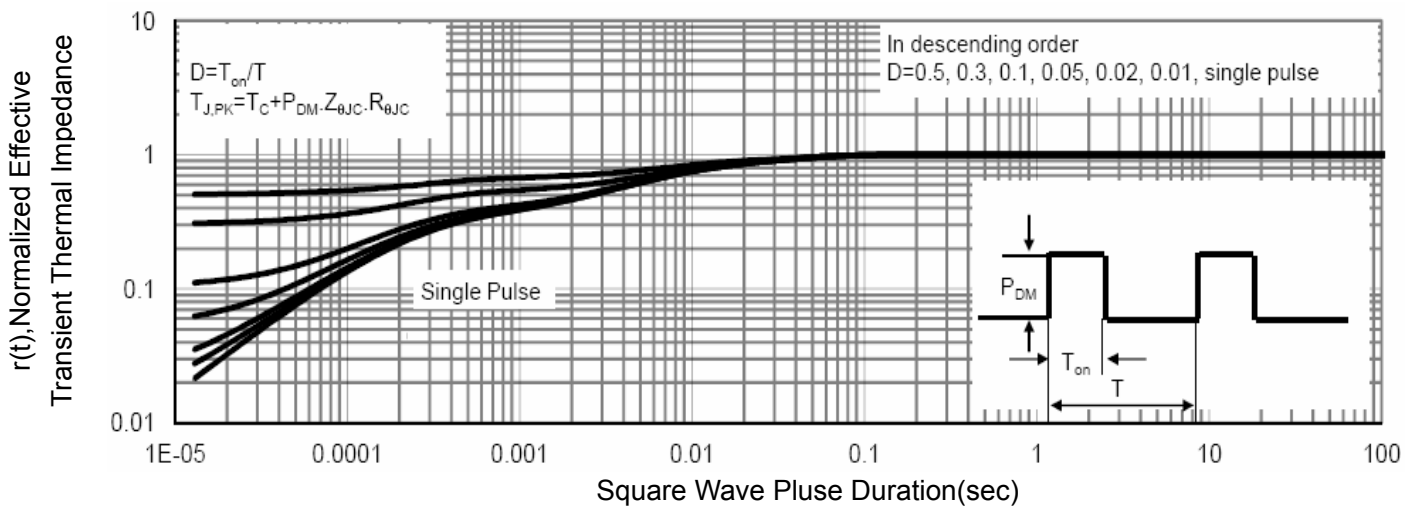
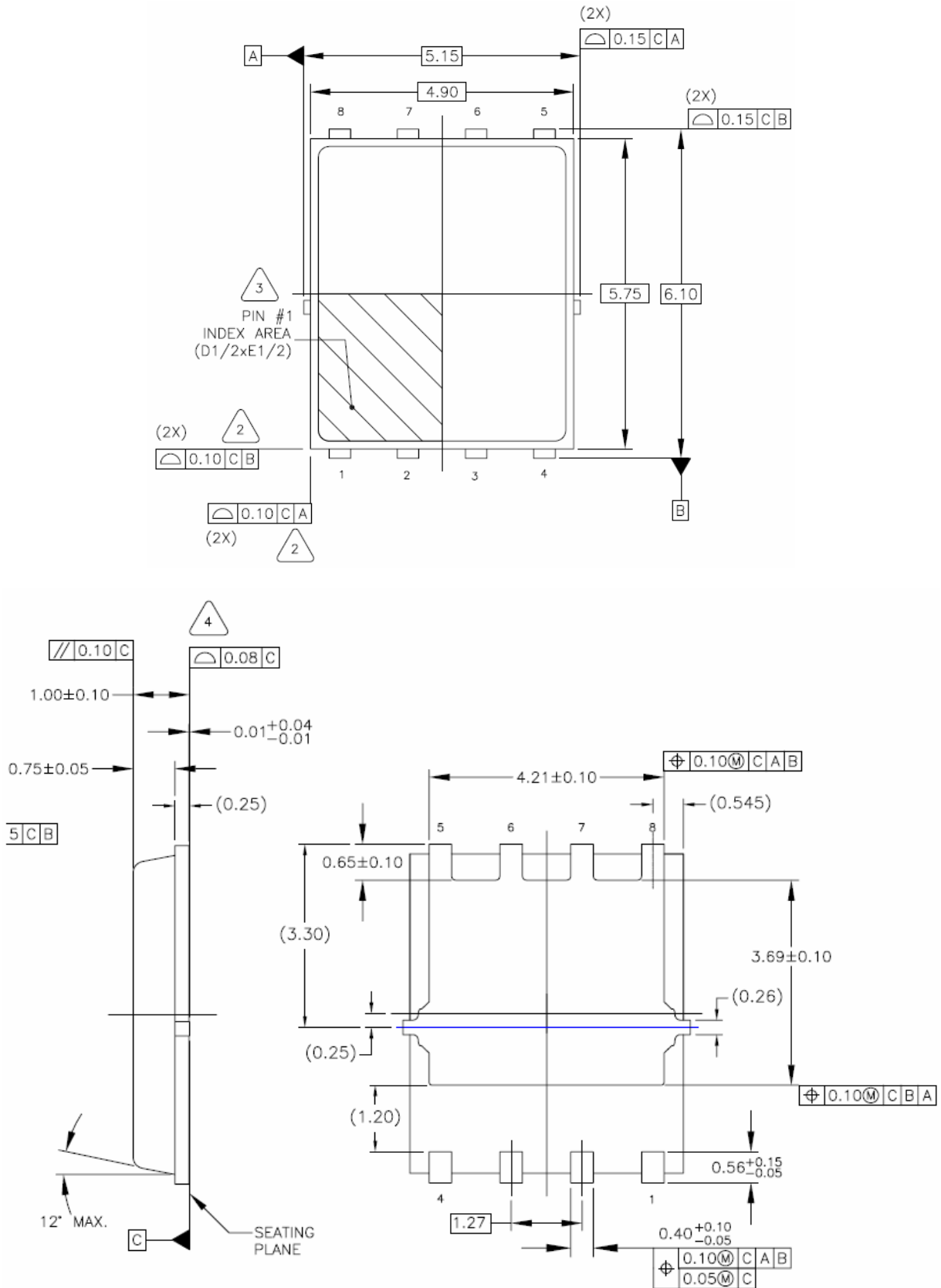


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



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