

N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The PW2202 is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system

FEATURES

$V_{DS} = 200V$, $I_D = 2A$

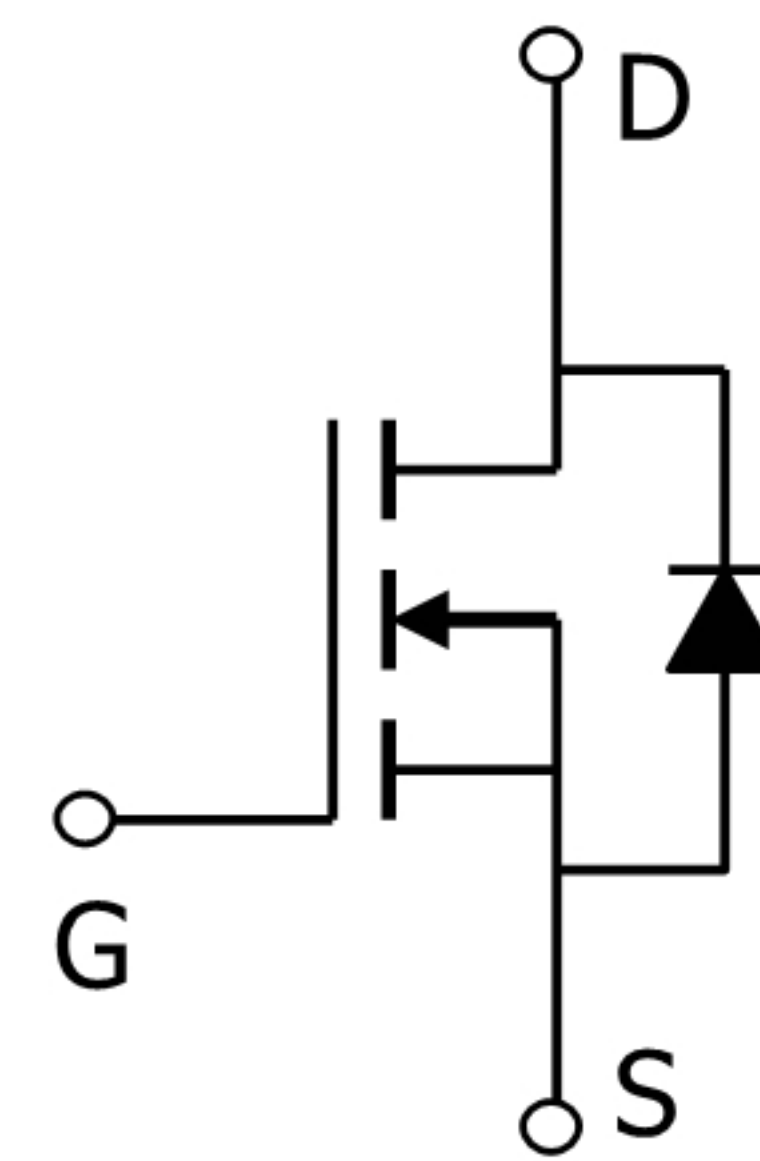
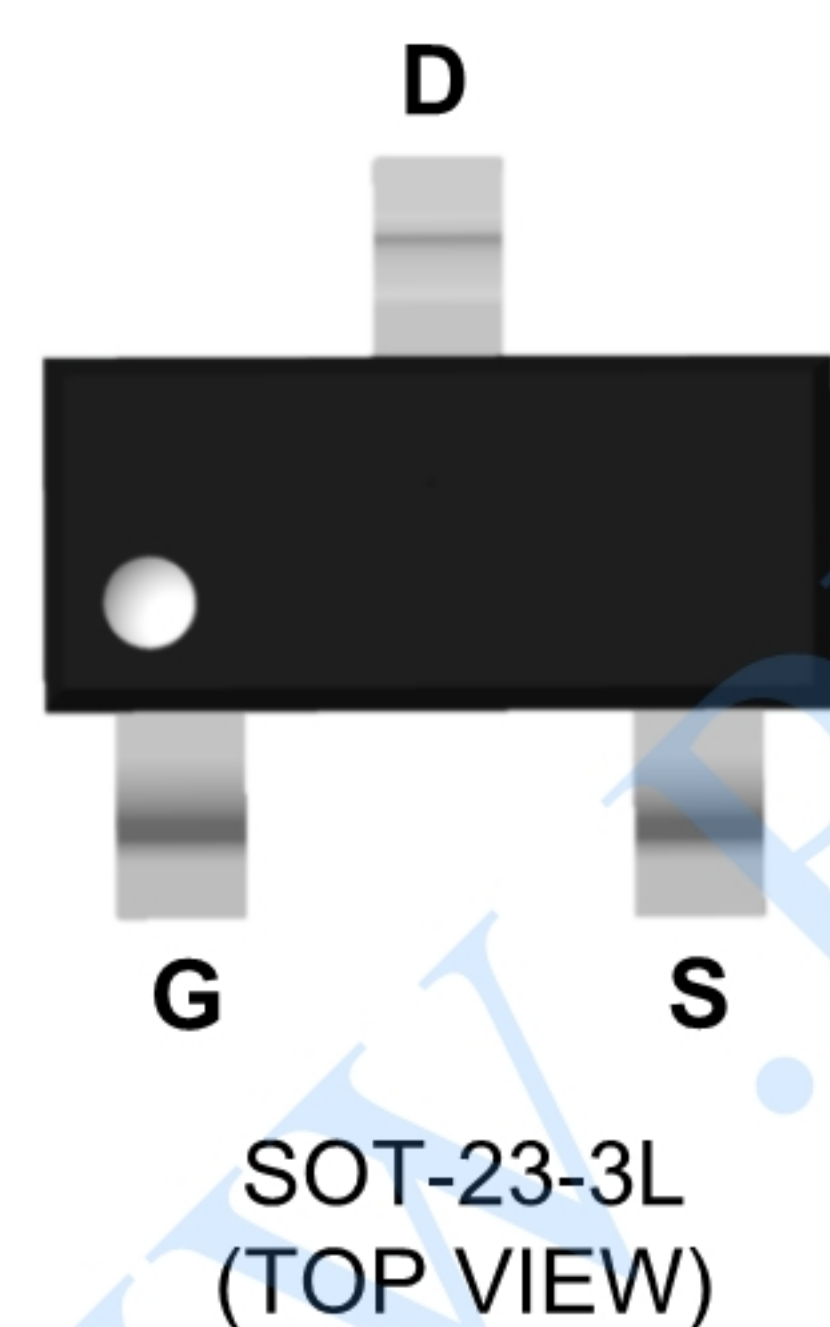
$R_{DS(ON)} < 1.8\Omega$ @ $V_{GS} = 10V$

Available in a 3-Pin SOT23-3 Package

Application

LED dimming

Emergency lamp



Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_{D@TA=25^\circ C}$	2	A
Pulsed Drain Current (NOTE1)	I_{DM}	10	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$
Thermal Resistance Junction-Ambient (NOTE2)	$R_{\theta JA}$	41.7	$^\circ C/W$

Note 1、 Repetitive Rating: Pulse width limited by maximum junction temperature.

Note 2、 Surface Mounted on FR4 Board, $t \leq 10$ sec.



ELECTRICAL CHARACTERISTICS

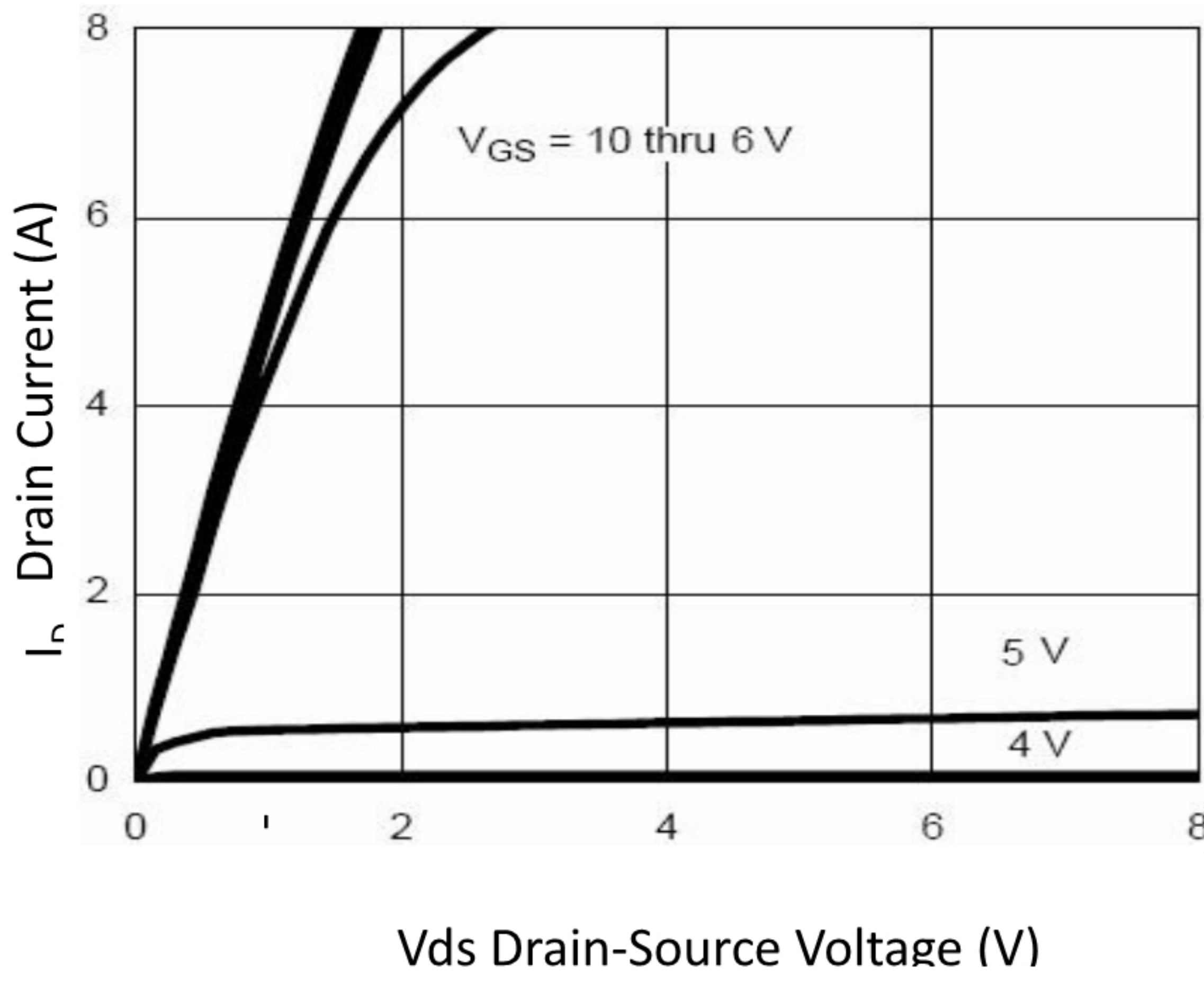
(TA = 25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	200			V
R _{DS(ON)}	Drain-Source On- Static Resistance	V _{GS} =10V , I _D =2A		1.4	1.8	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	1.0		3.0	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =200V , V _{GS} =0V ,			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V , V _{DS} =0V			±100	nA
g _{fs}	Forward Transconductance	V _{DS} =15V , I _D =2A		8		S
Q _g	Total Gate Charge	V _{DS} =100V , V _{GS} =10V , I _D =2A		12		nC
Q _{gs}	Gate-Source Charge			2.5		nC
Q _{gd}	Gate-Drain Charge			3.8		nC
T _{d(on)}	Turn-On Delay Time	V _{DS} =100V , V _{GS} =10V , R _G =2.5Ω, R _L =15Ω		10		ns
T _r	Rise Time			12		ns
T _{d(off)}	Turn-Off Delay Time			15		ns
T _f	Fall Time			15		ns
C _{iss}	Input Capacitance	V _{DS} =25V , V _{GS} =0V , f=1MHz		580		pF
C _{oss}	Output Capacitance			90		pF
C _{rss}	Reverse Transfer Capacitance			3		pF
I _s	Continuous Source Current (NOTE1)				2	A
V _{SD}	Diode Forward Voltage (NOTE2)	V _{GS} =0V , I _s =1A ,			1.2	V

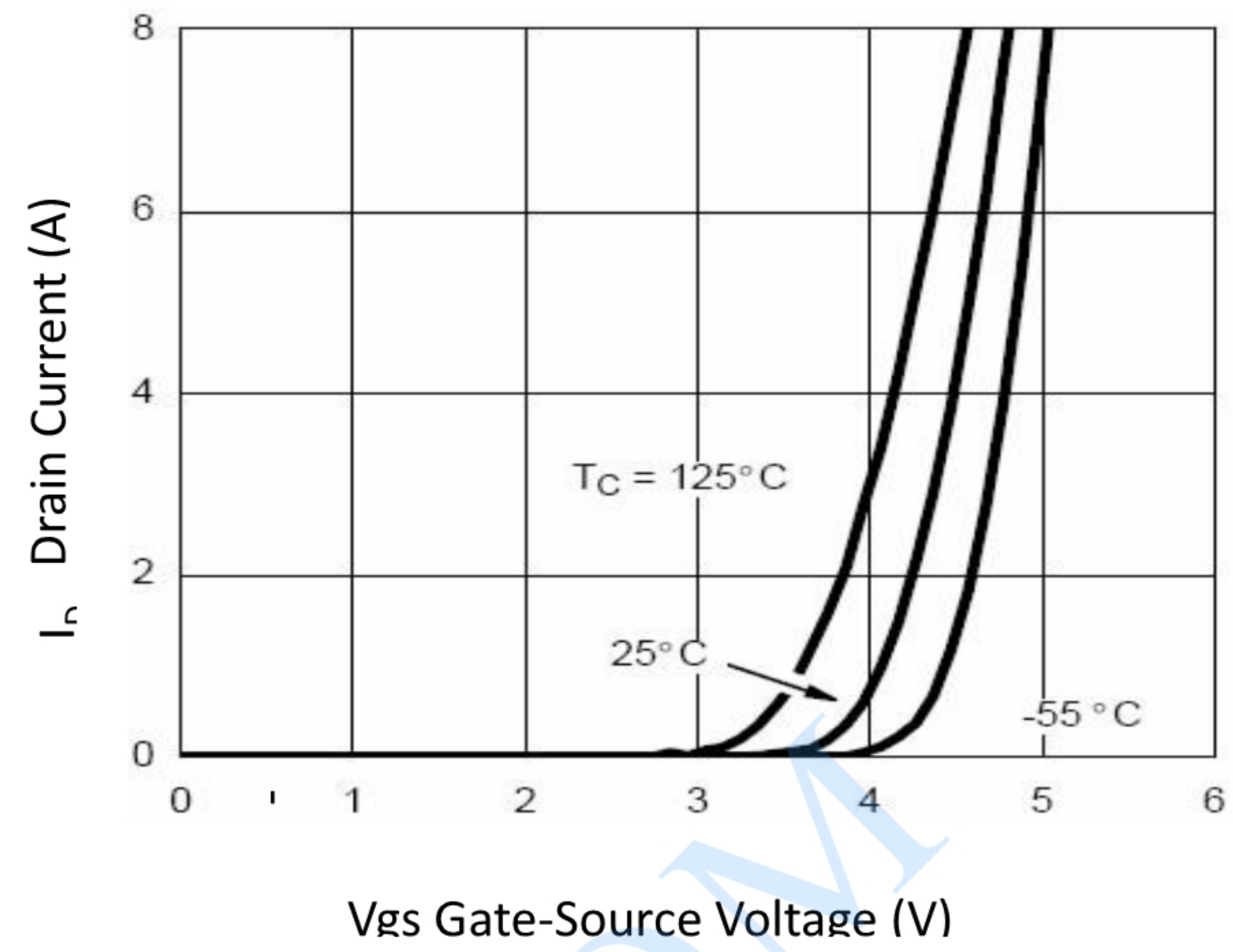
Note 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

Note 2. Guaranteed by design, not subject to production

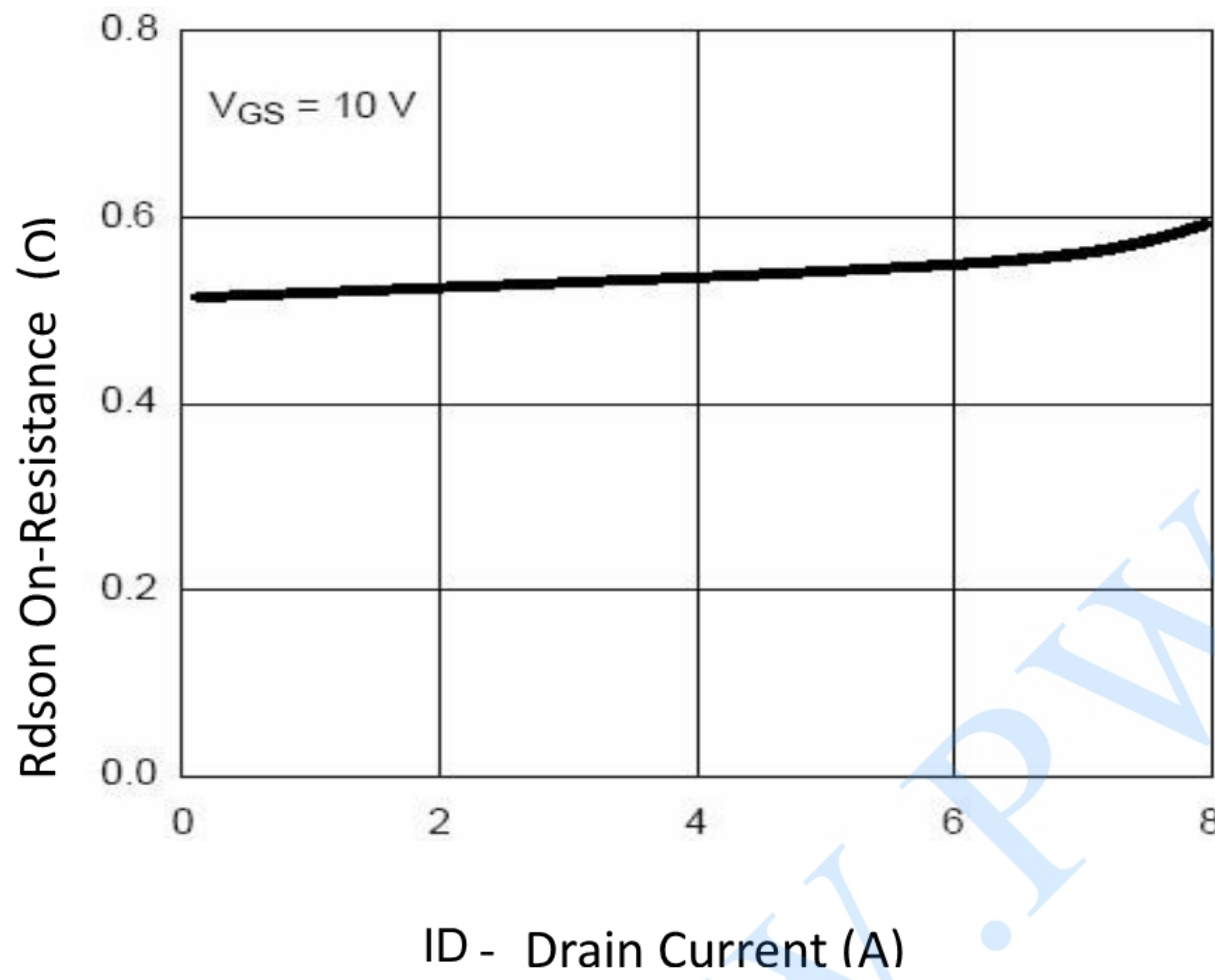
Thermal Characteristics And Typical electrical



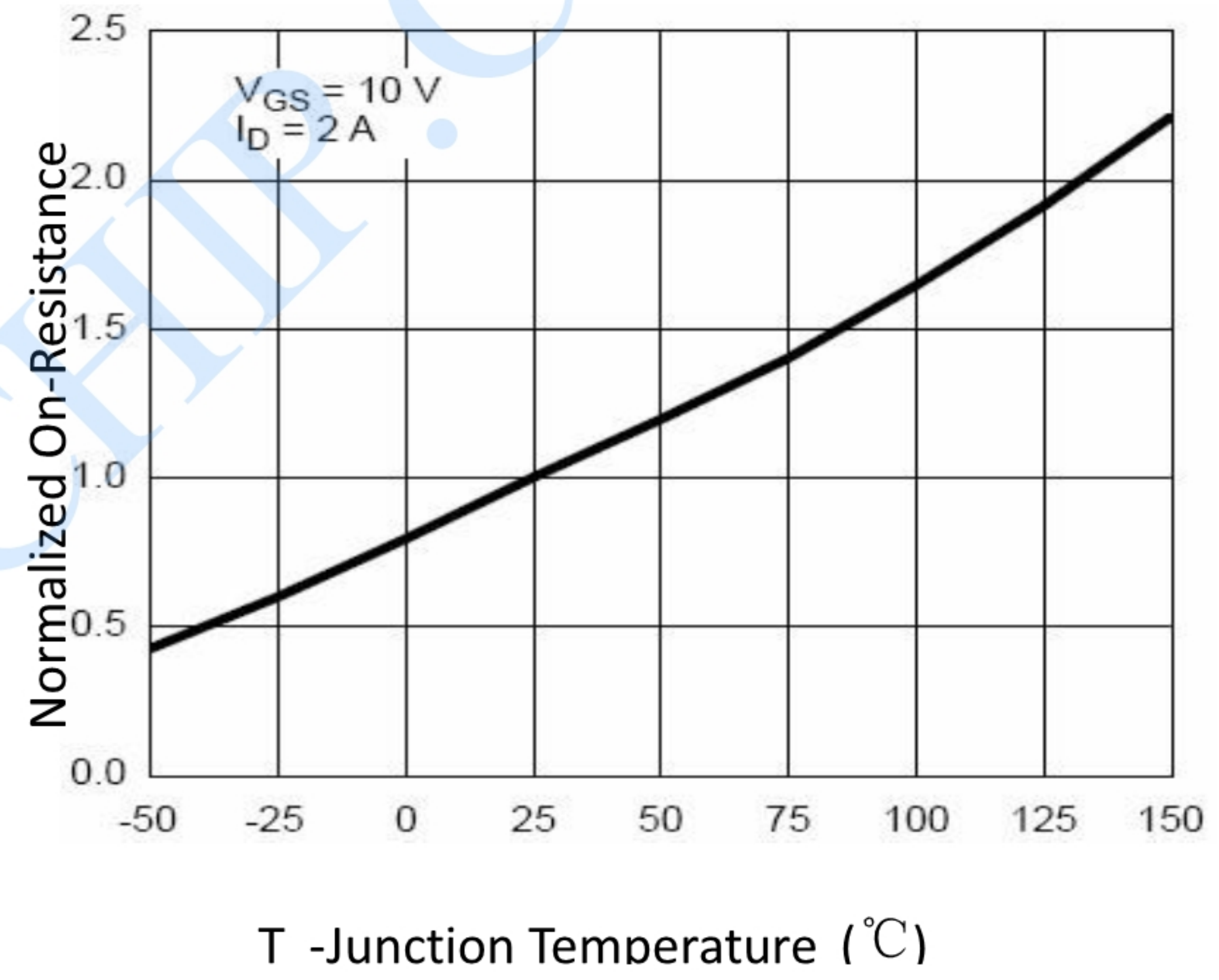
Output Characteristics



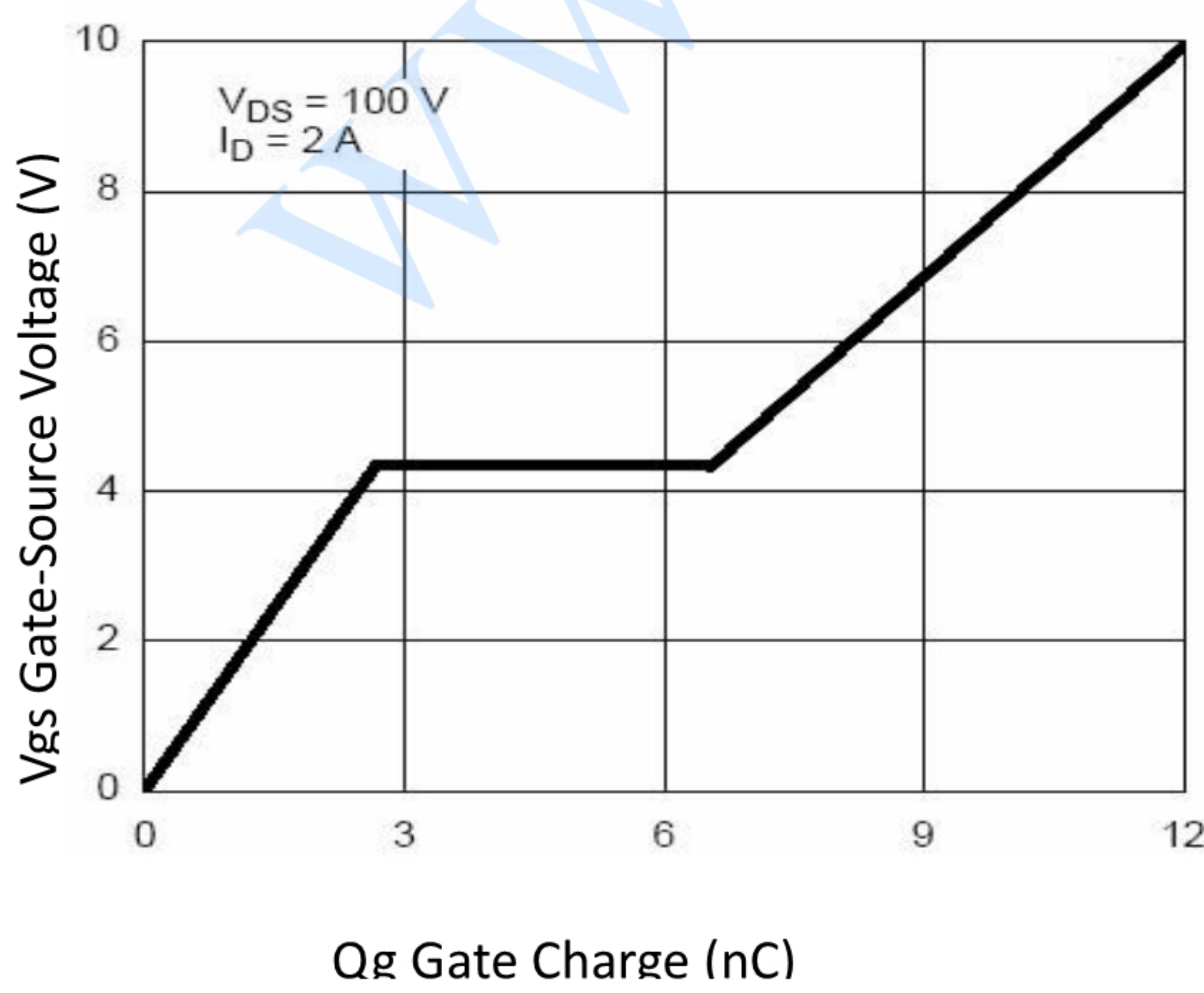
Transfe Characteristics



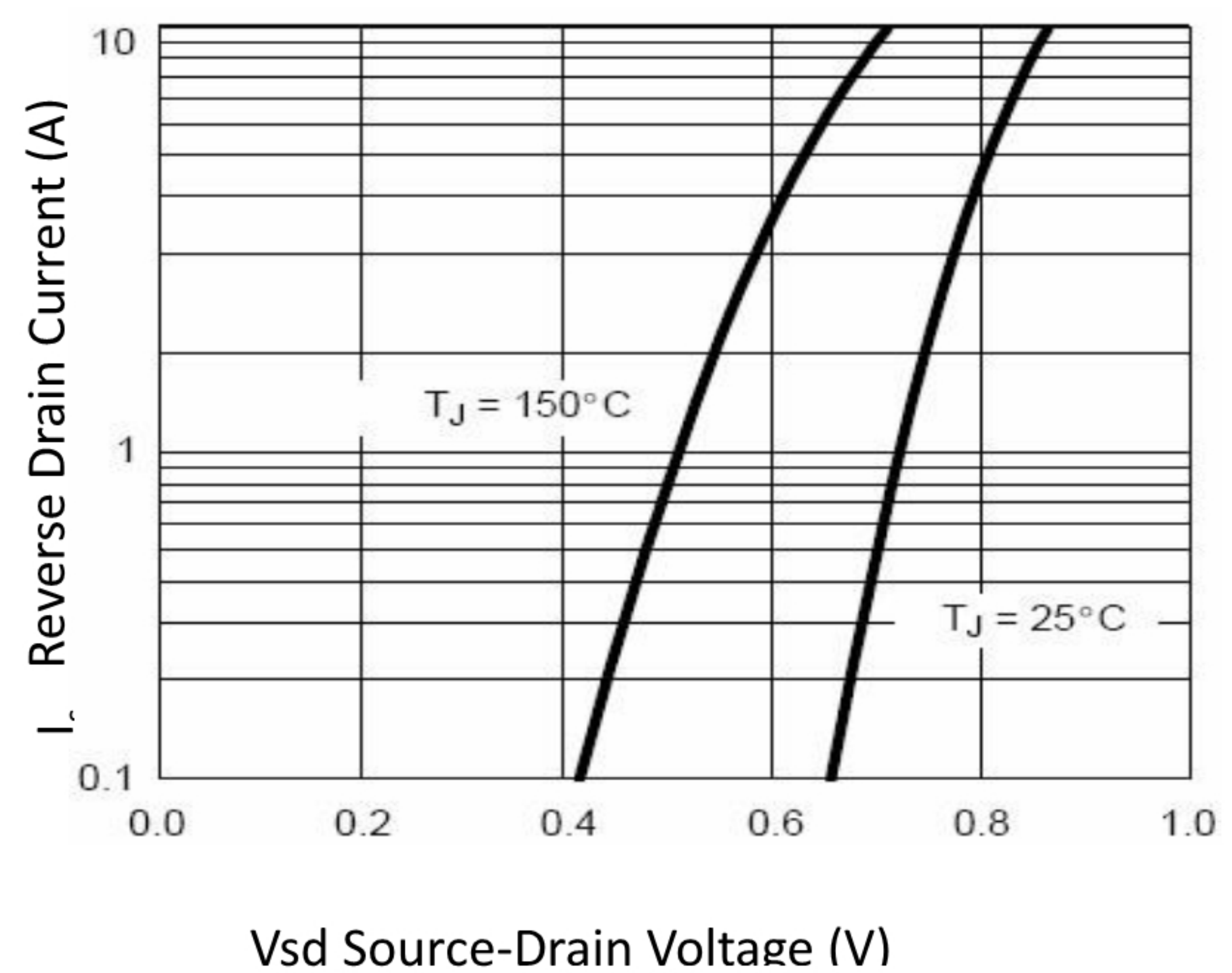
RDSON vs. Drain Current



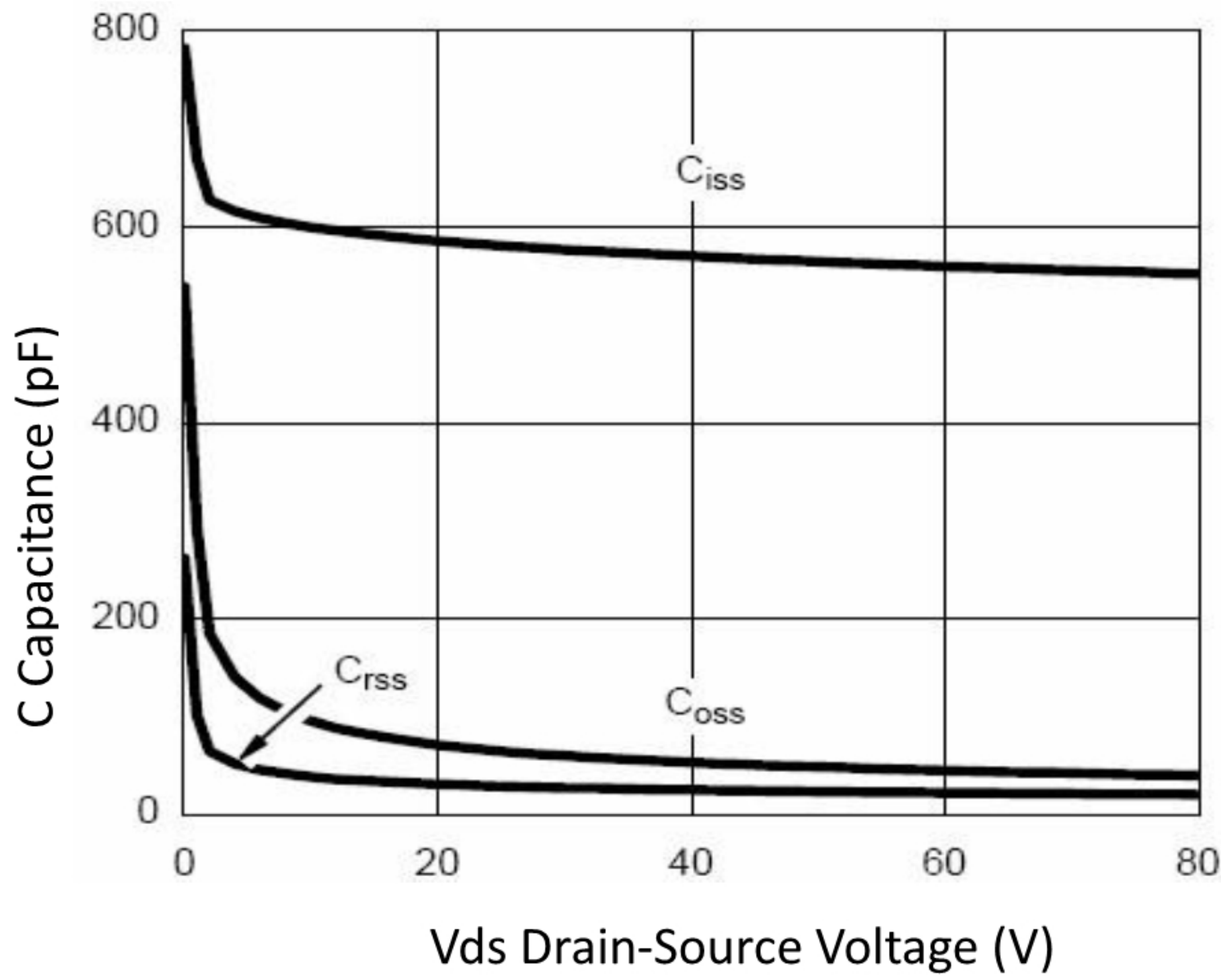
Rdson Junction Temperature



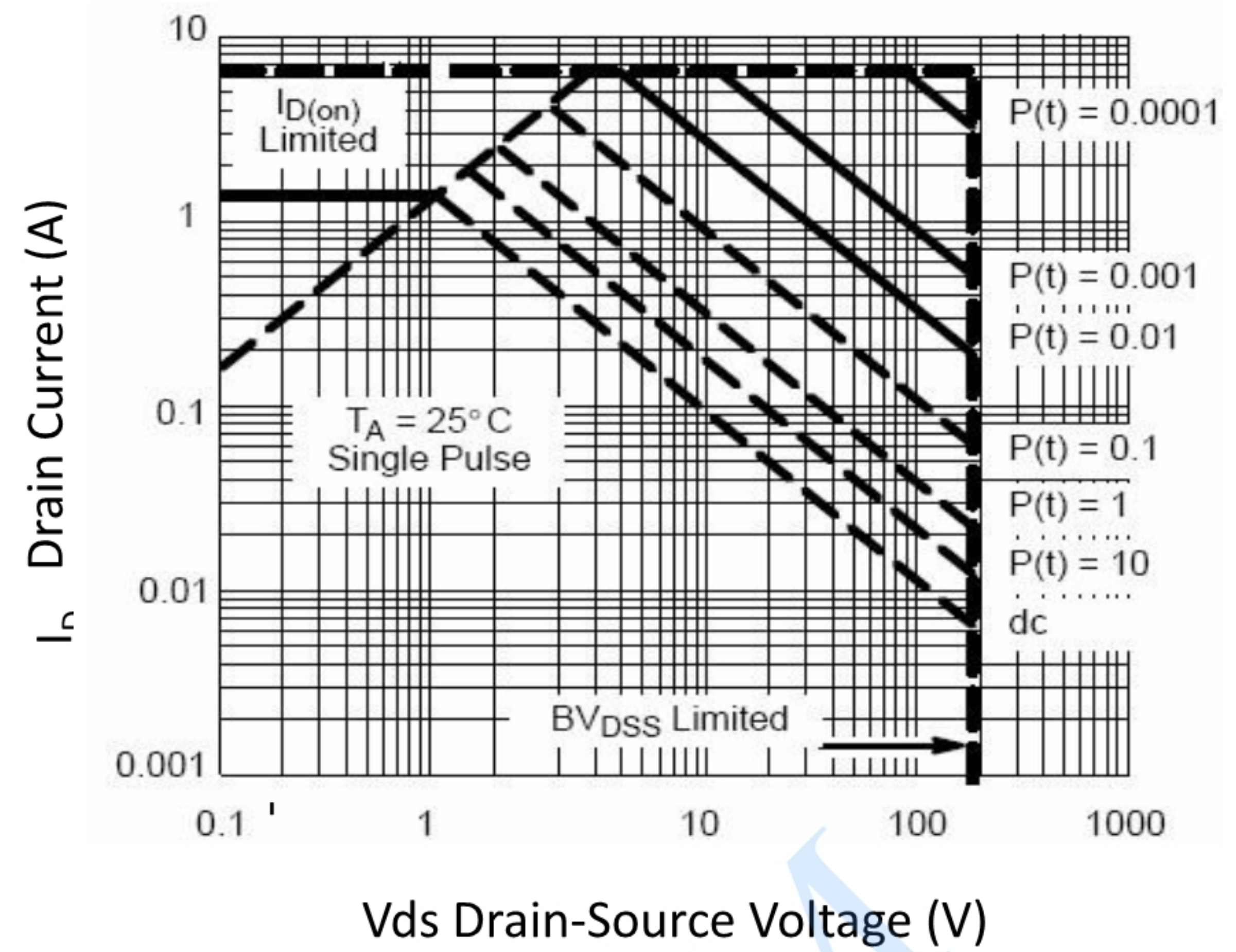
Gate Charge



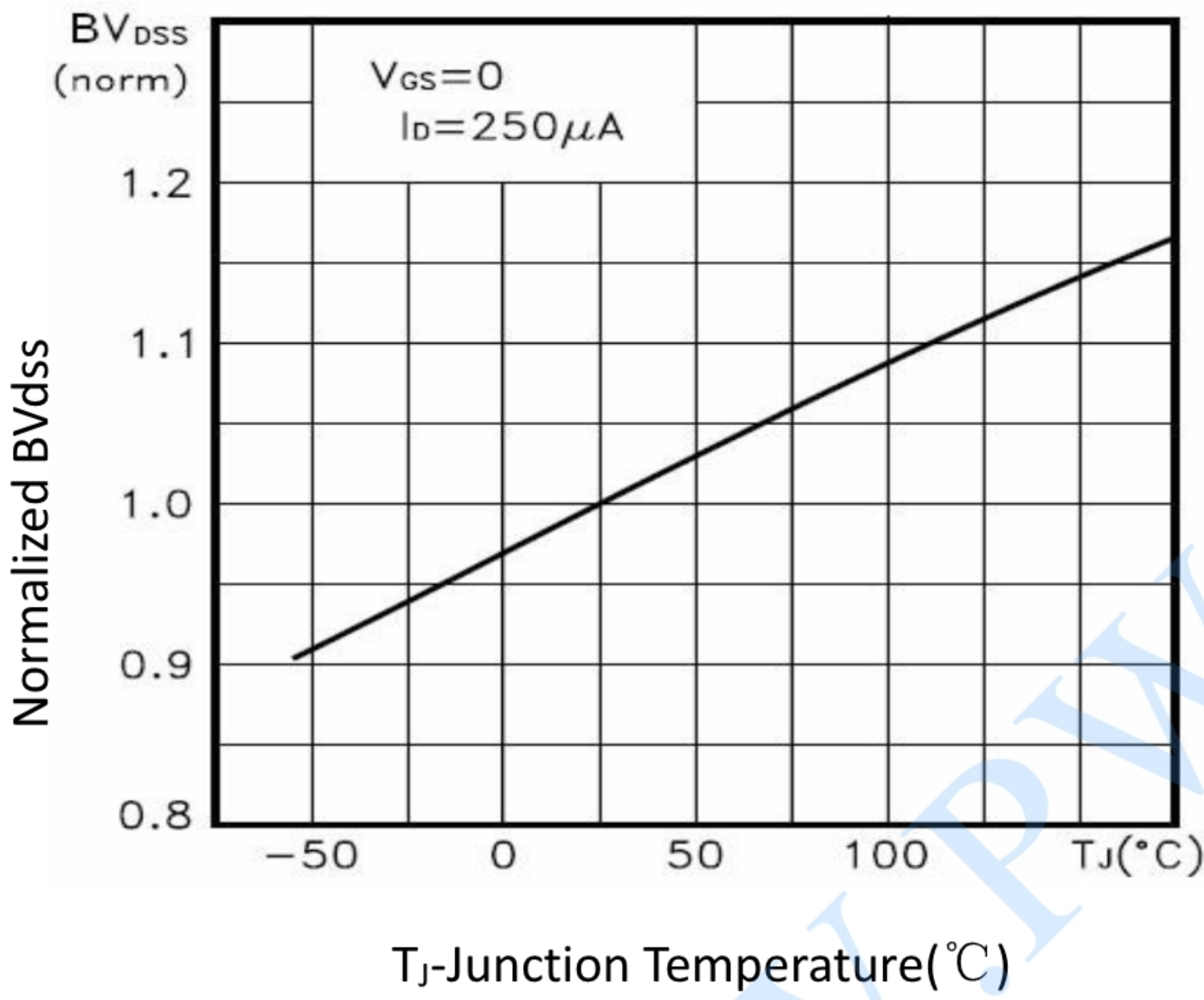
Source- Drain Diode Forward



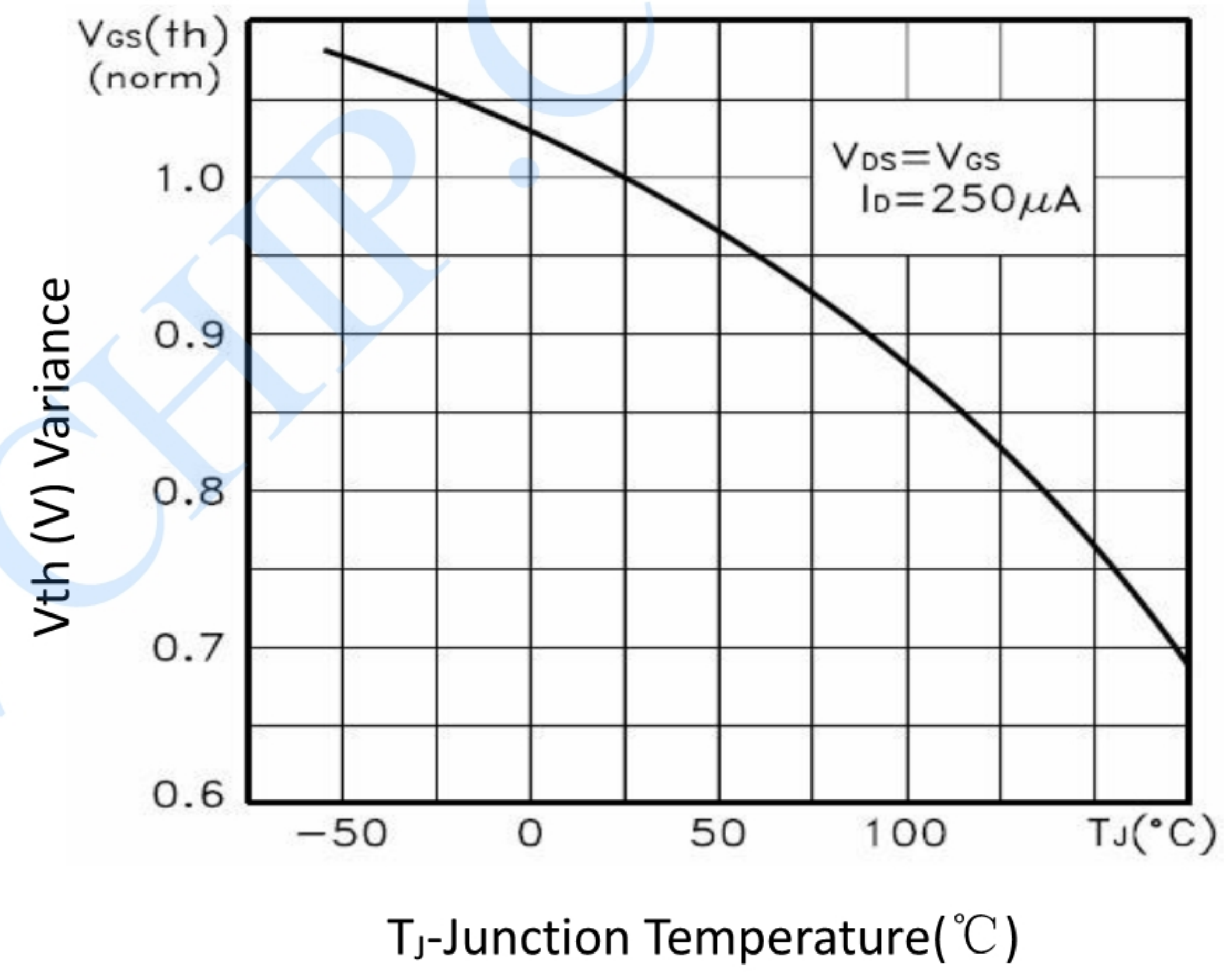
Capacitance vs Vds



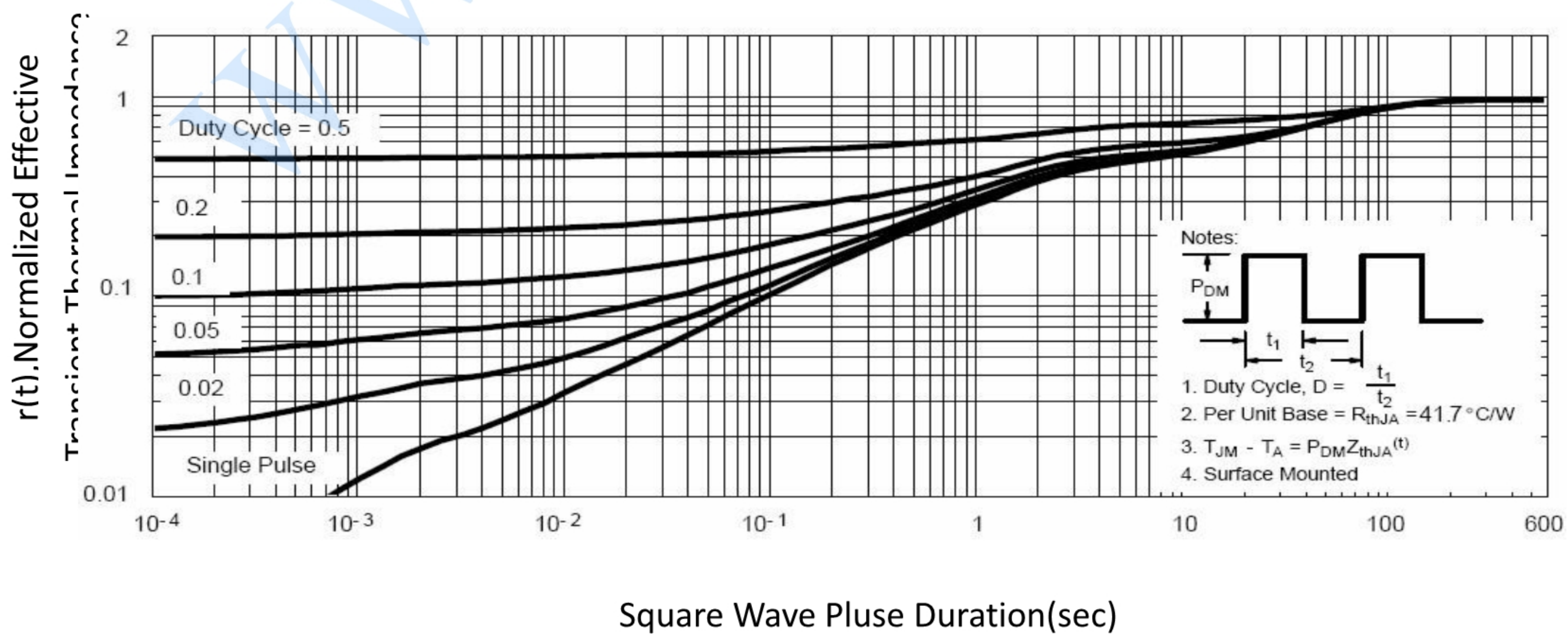
Safe Operation Area



BVDSS vs Junction Temperature



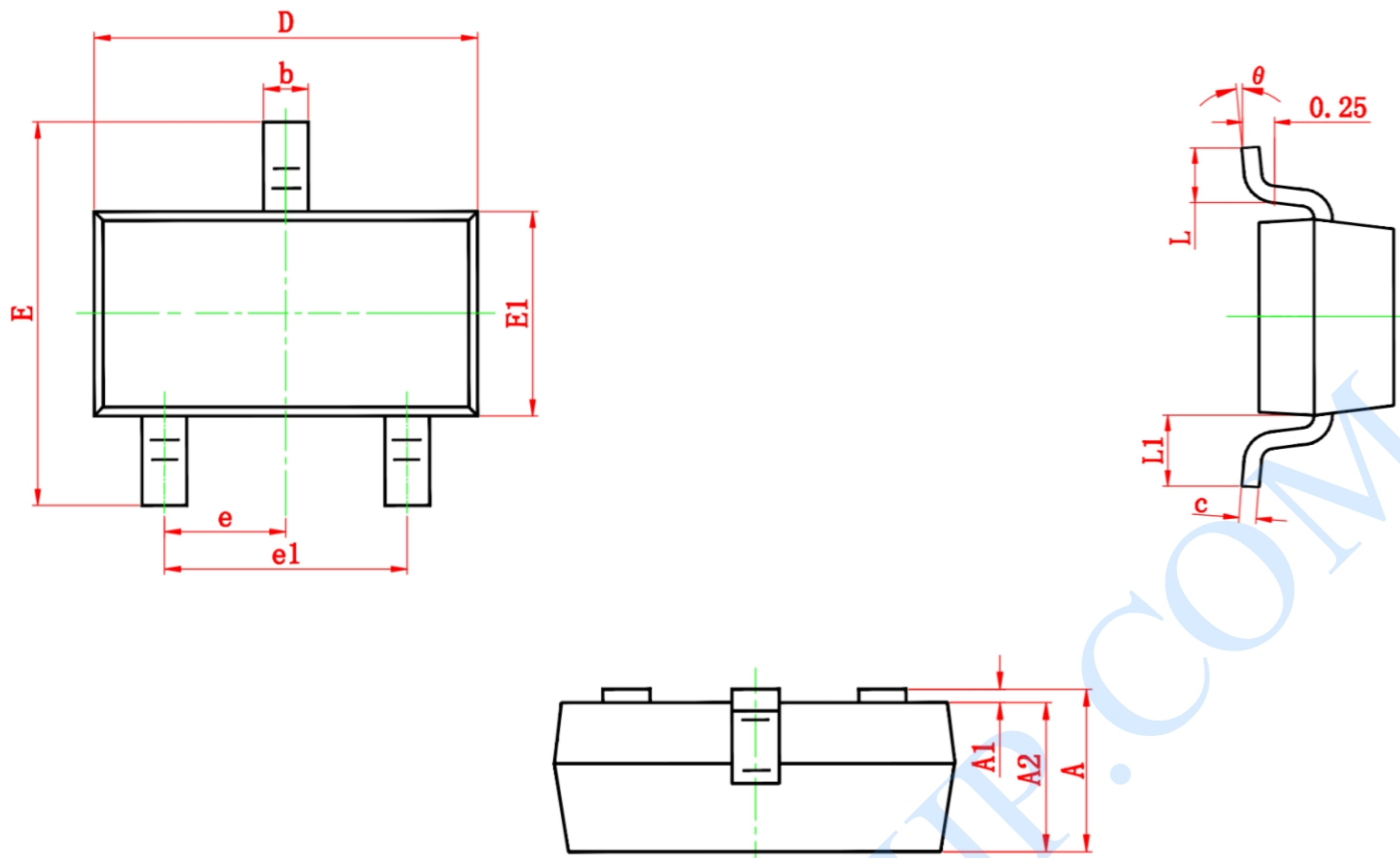
VGS(th) vs Junction Temperature



Normalized Maximum Transient Thermal Impedance

PACKAGE DESCRIPTION

SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	2.250	2.550	0.089	0.100
E1	1.200	1.400	0.047	0.055
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.300	0.500	0.012	0.020
L1	0.550 REF.		0.022 REF.	
θ	0°	8°	0°	8°

Notes

- All dimensions are in millimeters.
- Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
- Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
- Dimension L is measured in gauge plane.
- Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.



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