

## NCE N-Channel Enhancement Mode Power MOSFET

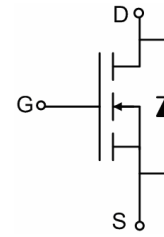
### General Features

- $V_{DS} = 60V, I_D = 0.115A$   
 $R_{DS(ON)} < 3.5\Omega @ V_{GS}=5V$   
 $R_{DS(ON)} < 3\Omega @ V_{GS}=10V$

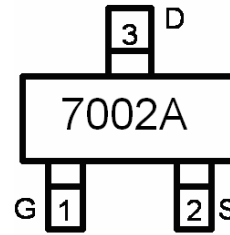
- Lead free product is acquired
- Surface mount package

### Application

- Direct logic-level interface: TTL/CMOS
- Drivers: relays, solenoids, lamps, hammers, display, memories, transistors, etc.
- Battery operated systems
- Solid-state relays



Schematic diagram



Marking and pin assignment



SOT-23 top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7002A	2N7002A	SOT-23	Ø180mm	8 mm	3000 units

### Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous@ Current-Pulsed <sup>(Note 1)</sup>	$I_D$	0.115	A
	$I_{DM}$	0.8	A
Maximum Power Dissipation	$P_D$	0.2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	625	°C/W
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### Electrical Characteristics (TC=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	68	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA

Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=5V, I_D=0.05A$	-	2.3	3.5	$\Omega$
		$V_{GS}=10V, I_D=0.5A$	-	2.1	3	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=0.2A$	0.08	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	20	50	PF
Output Capacitance	$C_{oss}$		-	10	20	PF
Reverse Transfer Capacitance	$C_{rss}$		-	3.6	5	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=0.2A$ $V_{GS}=10V, R_{GEN}=10\Omega$	-	10	-	nS
Turn-on Rise Time	$t_r$		-	50	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=0.115A,$ $V_{GS}=4.5V$	-	1.7	3	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=0.115A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	0.115	A

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

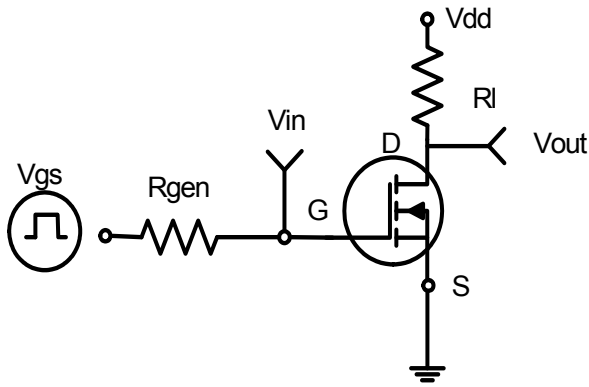


Figure 1: Switching Test Circuit

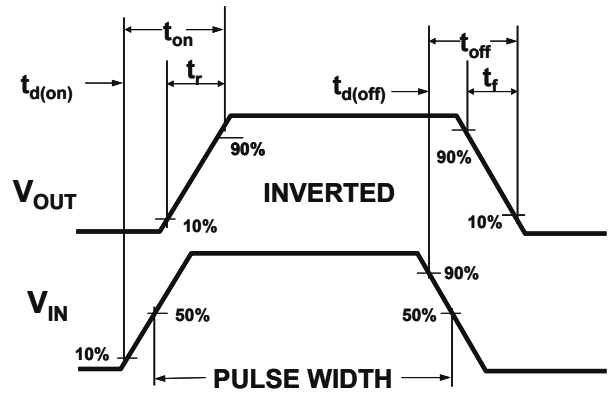


Figure 2: Switching Waveforms

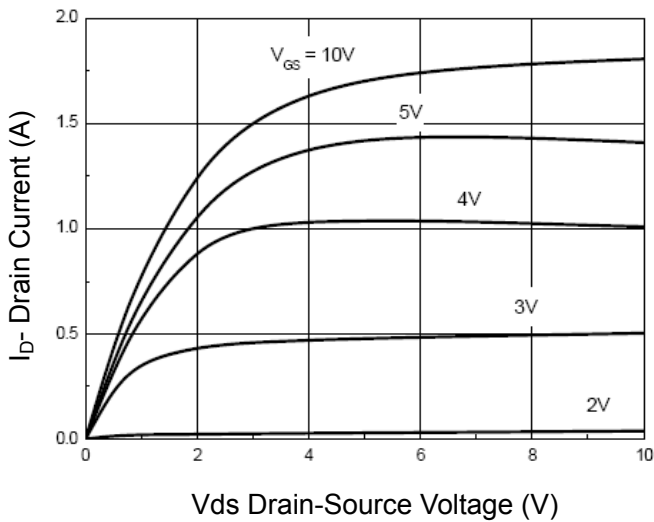


Figure 3 Output Characteristics

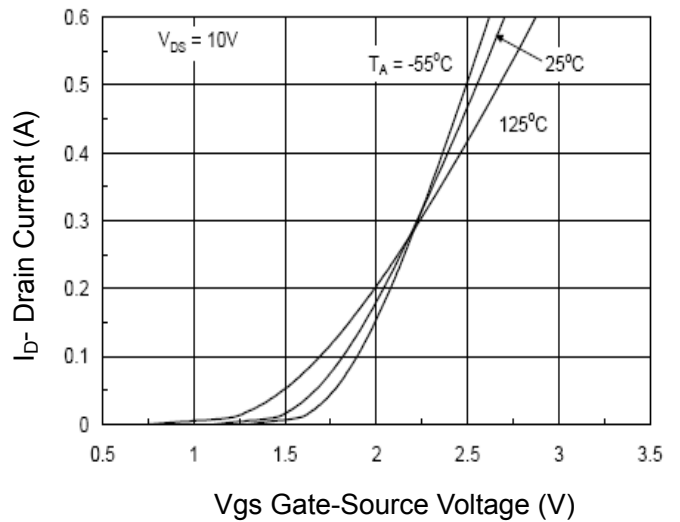


Figure 4 Transfer Characteristics

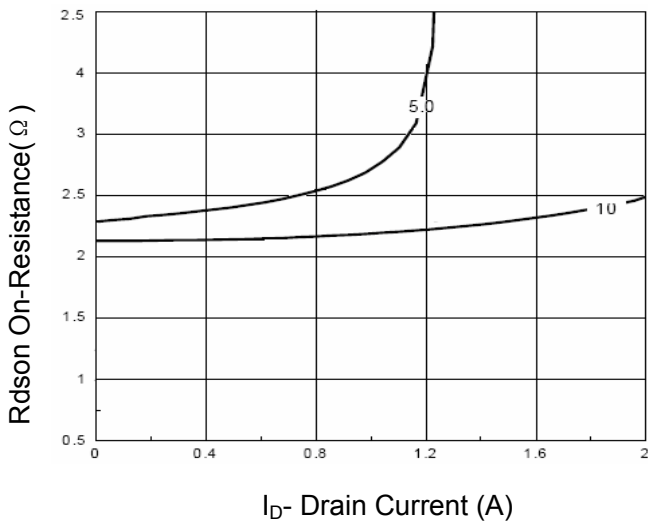


Figure 5 Drain-Source On-Resistance

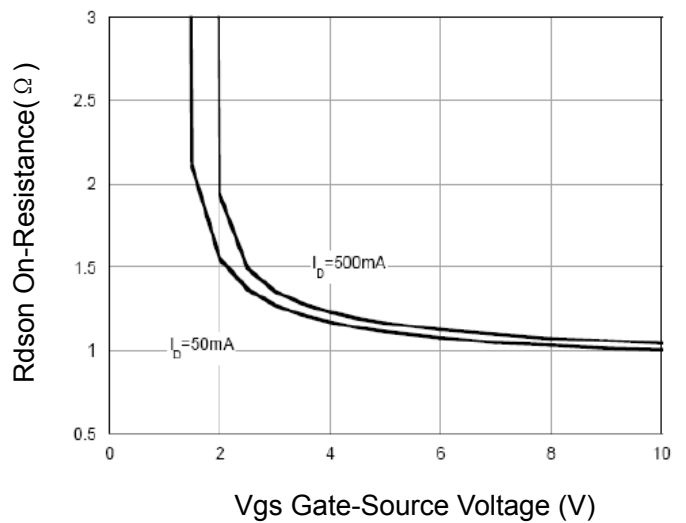
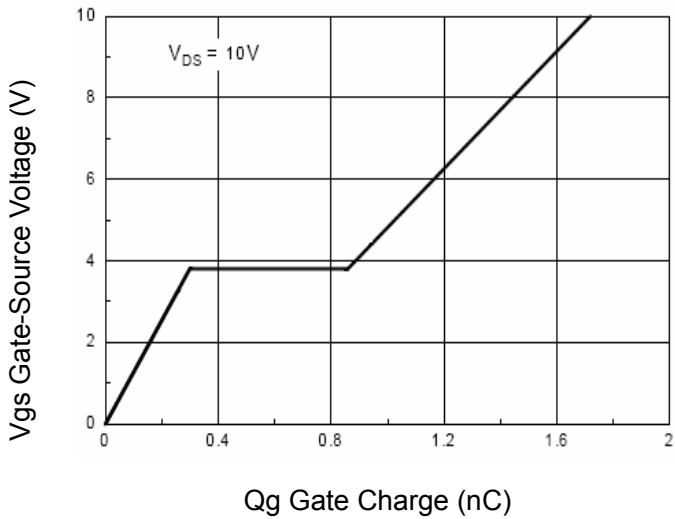
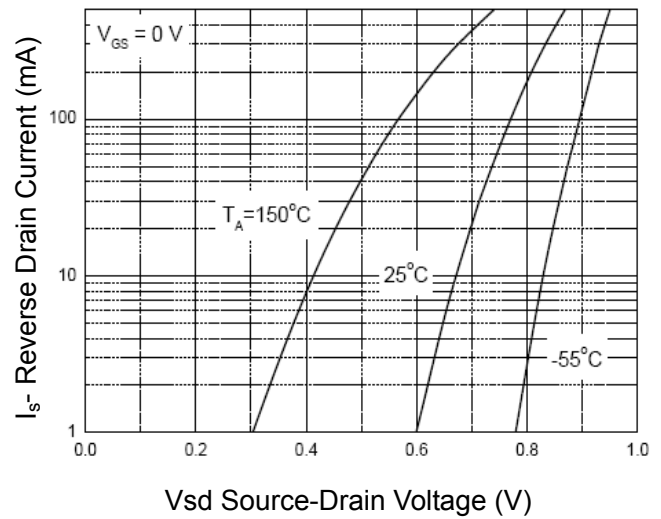


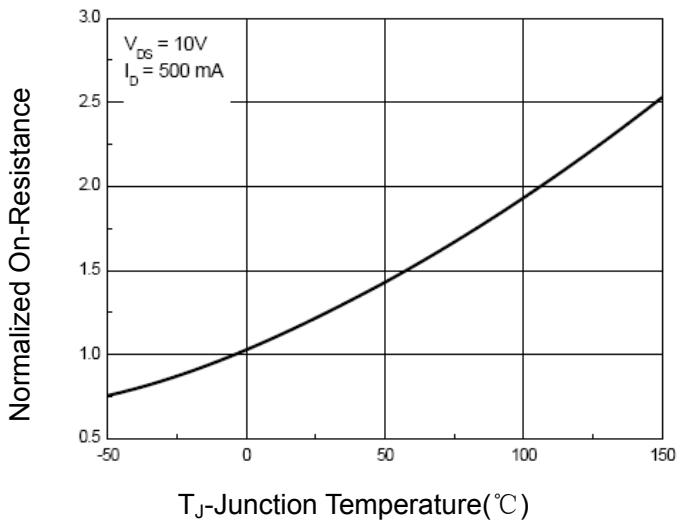
Figure 6 Rdson vs Vgs



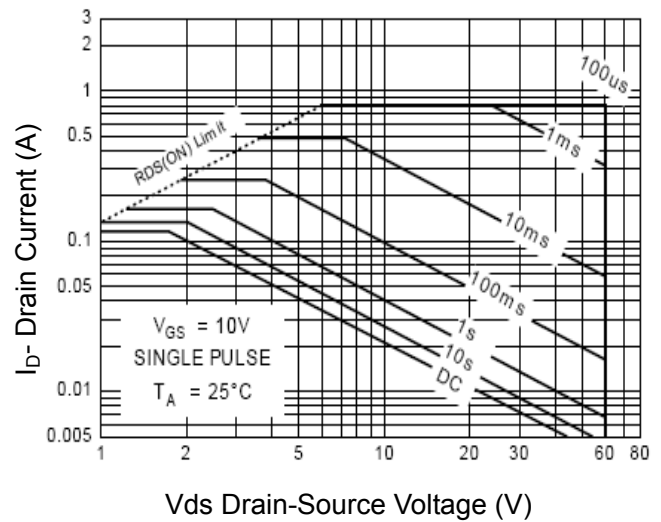
Qg Gate Charge (nC)  
**Figure 7 Gate Charge**



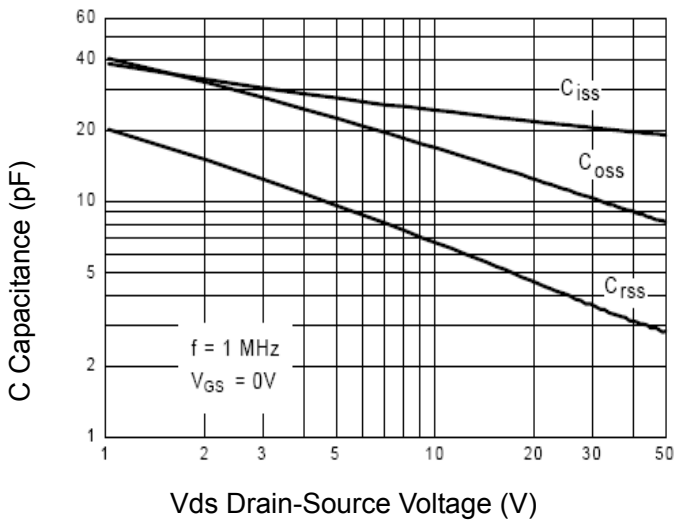
Vsd Source-Drain Voltage (V)  
**Figure 8 Source-Drain Diode Forward**



TJ-Junction Temperature(°C)  
**Figure 9 Drain-Source On-Resistance**



Vds Drain-Source Voltage (V)  
**Figure 10 Safe Operation Area**



Vds Drain-Source Voltage (V)  
**Figure 11 Capacitance vs Vds**

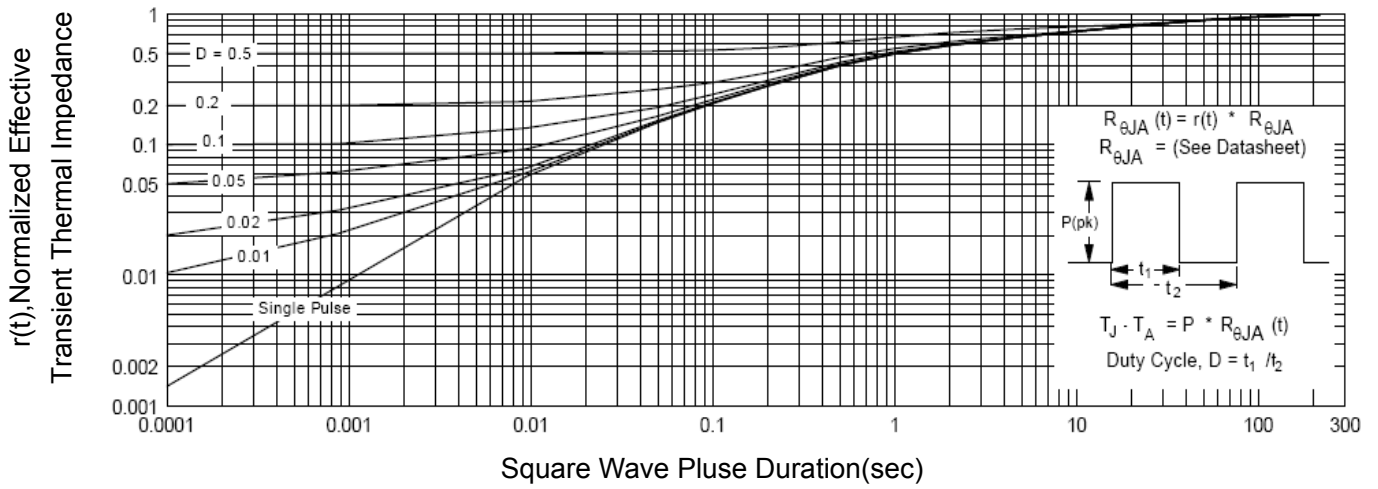
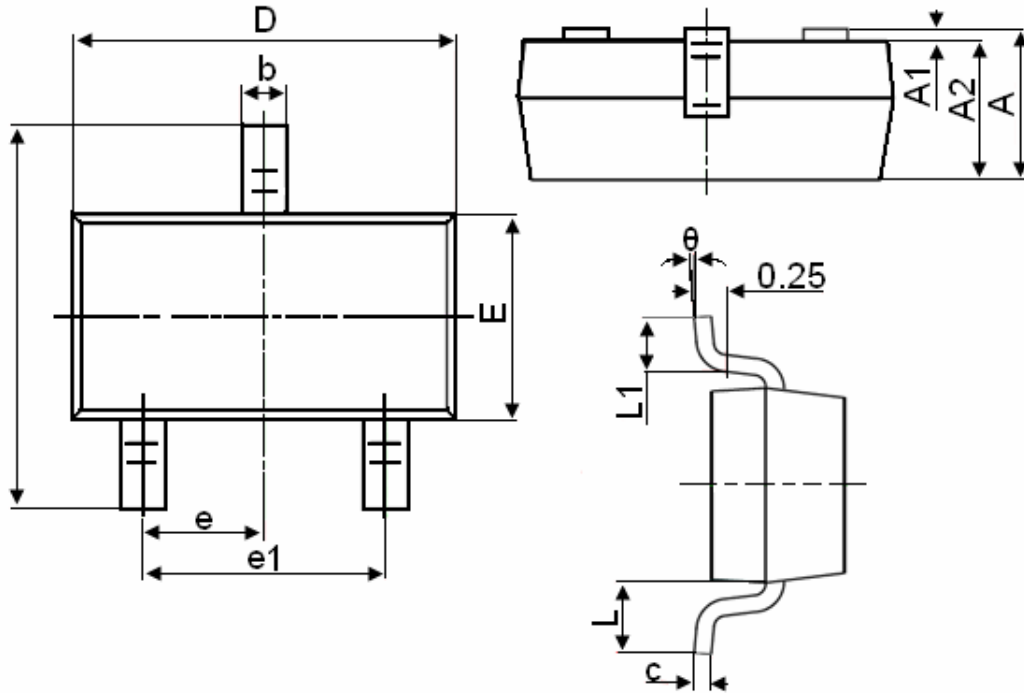


Figure 12 Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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