



2A , 4.5V-22V Input , 4.2V/4.35V Cell Switching Charger

GENERAL DESCRIPTION

PW4203A is a 4.0-22V input, 2A single-cell synchronous buck Li-Ion battery charger, suitable for portable application. VSET pin is convenient for different cell voltage. Integrated 800 kHz synchronous buck regulator consists of 25V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

The PW4203A is available in an 8-pin SOP package, provides a very compact system solution and good thermal conductance.

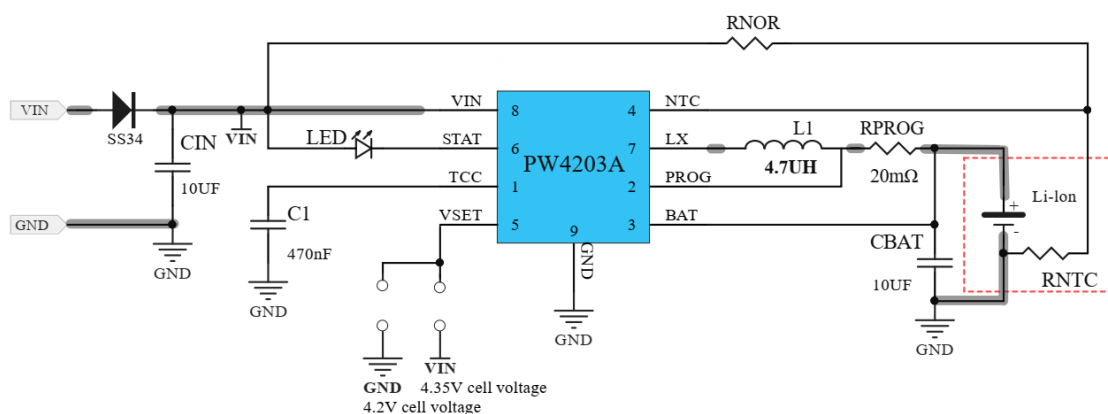
FEATURES

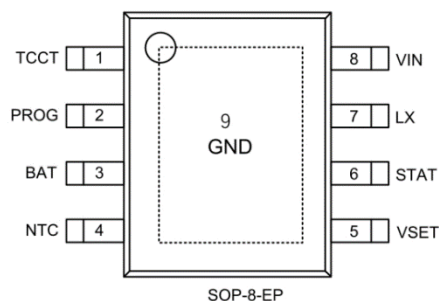
- Adaptive input current limit
- Programmable Charging Timeout
- Input Voltage Range: 4.0V to 22V
- ADJ (2A MAX) Constant Charge Current
- Input Voltage UVLO and Battery OVP
- Normal Synchronous Buck Operation when Battery Removed
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- SOP-8 Exposed Pad Packag

APPLICATIONS

- Cellular Telephones,
- PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players

TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT/DESCRIPTION


Pin Number	Pin Name	Function
1	TCCT	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/9 of CC charge time.
2	PROG	Charge current program pin. Connect a current sense resistor from PROG pin to BAT pin. Average charge current is detected for both TC mode and CC mode.
3	BAT	Battery positive pin
4	NTC	Thermal protection pin. UTP threshold is about 75%VIN and OTP threshold is about 30%VIN. Pull up to VIN can disable charge logic and make the IC operate as normal buck regulator. Pull down to ground can shutdown the IC.
5	VSET	Pull down for 4.2V cell voltage, pull high for 4.35V cell voltage.
6	STAT	Charge status indication pin. It is open drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, LED is off.
7	LX	Switch node pin. This pin connects the drains of the integrated main and synchronous power MOSFET switches. Connect to external inductor.
8	VIN	Positive power supply input pin. VIN ranges from 4V to 22V for normal operation. It has UVLO function and must be 120mV greater than the battery voltage to enable normal operation.
9	GND	Exposed Pad, Ground pin.



Absolute Maximum Ratings (note1)

Parameter	VALUE	Unit
VSET, NTC, STAT	-0.5-32	V
VIN, BAT, LX	-0.5- 25	V
TCCT	-0.5- 3.6	V
PROG	BAT-0.3~BAT+0.3	V
LX Pin current continuous	2.5	A
Power Dissipation, PD @ TA = 25°C	3.3	W
Package Thermal Resistance (Note 2)	θ_{JA}	30 °C/W
	θ_{JC}	20 °C/W
Junction Temperature Range	-40 to 125	°C
Lead Temperature (Soldering, 10 sec.)	260	°C
Storage Temperature Range	-65 to 125	°C

RECOMMENDED OPERATING Conditions (note3)

Parameter	VALUE
VSET, NTC, STAT	less than 32V
VIN, BAT, LX	less than 25V
TCCT	less than 3.6V
PROG	in the range of BAT-0.1V ~ BAT+0.1V
Pin current continuous	less than 2A
Junction Temperature Range	-20°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Layout Considerations

The layout design of PW4203 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: CIN, L, R1 and R2.

1. It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2. CIN must be close to Pins VIN and GND. The loop area formed by CIN and GND must be minimized.
3. The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
4. The capacitor C1 and the trace connecting to the TCCT pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem. It should be better to ground C1 to the output Capacitor's ground



ELECTRICAL CHARACTERISTICS

(TA=25°C, VIN=15V, GND=0V, CIN=10uF, L1=2.2uH, RPROG=25mΩ, C1=470nF, unless otherwise specified.)

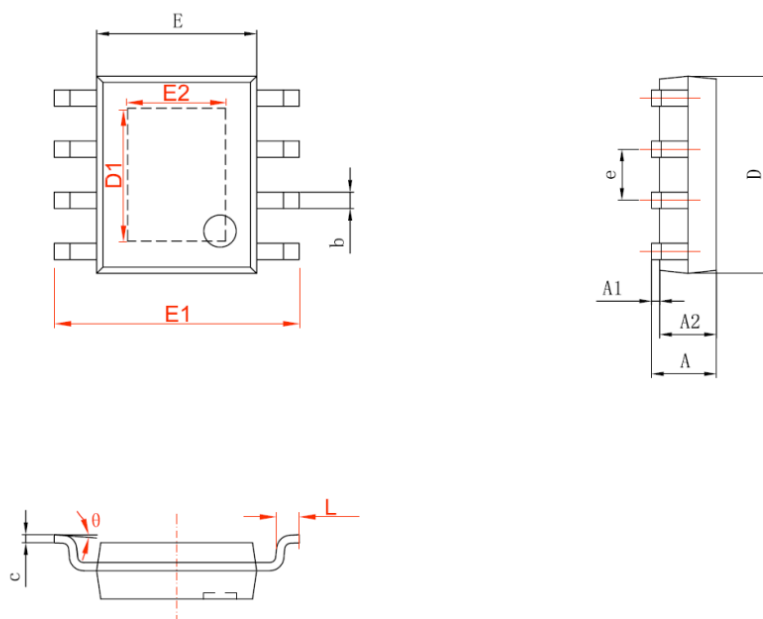
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN	Supply voltage		4.5		22	V
VUVLO	VIN under voltage lockout threshold	VIN rising and measured from VIN to GND			3.9	V
ΔVUVLO	VIN under voltage lockout hysteresis	Measured from VIN to GND		190.		mV
VOVP	Input overvoltage protection	VIN rising and measured from VIN to GND	23			V
ΔVOVP	Input overvoltage protection hysteresis	Measured from VIN to GND		750		mV
IBAT	Battery discharge current	NTC pull down to GND			25	uA
IIN	Input quiescent current	Disable Charge			1.5	mA
fOSC	Oscillator frequency		640	800	960	kHz
D	PFET duty cycle				100	%
RNFET	RDS(ON) of N-FET			150		mΩ
RPFET	RDS(ON) of P-FET			160		mΩ
Vcv	4.2V cell voltage CV charge mode	0°C ≤ TA ≤ 70°C	4.16	4.20	4.24	V
	4.35V cell voltage CV charge mode		4.3	4.35	4.4	V
ΔVRCH	4.2V cell Voltage threshold for Recharge	0°C ≤ TA ≤ 70°C	50	100	150	mV
	4.35V cell Voltage threshold for Recharge		100	150	200	mV
VTRK	Single-cell TC charge mode voltage threshold	0°C ≤ TA ≤ 70°C	2.2	2.5	2.8	V
VDET	Detect voltage threshold	VSHOT < VBAT < VRCH	80%		90%	VIN
tDET	Detect delay time	VSHOT < VBAT < VRCH	30	35	40	mS
	Internal charge current accuracy for Constant Current Mode	ICC=25mV/Rprog	-10		10	%
	Internal charge current accuracy for Trickle Current Mode	ITC=2.5mV/Rprog	-50		50	%
VOVP	Output voltage OVP threshold		105%	110%	115%	VCV
ITERM	Charge Termination Current	VBAT falling edge		10%		ICC
VINSL	VIN voltage falling threshold at high current			4.6		V
ΔVINSL	VIN voltage hysteresis at high current			50		mV
ΔV	VIN voltage falling threshold at high current			4.4		V
ΔVINQK	VIN voltage hysteresis at high current			100		mV
fFBK	Frequency fold back	VBAT < 2V		12.5%		fOSC
ILM	Power FET current limit			4.0		A
TTC	Trickle current charge timeout	C1=330nF	0.425	0.5	0.575	hour
TCC	Constant current charge timeout	C1=330nF	3.825	4.5	5.175	hour
TMC	Charge mode change delay time			30		ms
TTERM	Termination delay time			30		ms
TRCHG	Recharge time delay			30		ms



UTP	Under temperature protection		70%	75%	80%	VIN
	Under temperature protection hysteresis	Falling edge		5%		VIN
OTP	Over temperature protection		28%	30%	32%	VIN
	Over temperature protection hysteresis	Rising edge		2%		
ΔV_{ASD}	ASD voltage threshold hysteresis	Measured from VIN to VBAT		80		mV

PACKAGE DESCRIPTION

SOP8-EP



字符	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

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