DP4T Antenna Cross Switch with MIPI 2.1

Features

- Low insertion loss: 1.0 dB typical @ 5.0 GHz
- High isolation: 30 dB typical @ 5.0 GHz
- High power handling capability of up to 38 dBm
- Broadband frequency range: 0.1 to 5 GHz
- MIPI RFFE V2.1 interface
- Single VIO supply
- No DC blocking capacitors in typical application
- Small WBQFN 2.0mm x 2.0mm x 0.55 mm -16L package

Applications

- Antenna routing switch for cellular devices
- Cellular Modems , Tablets and USB Devices
- GSM/CDMA/WCDMA/LTE and NR including n77, n78, n79 bands

General Description

The AW12024T is a dual-pole four-throw switch with low insertion loss, high Isolation and high power capability. It is suitable for multi-mode LTE and 5G NR quadruple antenna applications.

The AW12024T is perfectly compatible with MIPI RFFE V2.1 control interface operating in 1.65 to 1.95V voltage range. It is provided in a compact 2.0mm x 2.0mm x 0.55mm size, 16-pin WBQFN package.

Typical Application Circuit

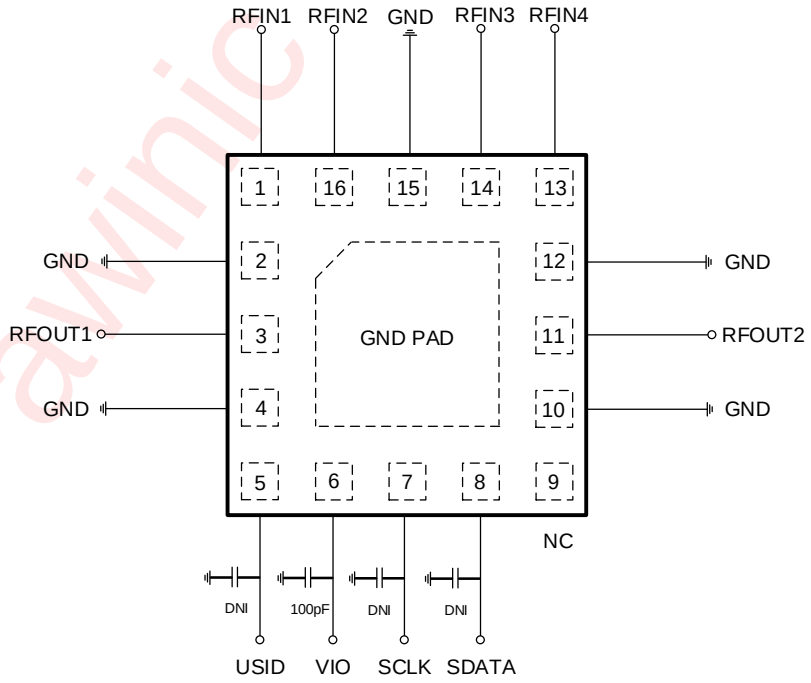


Figure 1 Typical Application Circuit of AW12024TQNR

Pin Configuration And Top Mark

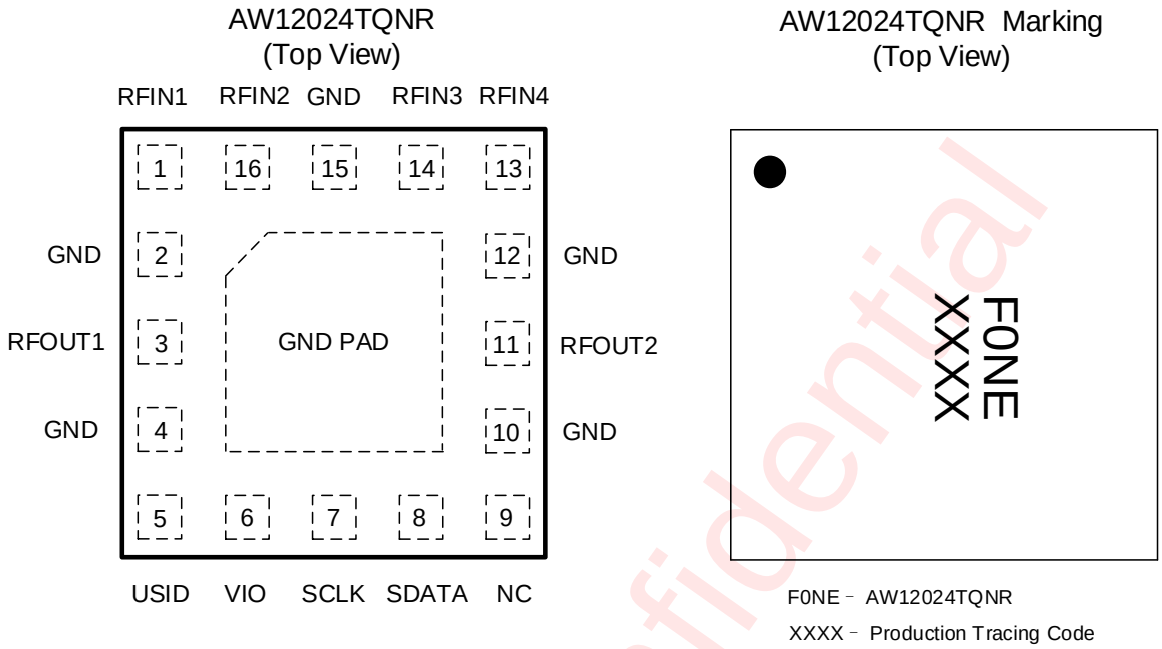


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RFIN1	RF input port 1
2	GND	Ground
3	RFOUT1	RF output port 1
4	GND	Ground
5	USID	MIPI USID select port
6	VIO	Supply voltage for MIPI
7	SCLK	MIPI clock
8	SDATA	MIPI data input/output
9	NC	NC
10	GND	Ground
11	RFOUT2	RF output port 2

12	GND	Ground
13	RFIN4	RF input port 4
14	RFIN3	RF input port 3
15	GND	Ground
16	RFIN2	RF input port 2
17	GND	Ground

Functional Block Diagram

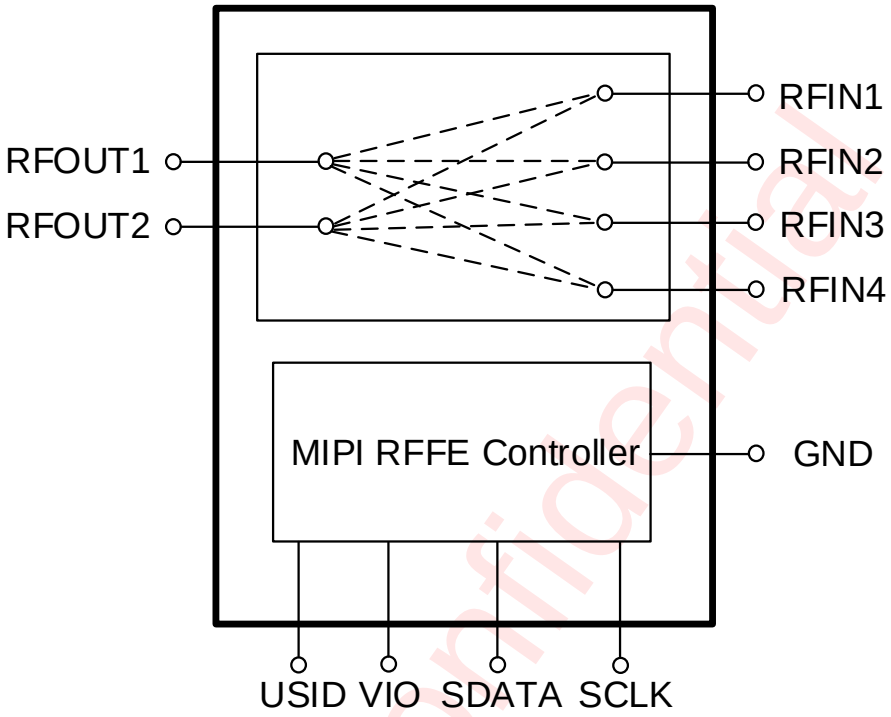


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW12024TQNR	-40°C～85°C	WBQFN 2.0mm x 2.0mm x 0.55 mm -16L	F0NE	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings (NOTE 1)

PARAMETERS	RANGE
Supply Voltage VIO for MIPI	-0.3V to 2.5V
Interface Control Voltage Range SDATA, SCLK	-0.3V to 2.5V
RF input power	38.5dBm
Operating Free-air Temperature Range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM(Human Body Model)(NOTE 2)	±1000V
CDM (Charged Device Model) (NOTE 3)	±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Electrical Characteristics

V_{IO}=1.8V, P_{IN}=0dBm, VSWR=1:1,Temp=+25°C. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V_{IO}	Supply voltage for MIPI		1.65	1.8	1.95	V
I_{IO}	V_{IO} Supply Current	Active Mode		40	110	μA
		Low Power Mode		2	9	μA
V_{CTL_H}	SDATA,SCLK Control Voltage High	Must not exceed V_{IO} voltage	0.8* V_{IO}	V_{IO}	1.95	V
V_{CTL_L}	SDATA,SCLK Control Voltage Low	Must not exceed V_{IO} voltage	0	0	0.3*V_{IO}	V
T_{SW}	Time to switch between RF states	50% last SCLK falling edge to 90% RF signal		1.6	3	μs
RF Specifications						
IL	Insertion Loss (RFOUT1/2 to RFIN1/2/3/4)	617-960MHz		0.40	0.61	dB
		1425-2200MHz		0.45	0.74	dB
		2300-2690MHz		0.50	1.21	dB
		3300-3800MHz		0.75	1.44	dB
		3800-5000MHz		1.00	1.98	dB
RL	Return Loss(All RFIN/RFOUT Ports)	617-960MHz	15	25		dB
		1425-2200MHz	13	22		dB
		2300-2690MHz	12	20		dB
		3300-3800MHz	9	16		dB
		3800-5000MHz	6	10		dB
ISO ON-ON	RFOUT to RFOUT Ports	617-960MHz	30	49		dB
		1425-2200MHz	24	41		dB
		2300-2690MHz	21	35		dB
		3300-3800MHz	20	33		dB
		3800-5000MHz	18	30		dB
	RFIN to RFIN Ports	617-960MHz	30	49		dB
		1425-2200MHz	24	41		dB
		2300-2690MHz	21	40		dB
		3300-3800MHz	20	35		dB
		3800-5000MHz	19	30		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		617-960MHz	30	49		dB
	RFIN to RFOUT Ports	1425-2200MHz	25	41		dB
		2300-2690MHz	23	35		dB
		3300-3800MHz	22	33		dB
		3800-5000MHz	20	34		dB
ISO ON-OFF	RFOUT to RFOUT ports	617-960MHz	30	49		dB
		1425-2200MHz	24	42		dB
		2300-2690MHz	21	41		dB
		3300-3800MHz	20	38		dB
		3800-5000MHz	18	36		dB
	RFIN to RFIN Ports	617-960MHz	31	50		dB
		1425-2200MHz	26	49		dB
		2300-2690MHz	23	47		dB
		3300-3800MHz	21	40		dB
		3800-5000MHz	20	35		dB
	RFIN to RFOUT Ports	617-960MHz	31	50		dB
		1425-2200MHz	26	48		dB
		2300-2690MHz	23	45		dB
		3300-3800MHz	21	41		dB
		3800-5000MHz	21	35		dB
H2	Second Harmonics	Freq=900MHz, P_{IN}=+35dBm,CW		-60	-50	dBm
H3	Third Harmonics	Freq=900MHz, P_{IN}=+35dBm,CW		-58	-50	dBm
H2	Second Harmonics	Freq=1900MHz, P_{IN}=+35dBm,CW		-58	-50	dBm
H3	Third Harmonics	Freq=1900MHz, P_{IN}=+35dBm,CW		-48	-45	dBm
$P_{0.1dB}$	0.1dB Compression Point	All RFIN/RFOUT Ports		38		dBm

Power ON and OFF Sequence

1. Once V_{IO} is powered down to 0 V, wait at least 10 μs to reapply power to V_{IO}.

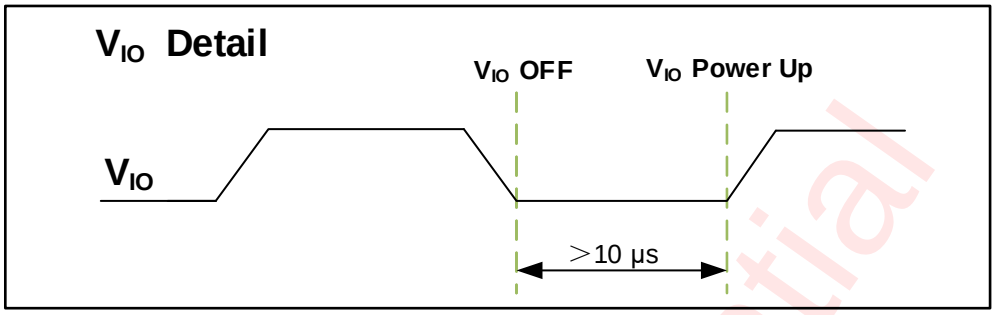


Figure 4 Digital Supply Detail

2. Before applying RF power , V_{IO} must be turned on for at least 20 μs.

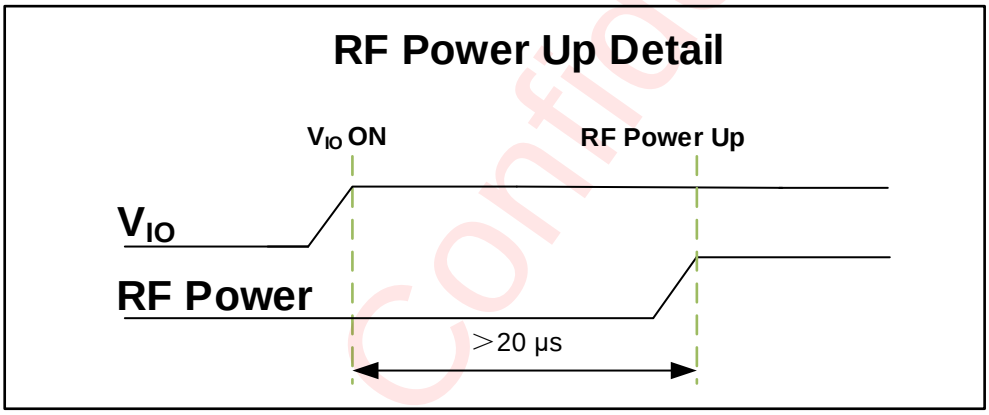


Figure 5 RF Power-Up Detail

3. Before sending SDATA/SCLK , V_{IO} must be applied for at least 800 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 10 μs to apply the RF signal.

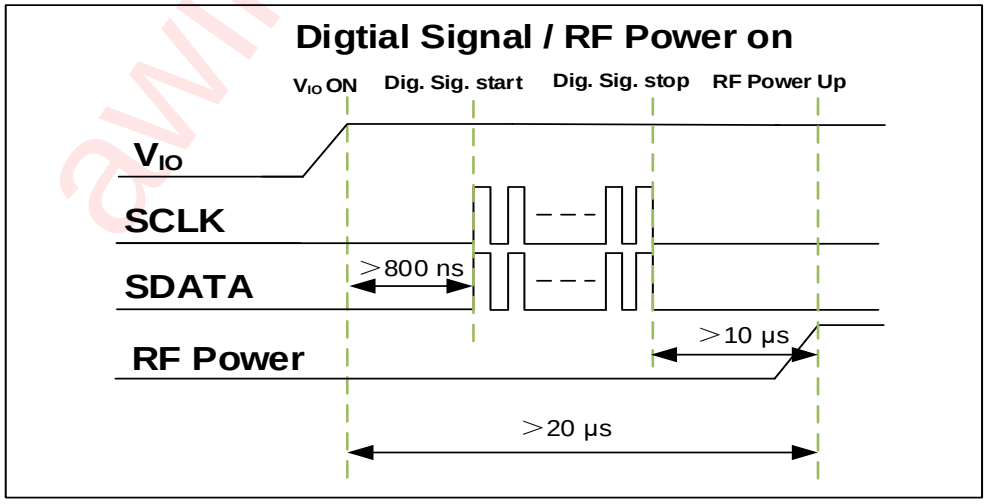


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

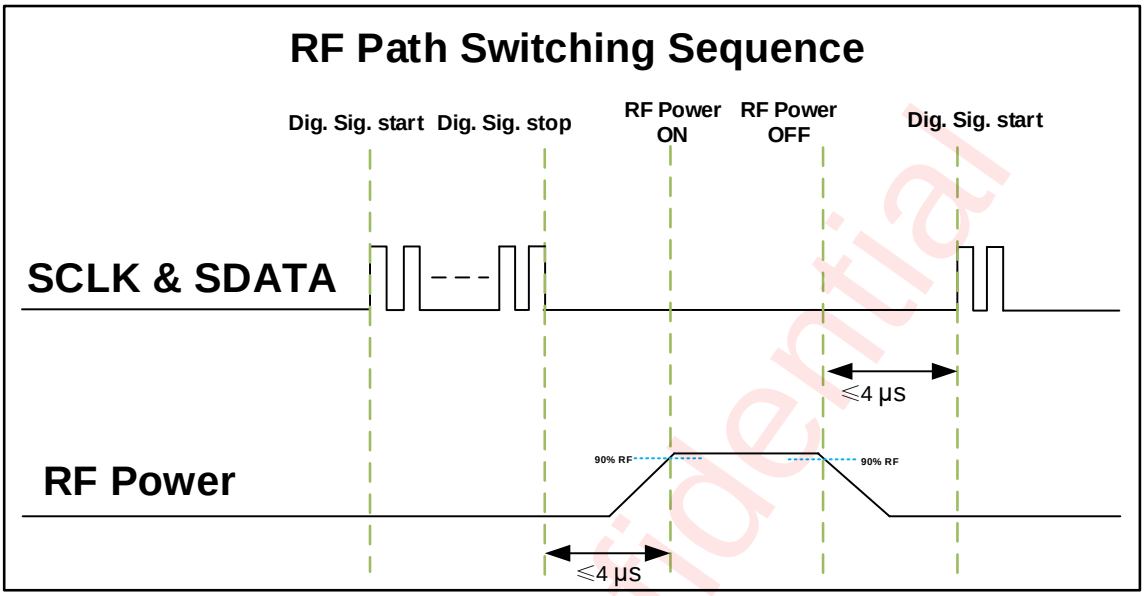


Figure 7 RF Path Switching Sequence

5. If “Lower Power Mode” is used, there must be a 10 µs delay before exiting “Lower Power Mode”.

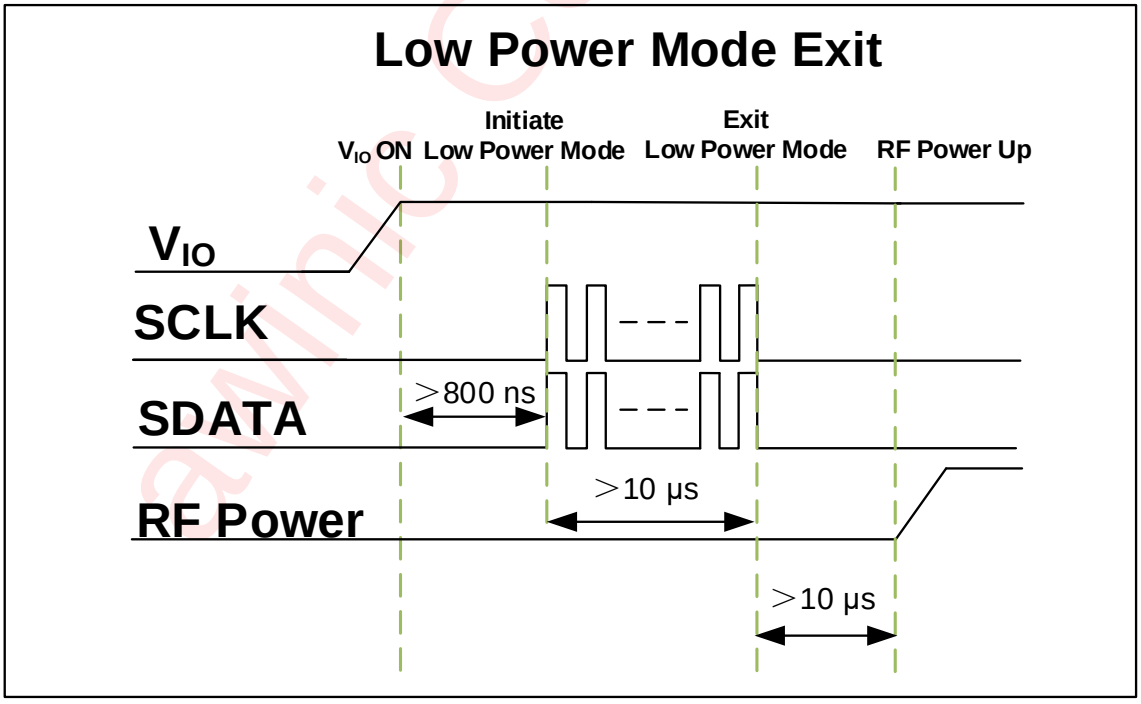


Figure 8 Lower Power Mode Exit Timing

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: USID select pin = 0→0x06 USID select pin = 1→0x07

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 write:

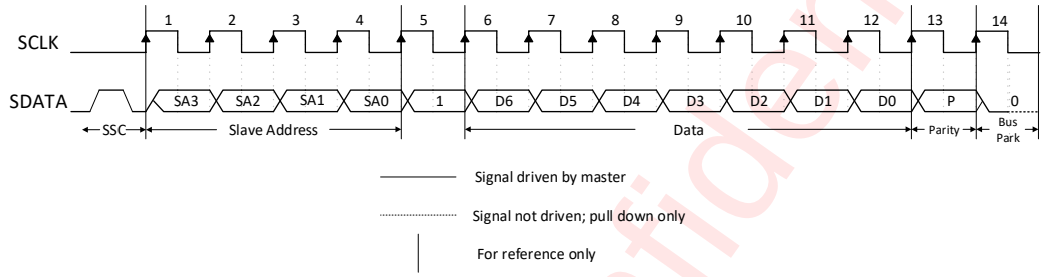


Figure 9 Register 0 write command sequence

Register write:

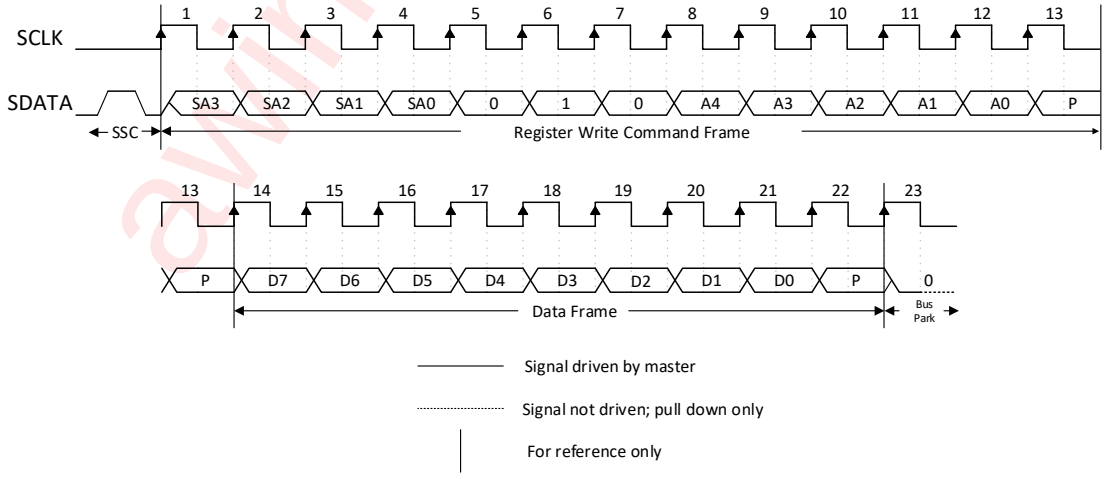


Figure 10 Register write command sequence

Register read:

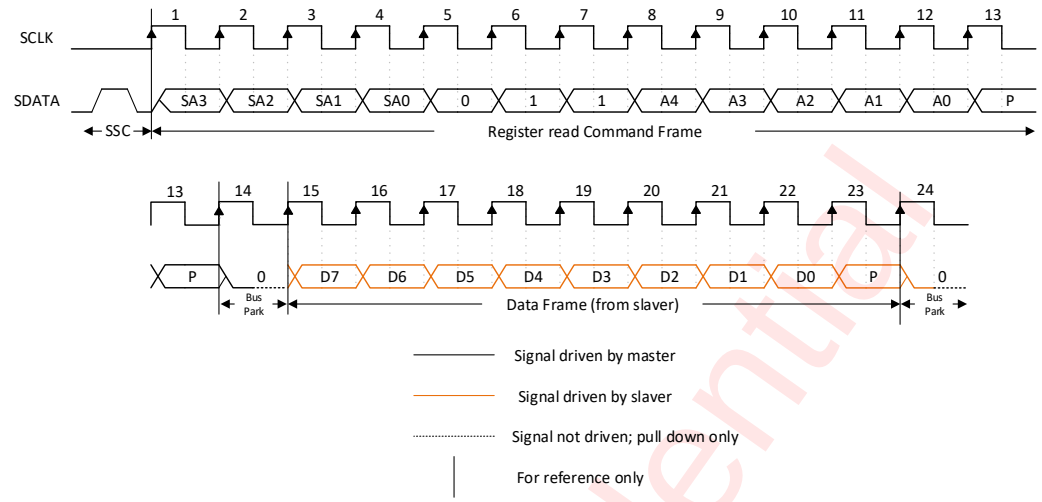


Figure 11 Register read command sequence

Extended Register write:

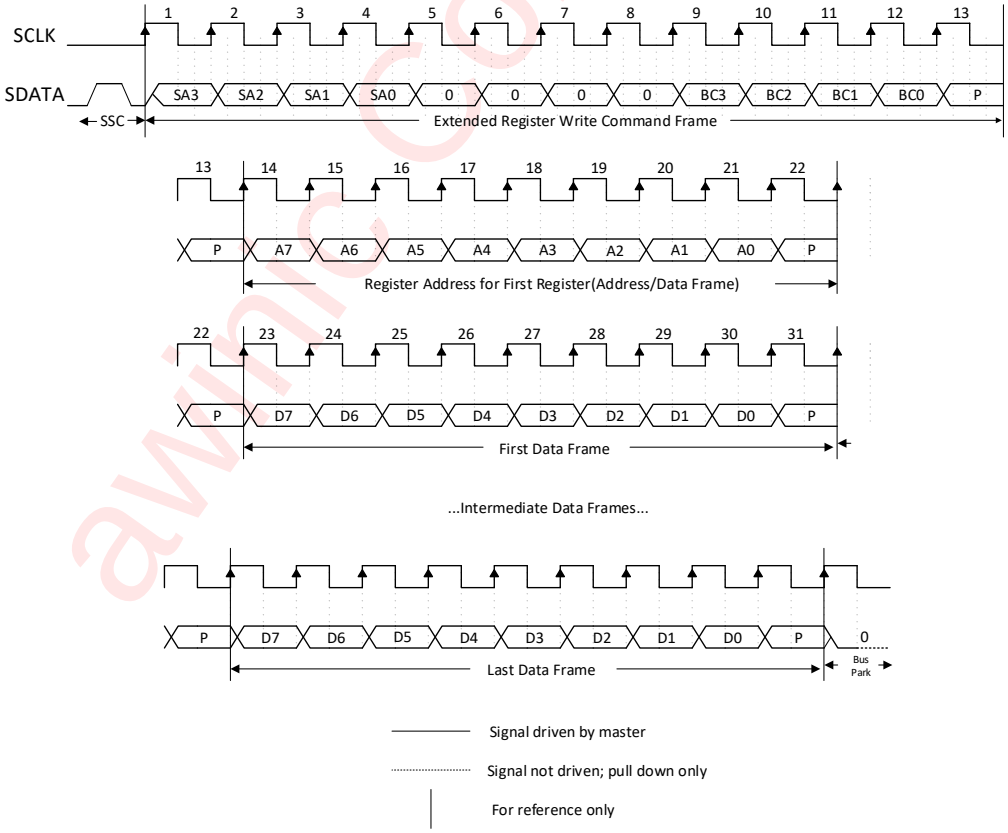


Figure 12 Extended Register write command sequence

Extended Register read:

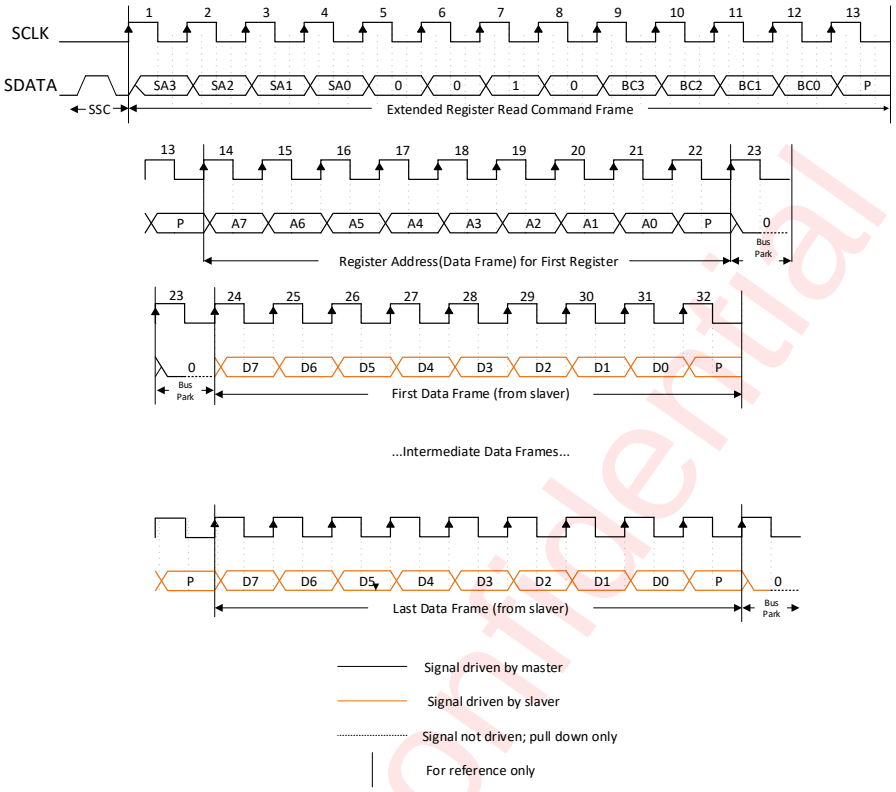


Figure 13 Extended Register read command sequence

Masked write:

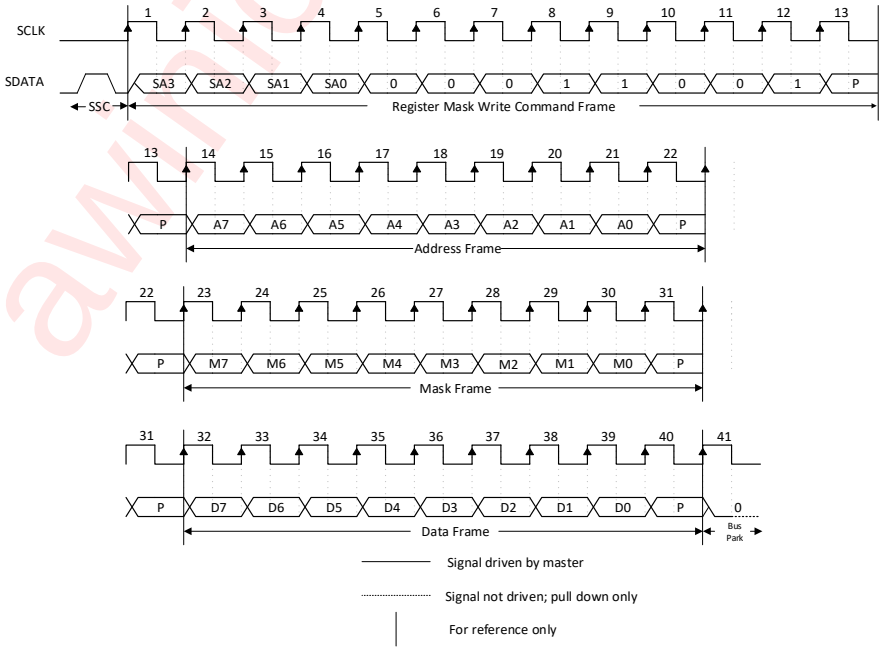


Figure 14 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER 0x0000：Output_Cross_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:1	SPARE	Reserved for future use	0x00	No	0	RW MW
0	Output_Cross	Enable DP4T output Switch to cross mode, 0x0: DP4T Direct operating mode 0x1: DP4T output cross operating mode	0x0	No	0-11	RW MW
Note: See Truth Table for example of operation						

REGISTER 0x0001：SW_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	SPARE	Reserved for future use	0x0	No	0	RW MW
5:4	SW_Connect_Ind[1:0]	Indicate switch connect sequence from bit 0 to bit 3 00: one port connect to output1, ouput2 isolation 01: Lower bit in bit0 to bit3 connect to output1 10: Higher bit in bit0 to bit3 connect to output1 11: one port connect to output2, ouput1 isolation	0x0	No	0-11	RW MW
3:0	Input_Sel[3:0]	Input Ports Select Enables DP4T input port. Each bit is a dedicated input port. 0000: Isolation Bit0 <->input1 Bit1 <->input2 Bit2 <->input3 Bit3 <->input4 0001: Input 1 Select 0010: Input 2 Select 0100: Input 3 Select 1000: Input 4 Select etc	0x0	No	0-11	RW MW
Note: See Truth Table for example of operation						

REGISTER 0x001A：RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset	0	No	No	W

		Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.				
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

REGISTER 0x001B：GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

REGISTER 0x001C：PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that*	0b000	B/G	No	W

		register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.				

REGISTER 0x001D：PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x06	No	No	R

REGISTER 0x001E：MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x49	No	No	R

REGISTER 0x001F：MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x00	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected via pin SID0	0x06	No	No	R/W
		USID set pin: 0 → USID: 0x06 USID set pin: 1 → USID: 0x07				
		Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.				

REGISTER 0x0020：EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

REGISTER 0x0021：REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Awinic according to manufacture date. The value may change throughout the product life cycle.				

REGISTER 0x0022：GSID2-3

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID2[3:0]	Group Slave ID2	0x0	No	No	R/W
3:0	GSID3[3:0]	Group Slave ID3	0x0	No	No	R/W

REGISTER 0x0023：UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

REGISTER 0x0024：ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W

5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
Note: Reading this register resets this register.						

REGISTER 0x002D：EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0x00	No	No	R/W

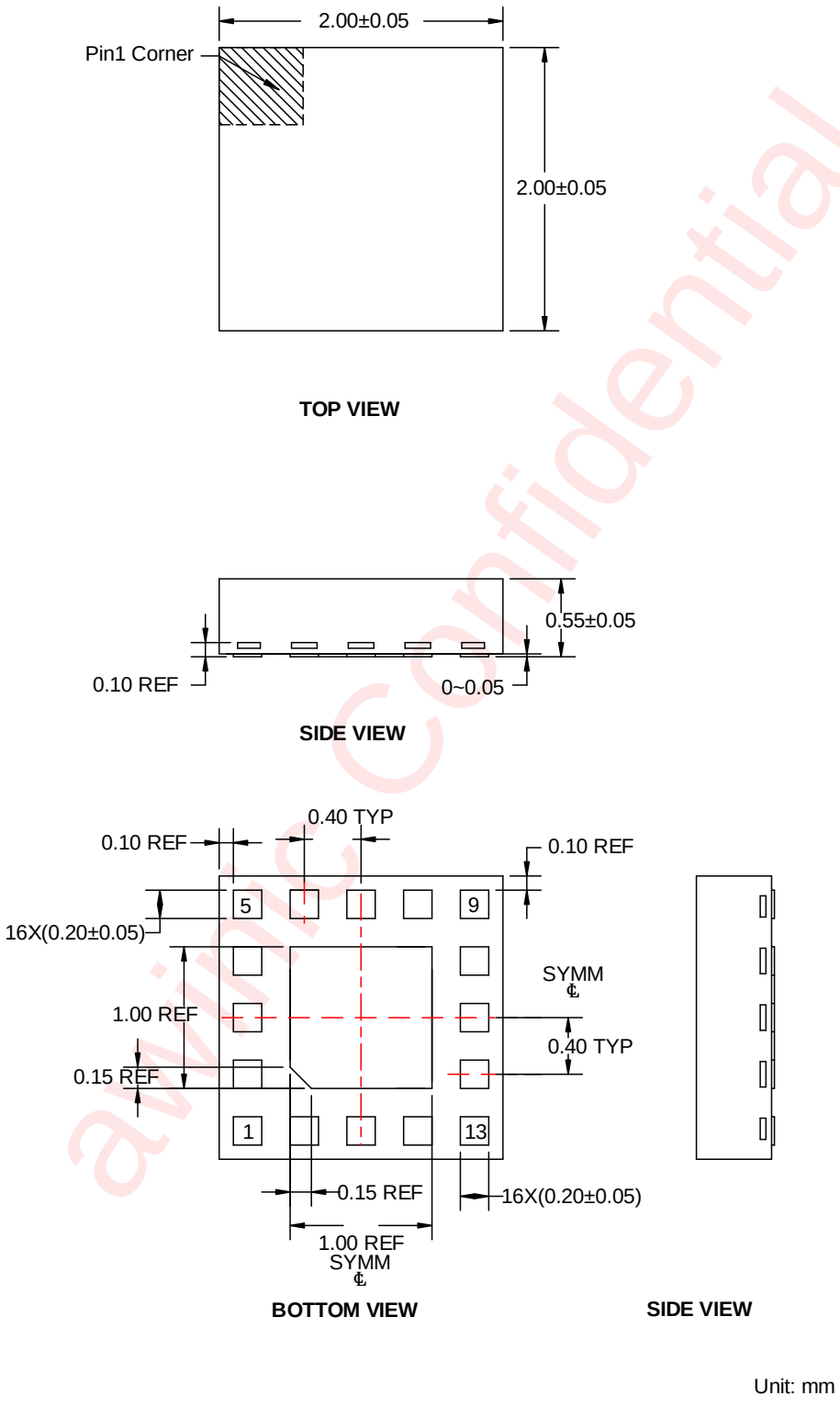
REGISTER 0x002E：EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

Truth Table

RFOUT1	RFOUT2	Reg_00	Reg_01					
		0	5	4	3	2	1	0
Isolation	Isolation	0	0	0	0	0	0	0
RFIN1	Isolation	0	0	0	0	0	0	1
RFIN2	Isolation	0	0	0	0	0	1	0
RFIN3	Isolation	0	0	0	0	1	0	0
RFIN4	Isolation	0	0	0	1	0	0	0
RFIN1	RFIN2	0	0	1	0	0	1	1
RFIN1	RFIN3	0	0	1	0	1	0	1
RFIN2	RFIN3	0	0	1	0	1	1	0
RFIN1	RFIN4	0	0	1	1	0	0	1
RFIN2	RFIN4	0	0	1	1	0	1	0
RFIN3	RFIN4	0	0	1	1	1	0	0
RFIN2	RFIN1	0	1	0	0	0	1	1
RFIN3	RFIN1	0	1	0	0	1	0	1
RFIN3	RFIN2	0	1	0	0	1	1	0
RFIN4	RFIN1	0	1	0	1	0	0	1
RFIN4	RFIN2	0	1	0	1	0	1	0
RFIN4	RFIN3	0	1	0	1	1	0	0
Isolation	RFIN1	0	1	1	0	0	0	1
Isolation	RFIN2	0	1	1	0	0	1	0
Isolation	RFIN3	0	1	1	0	1	0	0
Isolation	RFIN4	0	1	1	1	0	0	0
Isolation	Isolation	1	0	0	0	0	0	0
Isolation	RFIN1	1	0	0	0	0	0	1
Isolation	RFIN2	1	0	0	0	0	1	0
Isolation	RFIN3	1	0	0	0	1	0	0
Isolation	RFIN4	1	0	0	1	0	0	0
RFIN2	RFIN1	1	0	1	0	0	1	1
RFIN3	RFIN1	1	0	1	0	1	0	1
RFIN3	RFIN2	1	0	1	0	1	1	0
RFIN4	RFIN1	1	0	1	1	0	0	1
RFIN4	RFIN2	1	0	1	1	0	1	0
RFIN4	RFIN3	1	0	1	1	1	0	0
RFIN1	RFIN2	1	1	0	0	0	1	1
RFIN1	RFIN3	1	1	0	0	1	0	1
RFIN2	RFIN3	1	1	0	0	1	1	0
RFIN1	RFIN4	1	1	0	1	0	0	1
RFIN2	RFIN4	1	1	0	1	0	1	0
RFIN3	RFIN4	1	1	0	1	1	0	0
RFIN1	Isolation	1	1	1	0	0	0	1
RFIN2	Isolation	1	1	1	0	0	1	0
RFIN3	Isolation	1	1	1	0	1	0	0
RFIN4	Isolation	1	1	1	1	0	0	0

Package Description



Unit: mm

Figure 15 Package Outline

Land Pattern Data

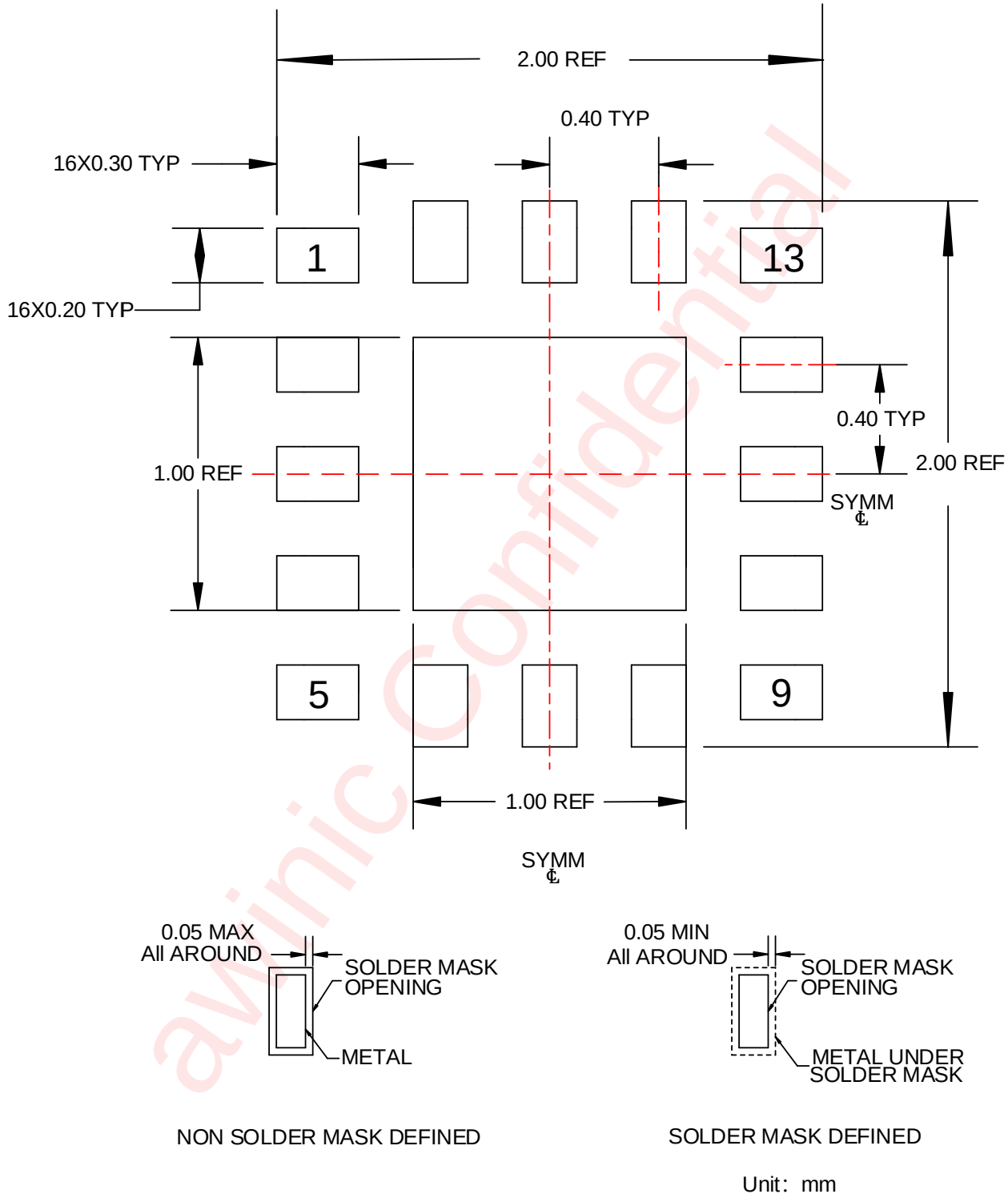
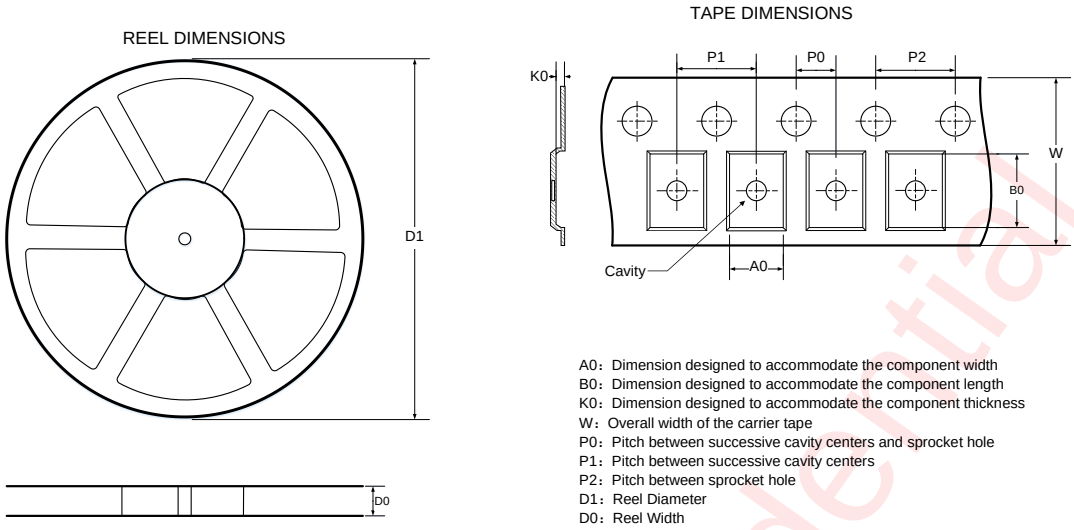
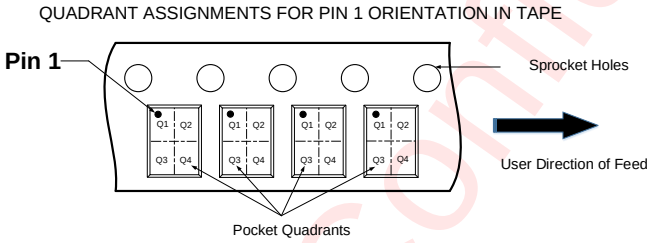


Figure 16 Land Pattern Data

Tape And Reel Information



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

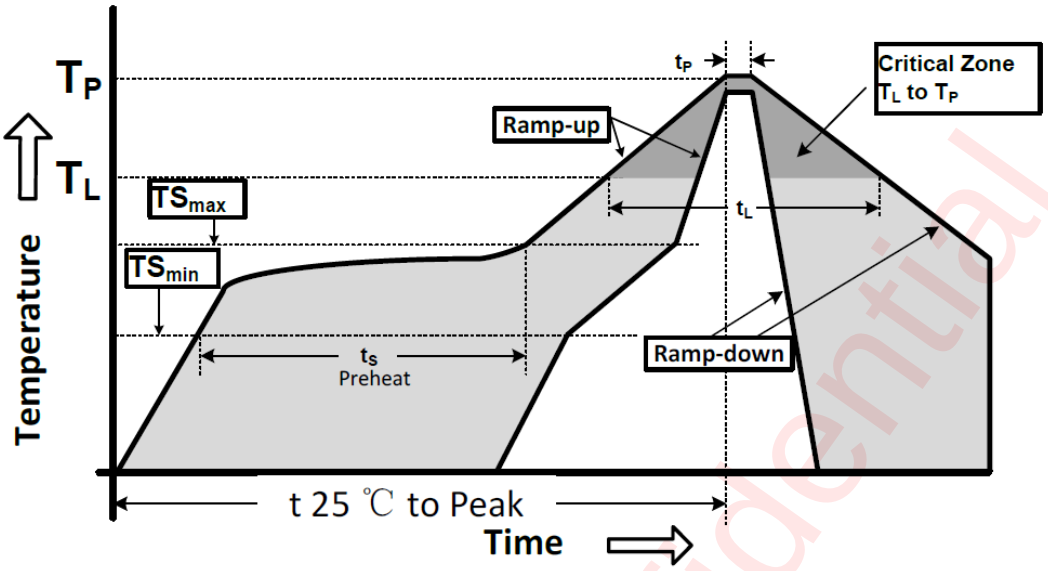
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.25	2.25	0.75	2	4	4	8	Q1

All dimensions are nominal

Figure 17 Tape and Reel

REFLOW



Reflow Note	Spec
Ramp-up rate（TSmax to Tp）	3℃/second max.
Preheat temperature（Tsmin to Tsmax）	150℃ to 200℃
Preheat time（ts）	60 – 180 seconds
Time above TL , 217℃（tL）	60 – 150 seconds
Peak temperature（Tp）	260℃
Time within 5℃ of peak temperature(tp)	20 – 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

备注：可过 reflow 次数≥3

Revision History

Version	Date	Change Record
V1.0	Oct. 2021	Officially Released
V1.1	Aug.2022	Update Delivery Form
V1.2	Aug.2022	Update Supply Voltage VIO for MIPI

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