Li-ION/POLYMER 3-CELL PROTECTOR

GENERAL DESCRIPTION

XBM3301 is a protection IC for 3 serial-c-ell lithium-ion/lithium polymer rechargeabl-e batteries and includes high accuracy volt-age detection circuitsdelay circuits and Cell balance circuits

XBM3301 is suitable for protecting 3 seri-al-cell rechargeable lithium-ion/lithium poly-mer battery packs from overcharge, overdi-scharge,overcurrent,short-circuiting and c-ell unbalance.

FEATURES

- Manufactured with High Voltage Tolera nt Process Maximum Rating 28V
- Low supply current
- Cell voltage3.6V,for 3-cell Typ.15μA(I_q)
- Cell voltage2.0V, for 3-cellTyp.0.5μA(I_{sd})
- SSOP16(pitch 0.65mm) Package
- Variety of detector threshold
- Over-charge detector threshold-V_{cu}:3.7V -4.5V step of 0.1V
- Overcharge ReleaseVoltage-V_{cL}=V_{cu}-0.1 5V
- Overdischarge detector threshold V_{DL}:2. 4V-3.0V step of 0.1V
- Over-discharge Release Voltage-V_{DR}= V_{DL} +0.4V
- Discharge-current threshold1 0.2V
- Short detector threshold 1.5V (Fixed)
- Charge-current threshold -0.2V
- Setting of Output delay time
- Overcharge detector Output Delay 1.0s
- Overdischarge detector Output Delay 100ms
- Discharge-current detector Output Dela-y 9ms
- Charge-current detector Output Delay 9 ms
- Short Circuit detector Output Delay 100 μs
- 0V Battery Charging Function
- Built-in Cell balance Function
- ESD HBM >4KV
- RoHS Compliant and Lead Pb Free

APPLICATIONS

- Power Tools
- E-Bike
- Power Bank
- 3 Cell Lithium-ion or Lithium polymer re-chargeable battery pack

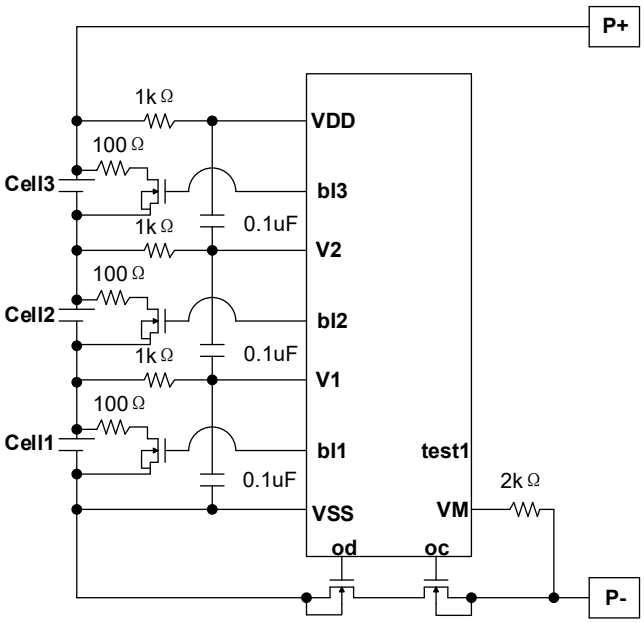


Figure 1. Typical Application Circuit

ORDERING INFORMATION

PART NUMBER	OCV [VCU] (V)	OCRV [VCL] (V)	ODV [VDL] (V)	ODRV [VDR] (V)	TOP MARK
XBM3301	4.25±50mV	4.10±50mV	2.7±100mV	3.1±100mV	XBM3301YW

Note: "YW" is manufacture date code, "Y" means the year, "W" means the week.

PIN CONFIGURATION

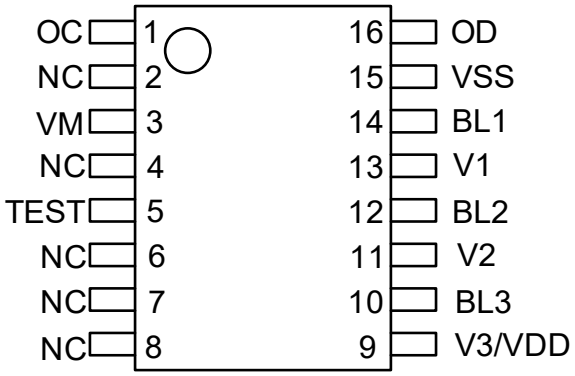


Figure 2. PIN Configuration

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	OC	Connection pin of charge control FET gate (CMOS output)
3	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)
5	TEST	Test Pin, Not Use
9	V3/VDD	Positive terminal Pin for Cell-3,VDD pin for the IC
10	BL3	Cell balance control pin for Cell-3
11	V2	Positive terminal Pin for Cell-2
12	BL2	Cell balance control pin for Cell-2
13	V1	Positive terminal Pin for Cell-1
14	BL1	Cell balance control pin for Cell-1
15	VSS	VSS pin. Ground pin for the IC
16	OD	Connection pin of discharge control FET gate (CMOS output)
2,4,6,7,8	NC	Not Used

ABSOLUTE MAXIMUM RATINGS

(NOTE: DO NOT EXCEED THESE LIMITS TO PREVENT DAMAGE TO THE DEVICE. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR LONG PERIODS MAY AFFECT DEVICE RELIABILITY.)

PARAMETER	VALUE	UNIT
VDD Supply Voltage; VM	-0.3~30	V
V1、BL1 to Vss； V2、BL2 to V1；V3、BL3 to V2	-0.3~6.5	V
OC	VSS-0.3~VSS+30	V
OD	VSS+0.3~VDD+0.3	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C
Power Dissipation at T=25°C	0.6	W
Package Thermal Resistance (Junction to Ambient) θJA	210	°C/W
Package Thermal Resistance (Junction to Case) θJC	35	°C/W
ESD(HBM)	6000	V

ELECTRICAL CHARACTERISTICS

Typical and limits appearing in normal type apply for TA = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Detection Voltage						
Charger Detection Voltage	V_{CHA}		-0.17	-0.2	-0.23	V
Discharger Detection Voltage	V_{DIS}		0.17	0.2	0.23	V
Current Consumption						
Current Consumption in Normal Operation	I_{OPE}	VDD=3.6V VM =0V		15	20	μA
Current Consumption in Power Down	I_{PD}	VDD=2.0V VM pin floating		0.5	1.0	μA
Detection Delay Time						
Overcharge Voltage Detection De-layTime	t_{CU}		500	800	1100	mS
Overdischarge Voltage Detection Delay Time	t_{DL}		70	100	140	mS
Overdischarge Current1 Detection Delay Time	t_{IOV1}	V_{DD}=3.6V	5	8	12	mS
Load Short-Circuiting Detection Delay Time	*t_{SHORT}	V_{DD}=3.6V	100	150	250	μS
Cell balance						
Cell Balance Voltage Threshold	V_{BL}	Other Cell Voltage 3.6V	3.75	3.83	3.90	V
Cell Balance Voltage hysteresis				50		mV

Note1: *---The parameter is guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM

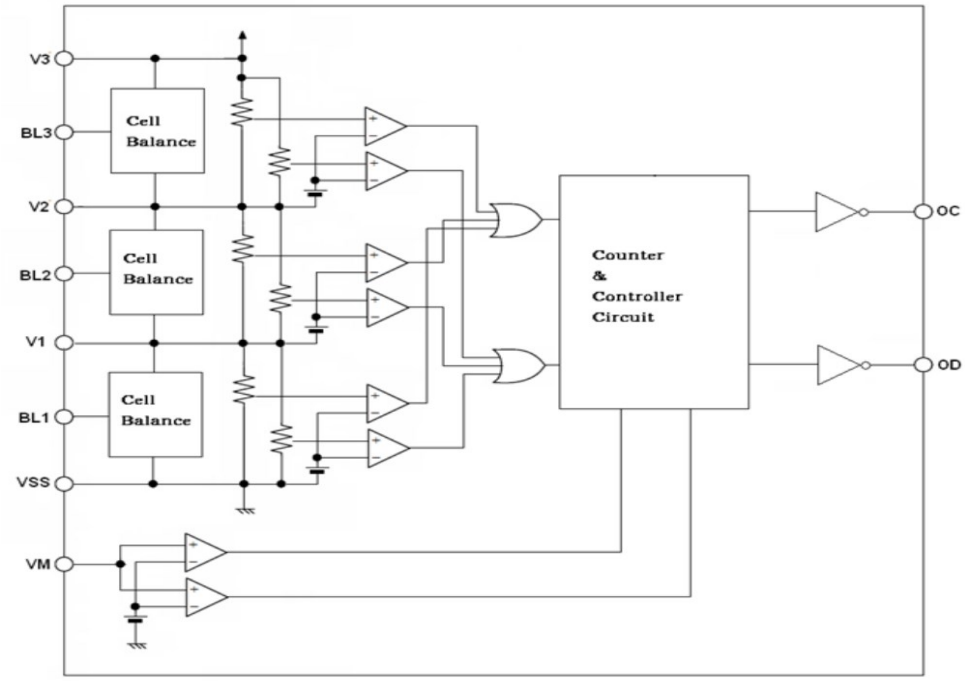


Figure 3. Functional Block Diagram

OPERATION

Over-charge detectors

While the cell is charged, the voltage between V1 pin and V_{SS} pin (voltage of the Cell1), the voltage between V2 pin and V1 pin (voltage of the Cell-2), the voltage between V3 pin and V2 pin (voltage of the Cell-3) are supervised. If at least one of the cells' voltage becomes equal or more than the over charge detector threshold, the overcharge is detected, and an external charge control N-MOSFET turns off with OC pin being at "L" level via an external pull-down resister and charge stops.

To reset the over charge and make the OC pin level to "H" again after detecting over charge, in such conditions that a time when all the cells' voltages are down to a level lower than overcharge released voltage. The output voltage of OC pin becomes "H", and it makes an external N-MOSFET turns on, and charge cycle is available. The over-charge detectors have hysteresis. Internal fixed output delay times for overcharge detection and release from overcharge exist. Even if one of voltage of Cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. Even when the voltage of each cell becomes equal or higher level than V_{CU} if these voltages would be back to a level lower than the overcharge detector threshold within a time period of the output delay time, the overcharge is not detected. Besides, after detecting overcharge, each cell voltage is lower than the overcharge detector released voltage, even if just one of cells' voltage becomes equal or more than the over-charge released voltage within the released output delay time, overcharge is not released.

Over-discharge detectors

While the cells are discharged, the voltage between V1 pin and V_{SS} pin (the voltage of Cell-1), the voltage between V2 pin and V1 pin (Cell-2 voltage), the voltage between V3 pin and V2 pin (Cell-3 voltage) are supervised. If at least one of the cells' voltage becomes equal or less than the over-discharge detector threshold, the over-discharg

e is detected and discharge stops by the external discharge control N-MOSFET turning off with the OD pin being at "L". The condition to release over-discharge voltage detector is that after detecting over-discharge voltage, all the cells' voltage becomes higher than the over-discharge released voltage, OD pin becomes “H”level, and by turning on the external N-MOSFET, discharge becomes possible. The over-discharge detectors have hysteresis.

Internal fixed output delay times for over-charge detection and release from over-charge exist. If at least one of the voltage of Cells is down to equal or lower than the over-discharge detector threshold, if the voltage of each Cell would be back to a level higher than the over-discharge detector threshold within a time period of the output delay time, the over-discharge is not detected. Output delay time for release from over-discharge is also set internally. After detecting over-discharge, supply current would be reduced and be into standby by halting unnecessary circuits and consumption current of the IC itself is made as small as possible.

Discharge-current Detector, & Short Circuit Protector

When the discharge is acceptable, VM voltage is supervised, if the load is short and VM voltage becomes equal or more than excess discharge current threshold, and equal or less than short detector threshold, the status becomes excess discharge current detected condition. If VM voltage becomes equal or more than short circuit detector threshold, the status becomes short circuit detected, then OD pin outputs "L" and by turning off the external MOSFET, large current flow is prevented. The excess discharge current detector and short detector has the fixed output delay time.

Charge-current detector

When the charge is acceptable, VM voltage is supervised, if the VM voltage becomes equal or more than excess charge current threshold, the status becomes excess charge current detected condition. then OC pin outputs "L" and by turning off the external MOSFET, large current flow is prevented. Output delay of excess charge current is internally fixed.

Cell balance function

When every cell voltage is above V_{BL} or every cell voltage is below V_{BL}, cell balance function will not work. If the voltage of only one cell or two cells is below V_{BL} and others' voltage is above V_{BL}, these cells(above V_{BL}) 's BLn pin will output "H" one by one and an external Nch transistor for cell balance turns on, and discharge path is connected in parallel with the cell and charge current is reduced.

The balance current can be set by one external resistor. absolute ratings must be cared.

If the cell balance function is unnecessary, BLn pin must be open.

When there are two high level cells, the cell balancing function see below sheet. When the cell voltage of this priority cell is below V_{BL}, the cell balancing function of the other high level cell will turn on.

V3	H	L	H
V2	H	H	L
V1	L	H	H
Priority Cell	V3	V2	V1

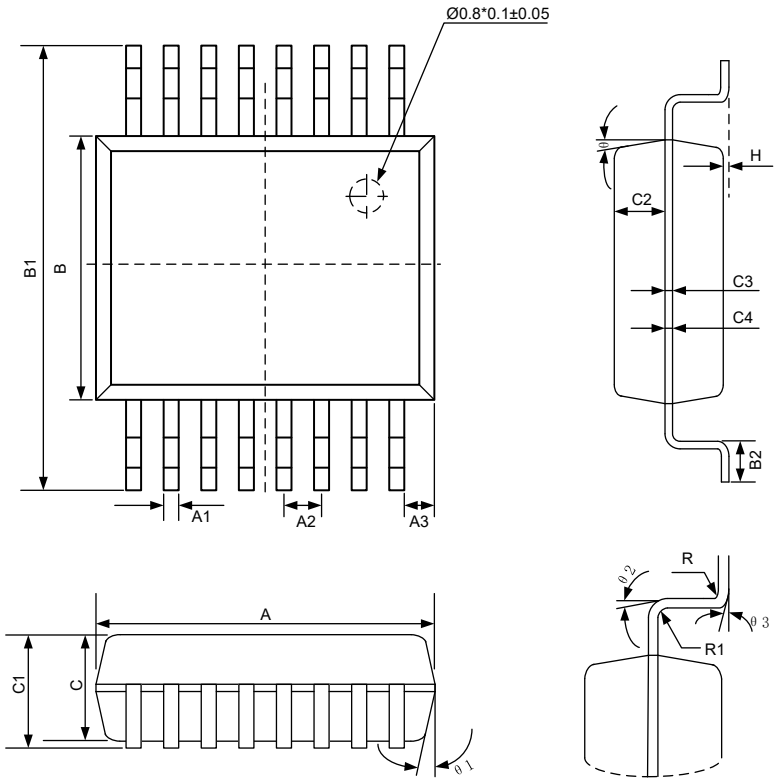
Remark:

"H" means cell voltage is above V_{BL} ,"L" means cell voltage is below V_{BL}.

Cell balancing function will not be turned on when all cells’ voltage are above V_{BL}.

In standby and discharging condition, When the voltage of one battery is lower than the over-discharge voltage (VDL), the cell balancing function will not work. In charging condition, when the voltage of one battery is lower than over-discharge voltage (VDL), the cell balancing function still works.

PACKAGE OUTLINE(SSOP16)



Symbol	Min(mm)	Max(mm)	Symbol	Min(mm)	Max(mm)
A	6.15	6.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.15
A3	0.675TYP		θ	12°TYP4	
B	5.25	5.35	θ 1	12°TYP4	
B1	7.65	7.95	θ 2	10°TYP	
B2	0.60	0.80	θ 3	0°~8°	
C	1.70	1.80	R	0.20TYP	
C1	1.75	1.95	R1	0.15TYP	
C2	0.799				

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