

0.1-8.5GHz SPDT Switch for 3G/4G/5G RX

Features

- Broadband frequency range: 0.1 to 8.5GHz
- Low insertion loss: 0.52dB typical @ 5.8 GHz
- High isolation: 24dB @ 5.8 GHz
- Integrated logic
- DFN 1.1 mm x 0.7 mm x 0.55 mm-6L package

Applications

- Cellular 3G/4G/5G RX and WLAN
- Cellular modems , tablets and USB Devices
- Other RF front-end modules
- UWB Application

General Description

The AW13012TDNR is a SPDT switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 3G/4G/5G, data cards and tablets. It is also WLAN compatible.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13012TDNR is provided in a compact DFN 1.1mm x 0.7mm x 0.55mm-6L package.

Typical Application Circuit

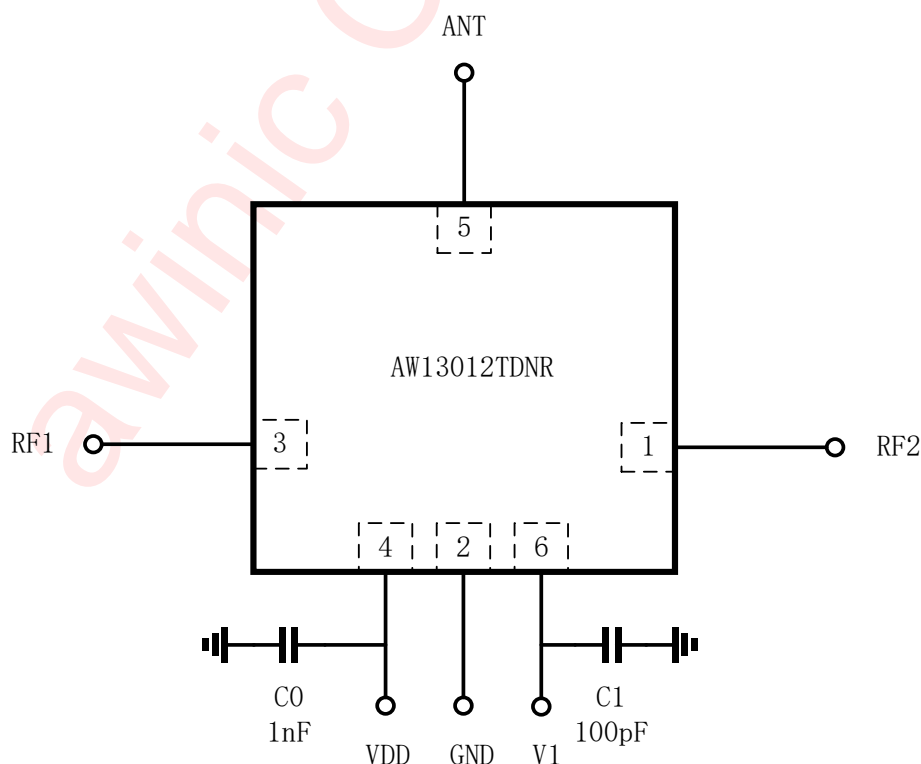


Figure 1 Typical Application Circuit of AW13012TDNR

Pin Configuration And Top Mark

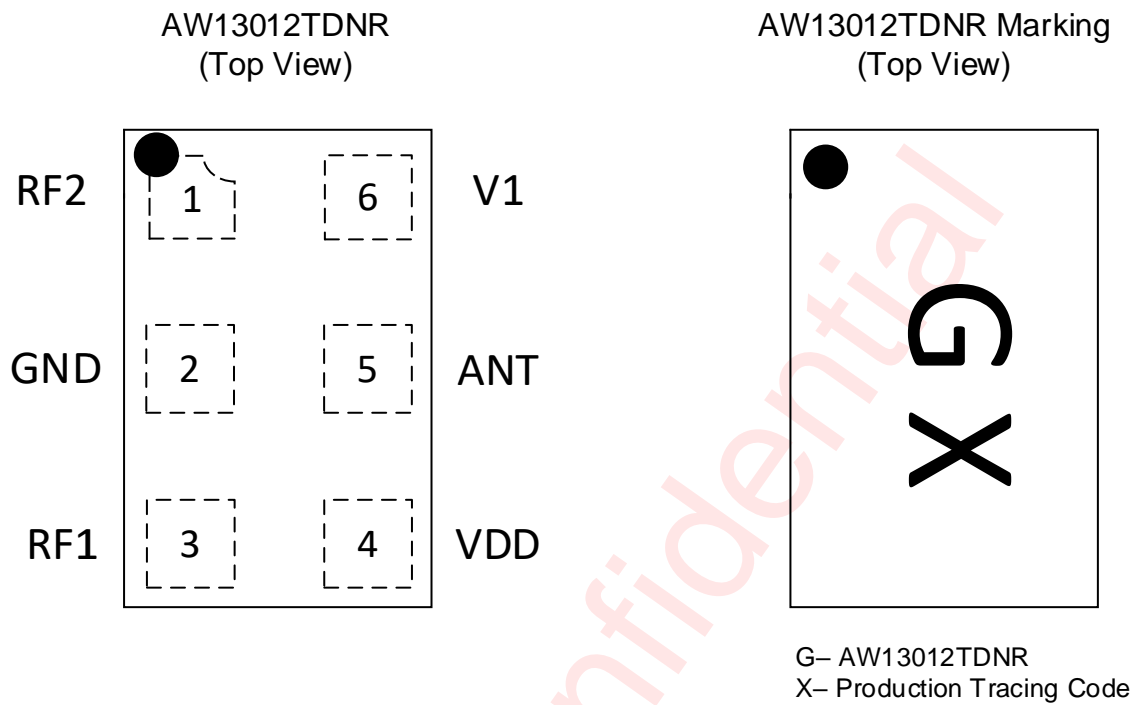


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF2	RF I/O path 2
2	GND	Ground
3	RF1	RF I/O path 1
4	VDD	DC power supply
5	ANT	Antenna port
6	V1	DC control voltage 1

Functional Block Diagram

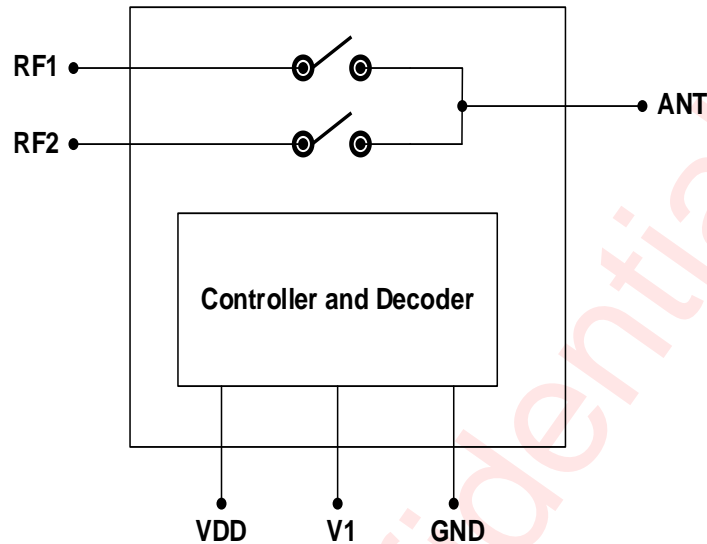


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13012TDNR	-40°C~85°C	DFN 1.1mmX0.7mm X0.55mm-6L	G	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		-0.3V to 3.6V
Control Voltage Range	V1	-0.3V to 3.6V
RF input power(RF1/RF2)		32dBm
Operating Free-air Temperature Range		-40°C to 85°C
Storage Temperature T _{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD (NOTE 2)		
HBM		±1000V
CDM		±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

HBM Test method: ESDA/JEDEC JS-001-2017. CDM Test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Ranges

PARAMETER		MIN	TYP	MAX	UNIT
VDD	Supply Voltage	1.65	1.8	3.3	V
VCTL_H	Control Voltage High	0.9		3.3	V
VCTL_L	Control Voltage LOW	0		0.3	V

Electrical Characteristics at 3.3V Supply

VDD=3.3V, V1=0/3.3V, PIN=0dBm, TEMP=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
IDD	Supply Current			25	50	μA
VCTL_H VCTL_L	Control Voltage High Low		0.9 0		VDD 0.3	V
ICTL	Control Current	VCTL=3.3V		1	5	μA
T _{SW}	Switching On/Off Time	50% of final control voltage to 10%/90% of final RF power, switching between RF1/2		200	300	ns
IL	Insertion loss(ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz		0.25 0.32 0.35 0.38 0.45 0.55 0.80	0.33 0.40 0.45 0.50 0.55 0.65 1.00	dB
ISO	Isolation (ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz	35 27 26 25 22 16 15	38 30 29 28 25 19 17		dB
RL	Input return loss (ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz	25 20 18 17 15 14 12	30 25 23 21 19 17 15		dB
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		90		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		88		dBc
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 1900MHz		90		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 1900MHz		88		dBc
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 2400MHz		90		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 2400MHz		88		dBc
P _{0.1dB}	0.1dB Compression Point (ANT pin to RF1/RF2)	0.1GHz–6GHz, 25% DC		32		dBm

Electrical Characteristics at 1.8V Supply

VDD=1.8V, V1=0/1.8V, PIN=0dBm, TEMP=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
IDD	Supply Current			20	50	μA
VCTL_H VCTL_L	Control Voltage High Low		0.9 0		VDD 0.3	V
ICTL	Control Current	VCTL=1.8V		1	5	μA
T _{SW}	Switching On/Off Time	50% of final control voltage to 10%/90% of final RF power, switching between RF1/2		210	300	ns
IL	Insertion loss(ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz		0.28 0.35 0.38 0.42 0.52 0.62 0.85	0.36 0.45 0.50 0.55 0.65 0.75 1.05	dB
ISO	Isolation (ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz	34 26 25 24 21 16 14	37 29 28 27 24 19 16		dB
RL	Input return loss (ANT pin to RF1/RF2)	0.1-0.9GHz 0.9-1.9GHz 1.9-2.4GHz 2.4-3.8GHz 3.8-5.8GHz 5.8-7.125GHz 7.125-8.5GHz	25 20 18 16 15 13 12	30 25 23 20 19 17 15		dB
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		90		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		80		dBc
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 1900MHz		88		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 1900MHz		80		dBc
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 2400MHz		88		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 2400MHz		80		dBc
P _{0.1dB}	0.1dB Compression Point (ANT pin to RF1/RF2)	0.1GHz–6GHz, 25% DC		32		dBm

Timing Diagram (Power ON and OFF sequence)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V1 should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

- 1) Apply voltage supply --- VDD
- 2) Set Controls---V1
- 3) Apply RF input

Change switch position from one RF port to another:

- 1) Remove RF input
- 2) Change control voltages V1 to set the switch to desired RF port
- 3) Apply RF input

Power OFF:

- 1) Remove RF input
- 2) Remove control voltages-V1
- 3) Remove VDD input

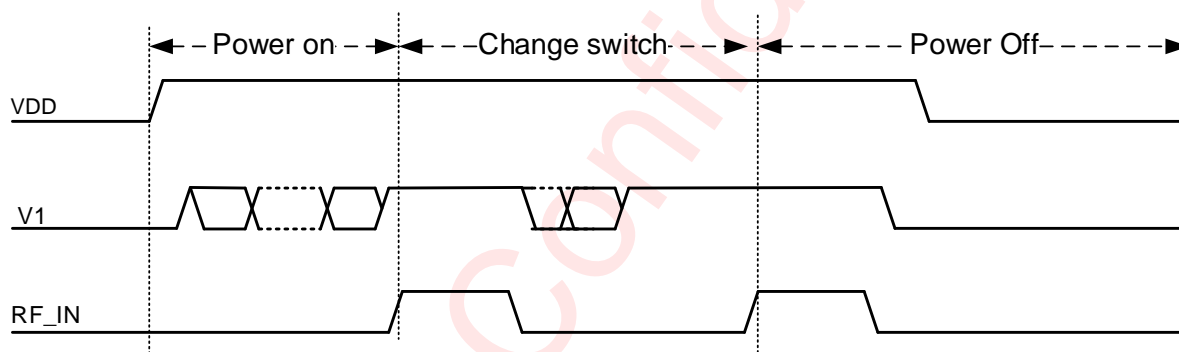
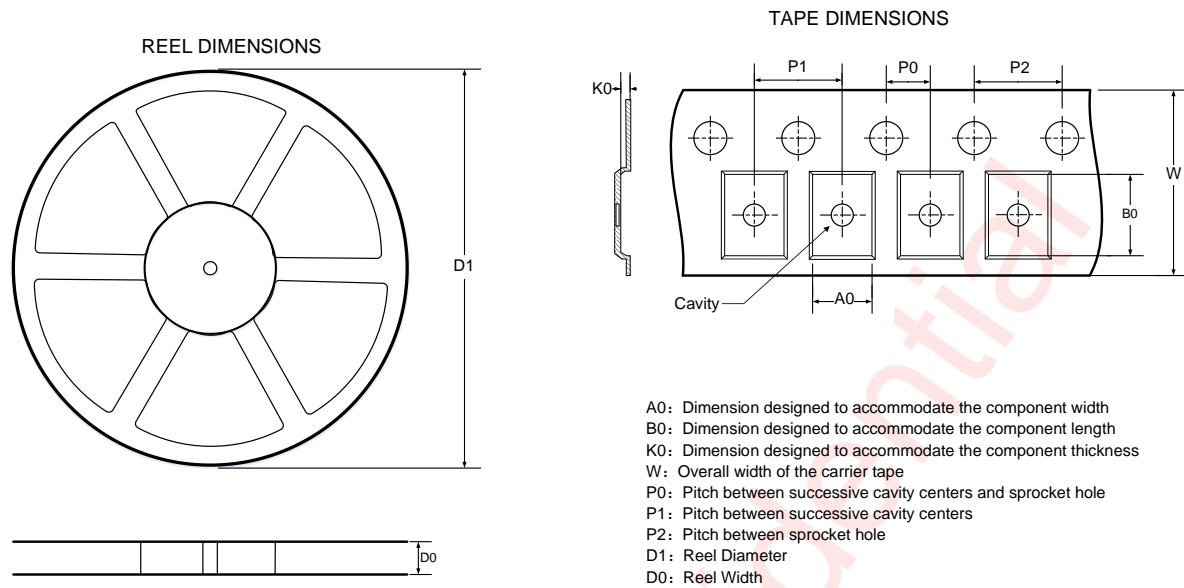


Figure 4 Power on/Change switch/Power off sequence

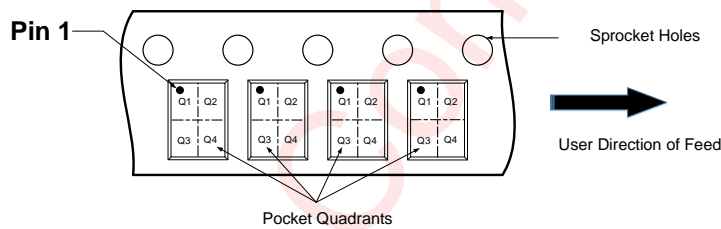
Control Logic

State	Active Path	V1
0	ANT to RF1	0
1	ANT to RF2	1

Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

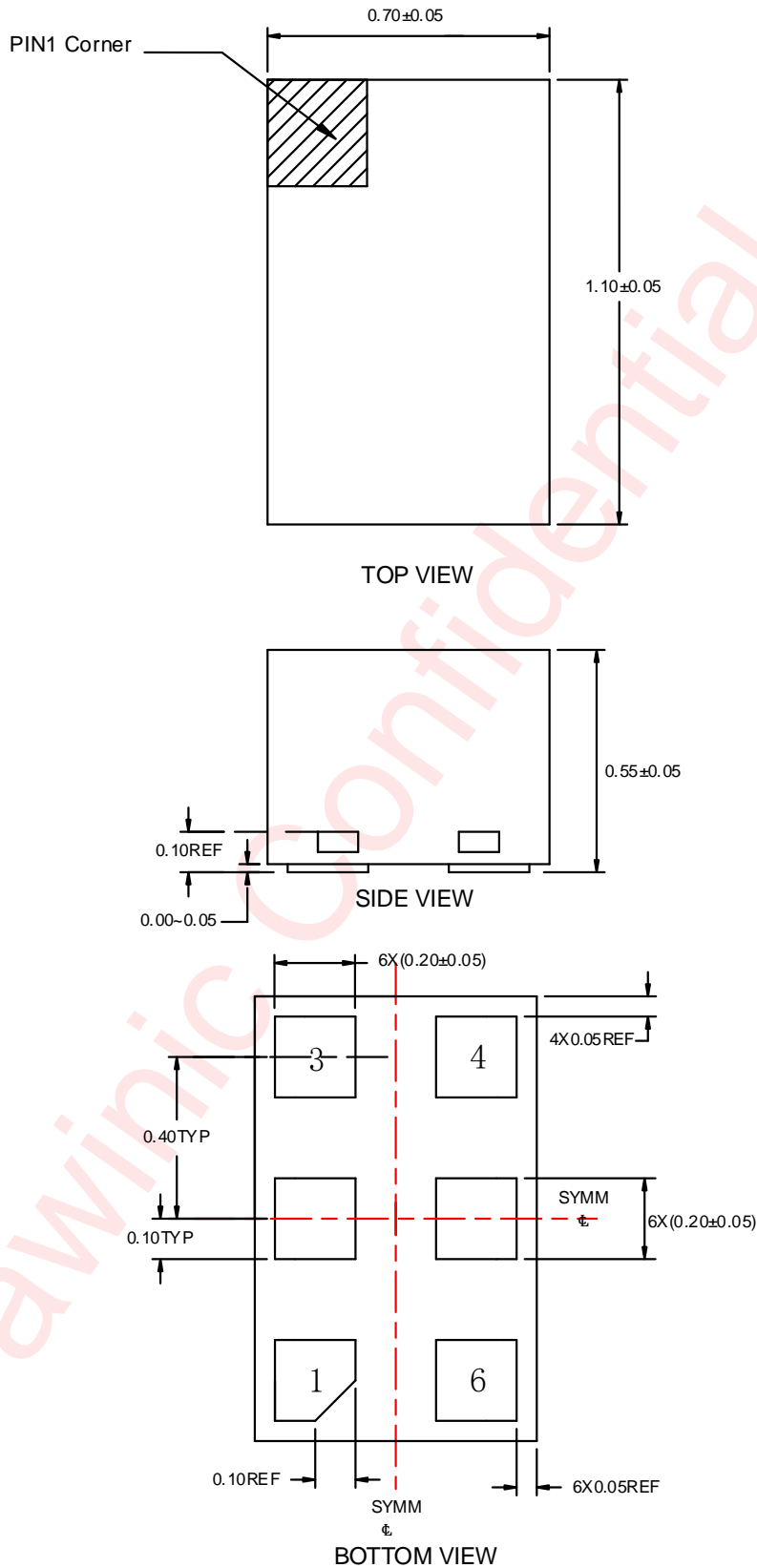
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.66	2	2	4	8	Q1

All dimensions are nominal

Figure 5 Tape and Reel

Package Description



Unit: mm

Figure 6 Package Outline

Land Pattern Data

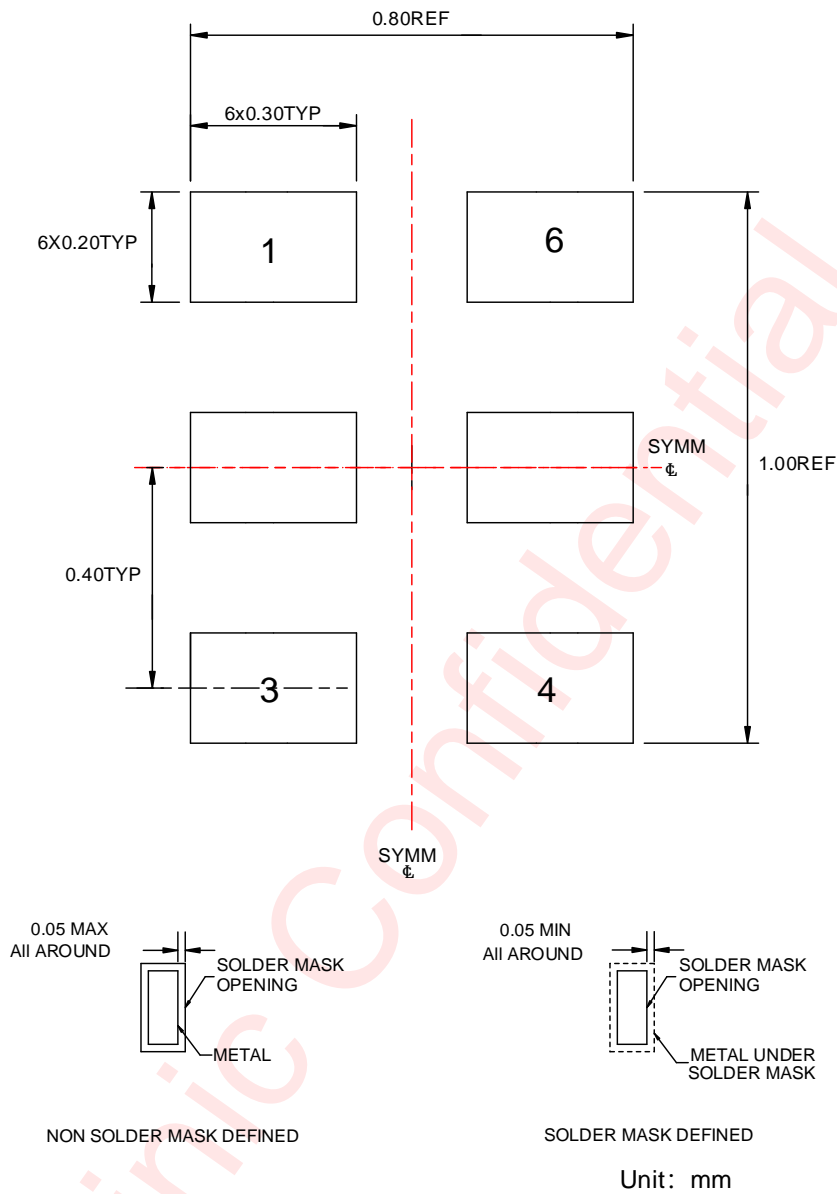


Figure 7 Land Pattern

Revision History

Vision	Date	Change Record
V1.0	Sep. 2021	Officially Released
V1.1	Jul. 2022	Update AMR and Recommended Operating Ranges
V1.2	Aug. 2022	Update Ordering Information and Electrical Characteristics

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