JD6621

Fast Charge Protocols, USB-PD 3.0 with PPS Controller

Description

The JD6621 is a highly integrated USB Power Delivery (PD) controller that supports USB PD 3.0 with Programmable Power Supply (PPS) specification designed for USB Type-C Downstream Facing Port (Source). It monitors the CC pin to detect a USB Type-C attach/detach. It is capable providing output voltage of 3.3V to 21V.

Additionally, the JD6621 integrates Huawei Super Charging Protocol (SCP), Fast Charging Protocol (FCP) and Qualcomm® Quick Charge™ 2.0/3.0/3+ (QC 2.0/3.0/3+) USB interface. It monitors USB D+/D− data line and automatically adjusts the output voltage depending on different powered device. If the powered device doesn't support USB PD protocol, the JD6621 can support other protocol as mentioned above.

The JD6621 integrates dual amplifiers with respectively reference voltages are included for voltage-loop and current-loop regulation to provide constant-voltage (CV) and constant-current (CC) regulation in applications of high precision control.

The JD6621 integrates 100mW switch to provide VCONN power for E-mark cable and provides VCONN discharge function.

Features

Protocols:

- USB Power Delivery 3.0 with PPS Specifications, TID:3543
- 3.3V to 21V Power Sourcing
- 100mW VCONN Power (20mA)
- VBUSC and VCONN Discharge Function
- Supports Qualcomm® Quick Charge™ Protocol QC 2.0/QC 3.0/QC 3+/QC 5
- Supports Huawei Fast Charging Protocol (FCP) & Super Charge Protocol (SCP)
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2

Others:

- Supports PDO Selectable Function
- Multi-Ports Control (MPC) Application
- Constant Voltage and Constant Current Control
- Over-Voltage Protection
- Under-Voltage Protection
- Over-Current Protection
- Over-Temperature Protection
- Short-Circuit Protection
- TQFN-20L (4 x 4 mm) Package

Applications

- Wall-Adapter
- Car Charger
- Power strip
- USB Power Output Ports

Pin Assignments

W7 Package: TQFN-20L (4mm x 4mm)

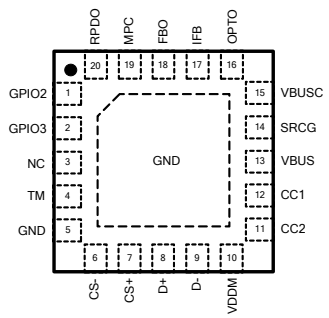


Figure 1. Pin Assignment of JD6621

Ordering Information

JD6621□

Package Type
W7: TQFN-20L (4 x 4 mm)

Typical Application Circuit

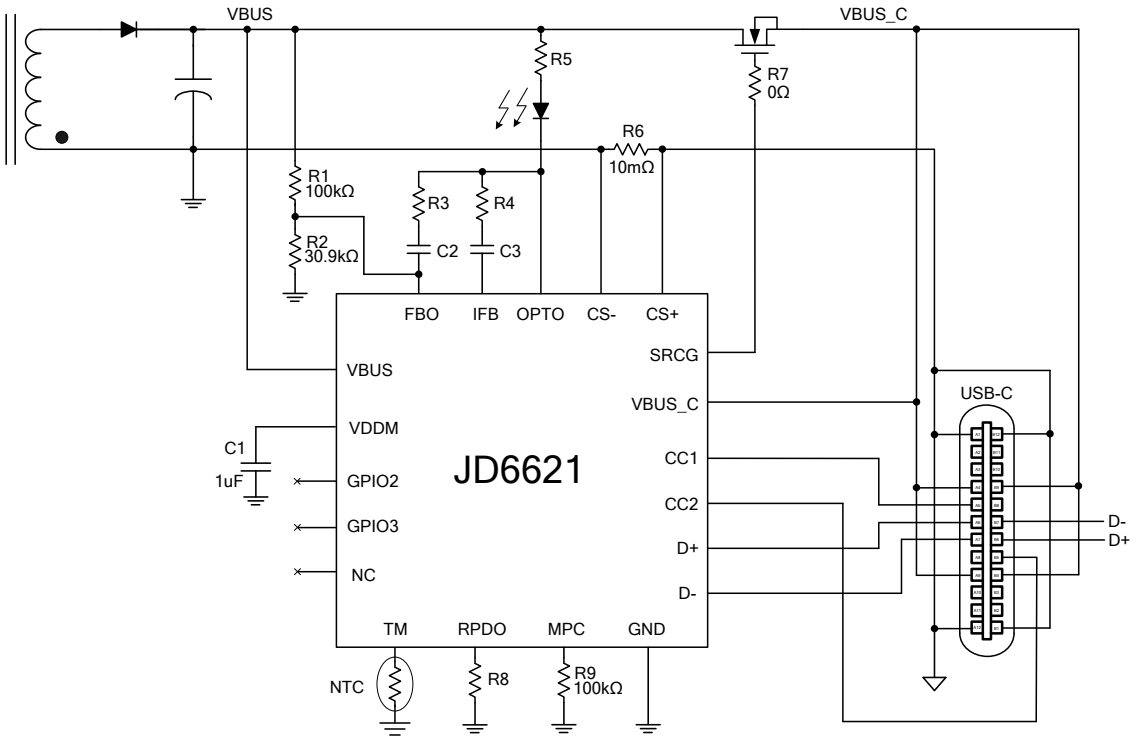


Figure 2. JD6621 Application Circuit

Table 1. R_{PDO} and Power Configuration Selection:

R_{PDO} (Ω)	Power	5V	9V	12V	15V	20V	PPS	QC Mode
open	20W	3A	2.22A	1.67A	-	-	-	5V/9V/12V
680k	25W	3A	2.77A	-	-	-	3.3V~5.9V/3A 3.3V~11V/2.25A	5V/9V
470k	27W	3A	3A			-	3.3V~5.9V/3A 3.3V~11V/2.45A	5V/9V
220k	30W	3A	3A	2.5A	2A	1.5A	3.3V~11V/2.7A 3.3V~21V/1.45A	5V/9V/12V/20V
100k	45W	3A	3A	3A	3A	2.25A	3.3V~11V/3A 3.3V~21V/2.15A	5V/9V/12V/20V
68k	45W	3A	3A	3A	3A	2.25A	3.3V~11V/3A 3.3V~21V/2.15A	5V/9V/12V/20V
47k	65W	3A	3A	3A	3A	3.25A	3.3V~11V/3A 3.3V~21V/3.1A *3.3V~11V/5A *3.3V~21V/3.1A	5V/9V/12V/20V
22k	65W	3A	3A	3A	3A	3.25A	3.3V~11V/3A 3.3V~21V/3.1A *3.3V~11V/5A *3.3V~21V/3.1A	5V/9V/12V/20V
10k	100W	3A	3A	*5A	*5A	*5A	3.3V~11V/3A 3.3V~21V/3A *3.3V~11V/5A *3.3V~21V/5A	5V/9V/12V/20V
0	100W	3A	3A	*5A	*5A	*5A	3.3V~11V/3A 3.3V~21V/3A *3.3V~11V/5A *3.3V~21V/5A	5V/9V/12V/20V

Table 2. Power Reduction and Power Configuration Selection:

R_{PDO} (Ω)	Power Reduction	5V	9V	12V	15V	20V	PPS	QC Mode
open	15W	3A	-	-	-	-	-	5V
680k	18W	3A	2A	-	-	-	-	5V/9V
470k	18W	3A	2A	-	-	-	-	5V/9V
220k	20W	3A	2.22A	1.67A	-	-	-	5V/9V/12V
100k	20W	3A	2.22A	1.67A	-	-	-	5V/9V/12V
68k	30W	3A	3A	2.5A	2A	1.5A	3.3V~11V/2.7A 3.3V~21V/1.45A	5V/9V/12V/20V
47k	20W	3A	2.22A	1.67A	-	-	-	5V/9V/12V
22k	45W	3A	3A	3A	3A	2.25A	3.3V~11V/3A 3.3V~21V/2.15A	5V/9V/12V/20V
10k	45W	3A	3A	3A	3A	2.25A	3.3V~11V/3A 3.3V~21V/2.15A	5V/9V/12V/20V
0	65W	3A	3A	3A	3A	3.25A	3.3V~11V/3A 3.3V~21V/3.1A *3.3V~11V/5A *3.3V~21V/3.1A	5V/9V/12V/20V

Functional Pin Description

Pin Name	Pin No.	Pin Function
GPIO2	**1**	Programmable digital input/output pin.
GPIO3	**2**	Programmable digital input/output pin.
NC	**3**	No connection.
TM	**4**	External thermal sensor connection node (NTC).
GND	**5**	Ground pin. Connect this pin to exposed pad.
CS-	**6**	Negative input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path.
CS+	**7**	Positive input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path.
D+	**8**	USB D+ data line for USB interface.
D-	**9**	USB D- data line for USB interface.
VDDM	**10**	Internal regulator output. Connect a 1uF capacitor to GND to stabilize the internal regulator voltage.
CC2	**11**	Type-C configuration channel signal 2.
CC1	**12**	Type-C configuration channel signal 1.
VBUS	**13**	VBUS voltage detection pin.
SRCG	**14**	NMOS gate node control pin.
VBUSC	**15**	VBUSC voltage detection and discharge pin.
OPTO	**16**	Output voltage control pin. Current sink function for opto-coupler node.
IFB	**17**	Feedback input pin for constant-current loop.
FBO	**18**	Feedback output pin. Current sink/source FB node.
MPC	**19**	Multi-ports control pin. Connect a 100kΩ resistor to GND.
RPDO	**20**	Select the PDO VBUS voltage. Connect a resistor to ground.

Absolute Maximum Ratings (Note 1)

- VBUS, VBUSC, SRCG Pins Voltage ---------- -0.3V to +35V
- CC1, CC2, D+, D−, OPTO Pins Voltage ---------- -0.3V to +24V
- All Other Pins Voltage ---------- -0.3V to +7V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Operating Ambient Temperature Range ---------- -40°C to +85°C
- Operating Junction Temperature Range ---------- -40°C to +125°C

Electrical Characteristics

(VBUS=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VBUS Input Voltage Range	V_{BUS}		3.3		21	V
VBUS Supply Current		V_{BUS} = 5V, Nothing Attach		180		μA
Input Supply Voltage UVLO Threshold	UVLO			3.3		V
UVLO Threshold Hysteresis	$UVLO_{(HYS.)}$			300		mV
NMOS Gate Driver						
SRCGC Sourcing Current		0V ≤ V_{SRCGC} – V_{BUSC} ≤ 6V		TBD		μA
Sourcing Voltage (ON) between SRCGC and VBUS			5		15	V
VBUSC						
VBUSC Bleed Discharge Resistance	$R_{\_CBLEED}$		8	10	12.5	kΩ
VBUSC Discharge Resistance	$R_{\_CDIS}$			400		Ω
USB Type-C						
SRC CC Current	I_{CC_3A}	Cable is attached whit Rd, PD Disabled	304	330	356	μA
D+/D- OV Threshold (Note 2)	$V_{\_DPDNOV}$	In DCP mode		7		V
D+/D- OV Threshold (Note 2)	$V_{\_DPDNOV}$	In HVDCP Mode		4		V
CCOV Rising (Note 2)	$V_{\_CCOV-rising}$			1.04* V_{DD}		V
CCOV Falling (Note 2)	$V_{\_CCOV-falling}$			V_{DD}		V
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
D+ High Glitch Filter Time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D− Low Glitch Filter Time	$T_{GLITCH(BC)-D^-\_L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\ CHANGE}$		20	40	60	ms
D− Pull-Down Resistance	$R_{D^-(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time (Note 2)	$T_{GLITCH-CONT-CHANGE}$		100		200	μs
D+ Leakage Resistance	$R_{DAT-LKG}$	V_{DD} = 3.2-6.4V,VD+ = 0.6-3.6V Switch SW1 = Off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD} =5V,SW1= 200μA			40	Ω
Up/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} = 40μA (9V), 70μA (12V), I_{DOWN} = 14μA (3.6V)		2		μA

Electrical Characteristics (Continued)

(VBUS=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
DCP Charging Mode							
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Voltage				0.44	0.48	0.52	V
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Impedance					900		kΩ
Apple Mode							
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Voltage				2.57	2.7	2.84	V
$D+_{\_2.7V}$/$D-_{\_2.7V}$ Line Output Impedance					33.6		kΩ
D− Section (FCP or SCP)							
D− Tx Valid Output High	V_{TX-VOH}			2.55		3.6	V
D− Tx Valid Output Low	V_{TX-VOL}					0.3	V
D− Rx Valid Output High	V_{RX-VIH}			1.4		3.6	V
D− Rx Valid Output Low	V_{RX-VIL}					1.0	V
D− Output Pull-Low Resistance(Note 2)	R_{PD}			400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	f_{CLK} = 125kHz		144	160	180	μs
Regulator Section							
Voltage Control Loop Reference	V_{REF}			1.227	1.24	1.252	V
Current control Loop Reference	CS+	Rsense =10mΩ	In SCP		60		mV
			In QC		36		mV
			In USB-PD		120% *I_{OUT}		mV
OPTO Sinking Current	I_{OPTO}				27	80	mA

Note 2: Not production tested.

Application Information

JD6621 is an integrated USB Power Delivery 3.0 controller that supports USB PD 3.0 Programmable Power Supply (PPS) specification and USB high voltage dedicated charging protocol (HVDCP), which can be used for Qualcomm's QC 2.0 / 3.0 / 3 +, AFC, FCP and SCP, Apple and other protocol specifications. JD6621 supports a variety of fast charging protocols, which can fast charge most Portable devices. It can be applied to charging adapters, car chargers, power strips and other USB output power devices.

USB Type-C / USB-PD Protocol

JD6621 is used for the USB Type-C interface to support the role of Source. When the sink device is connected, JD6621 will provide 3A current capability on the CC pin. It supports USB-PD 3.0 PPS and compatible with USB-PD 2.0 protocol. The output provides fixed voltage 5V/9V/12V/15V/20V, which can connect an external resistor to select the PDO voltage/current. (Pease refer to page 3 for select the RPDO and power configuration).

QC 2.0/3.0/3+ Protocol

JD6621 supports Qualcomm's QC 2.0/3.0/3+ charging protocol. The output voltage range is setting the class A or class B, please refer to the page 2 select the RPDO and power configuration. It supports output voltage range of QC 2.0 Class A (5V/9V/12V) and Class B (5V/9V/12V/20V), It also supports output voltage range of QC 3.0 Class A (3.6V to 12V, 200mV per step) and Class B (3.6V to 20V, 200mV per step). The step voltage of QC3+ is 20mV.

AFC/FCP/SCP Protocol

The JD6621 supports AFC protocol, the output voltage range is 5V/9V, and it supports FCP protocol, the output voltage range is 5V/9V/12V, it also supports SCP protocol, the charge capability is 4.5V/5A.

CC/CV Control

JD6621 supports constant current (CC)/constant voltage (CV) regulation. The constant voltage (CV) regulation is implemented by detecting the output voltage on the FBO pin via the resistor divider and constant voltage regulation control with compared internal reference voltage of the CV operational amplifier. The constant current (CC) regulation is implemented by detecting the output current via the resistor Rsense and constant current regulation control with compared internal reference voltage of the CC operational amplifier. If the output current is lower than the CC threshold and the output voltage will be adjusted to the default voltage. When the output current above the CC threshold, the output voltage will drop and the output current will be limited to the maximum current.

VBUSC Function

The VBUSC is monitoring the voltage and discharge the output for the implementation of a compliant USB Type-C application.

SRCG Driver

JD6621 provides a gate driver for controlling external N-MOSFET. The gate driver not only can control N-MOSFET smooth turn on to avoid VBUSC drops in the capacitive load condition but also provide quickly turn-off in any fault condition.

Multi-Port Control

JD6621 can realize the application of multiple USB-C ports share one power source. Connect the MPC pin of the chip to the bus, and connect a resistance of 100KΩ to the GND on the bus. Each chip transmits information through the bus, and then distributes the fixed rated power.

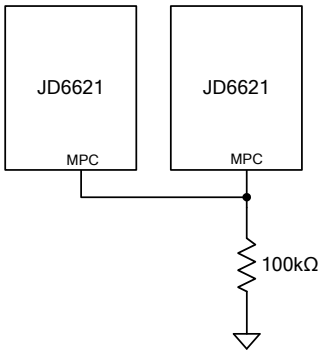


Figure 3. Multi-Port Control (MPC) Application

Application Information (Continued)

VBUS Over-Voltage Protection

JD6621 supports over-voltage protection of VBUS pin. When VBUS voltage is larger than the OVP threshold (24V typ.), GATE pin goes to low level to turn off blocking N-MOSFET. When the fault is removed, the GATE driver recovers to normal operation.

Configuration Channel Protection

JD6621 supports over-voltage protection of CC1/CC2 pin. When CC1/CC2 pin is touched by the external power in abnormal situation, the CC1/CC2 pin of both sink device and source device may be damaged. In order to protect the CC1/CC2 pin of the devices from damage in abnormal situation, the JD6621 will return the output voltage to default output voltage 5V.

Data Line Protection

JD6621 supports overvoltage protection of D+/D− pin. When D+/D− pin is touched by the output voltage in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the D+/D− pin of the devices from damage in abnormal situation, the JD6621 will return the output voltage to default output voltage 5V when the voltage of D+/D− pin is touched larger than 7.5V. If operating in HVDCP mode, the over voltage protection of D+/D- pin is 4V.

Over Temperature Protection

The JD6621 measures the temperature by the voltage at the TS pin. This voltage is typically generated by a negative-temperature coefficient thermistor. The JD6621 compares this voltage against its internal threshold voltages to determine if over temperature protection is triggered. The NTC thermistor shall use 100kohm. The default of OTP trip point is 125℃.

VDDM

Connect a 1uF ceramic capacitor between the VDDM and GND, This helps stabilize the internal regulator voltage.

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow general guidelines shown as below:

1. Place feedback resistors close to the FB pin.
2. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and the filter for current sense should be placed near the IC.

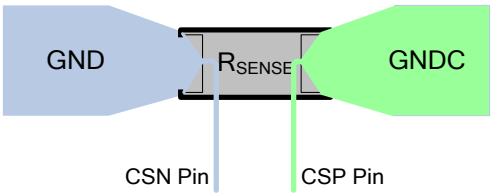
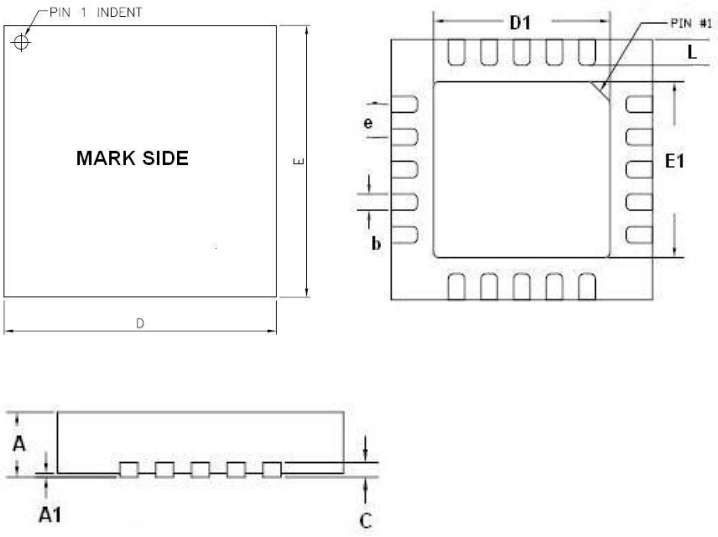


Figure 4. Current Sense

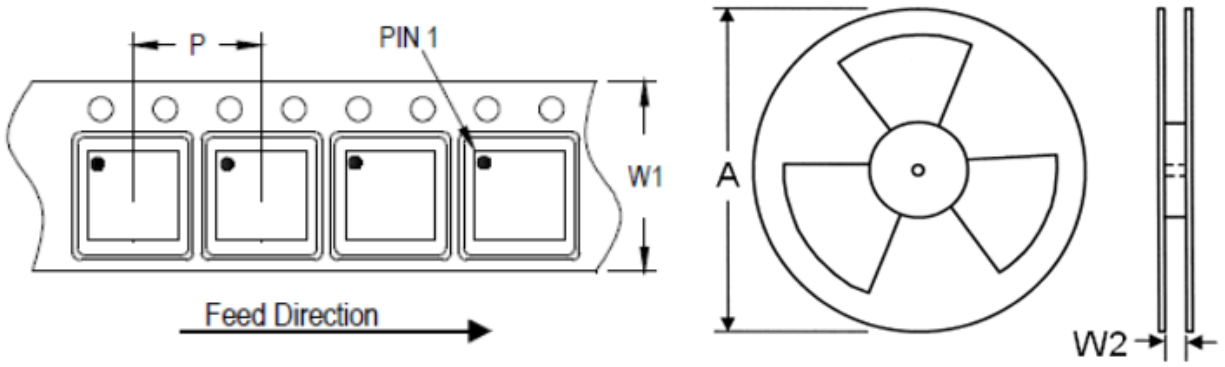
Outline Information

TQFN-20L 4mm × 4mm (pitch 0.5mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.25
E	4.00 BSC	
D	4.00 BSC	
L	0.30	0.50
b	0.20	0.30
e	0.50 BSC	
E1	2.45	2.75
D1	2.45	2.75

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000